National Semiconductor

PRELIMINARY

DP83840
10/100 Mb/s Ethernet Physical Layer

General Description

The DP83840 is a Physical Layer device for Ethernet 10BASE-T and 100BASE-X using category 5 Unshielded, Type 1 Shielded and Fiber Optic cables.

This VLSI device is designed for easy implementation of 10/100 Mb/s Ethernet LANs. It interfaces to the PMD sublayer through National Semiconductor's DP83223 Twisted Pair Transceiver, and to the MAC layer through a Media Independent Interface (MII), ensuring interoperability between products from different vendors.

The DP83840 is designed with National Semiconductor's BiCMOS process. Its system architecture is based on the integration of several of National Semiconductor's industry proven core technologies as listed below:

— 10BASE-T ENDEC/Transceiver module to provide the 10 Mb/s IEEE 802.3 functions

— Clock Recovery/Generator Modules from National Semiconductor's leading FDDI product

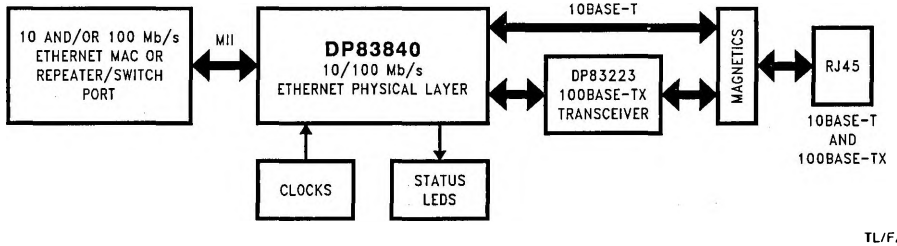
— FDDI Stream Cipher (Cyclone)

— 100BASE-X physical coding sub-layer (PCS) and control logic that integrate the core modules into a dual speed Ethernet physical layer controller

Features

- IEEE 802.3 10BASE-T compatible—ENDEC and UTP/STP transceivers and filters built-in
- IEEE 802.3u 100BASE-X compatible—support for 2 pair Category 5 UTP (100m), Type 1 STP and Fiber Optic Transceivers—Connects directly to the DP83223 Twisted Pair Transceiver
- ANSI X3T12 TP-PMD compatible
- IEEE 802.3u Auto-Negotiation for automatic speed selection
- IEEE 802.3u compatible Media Independent Interface (MII) with Serial Management Interface
- Integrated high performance 100 Mb/s clock recovery circuitry requiring no external filters
- Full Duplex support for 10 and 100 Mb/s
- MII Serial 10 Mb/s output mode
- Fully configurable node and repeater modes—allows operation in either application
- Programmable loopback modes for easy system diagnostics
- Flexible LED support
- IEEE 1149.1 Standard Test Access Port and Boundary-Scan compatible
- Small footprint 100-pin PQFP package

System Diagram



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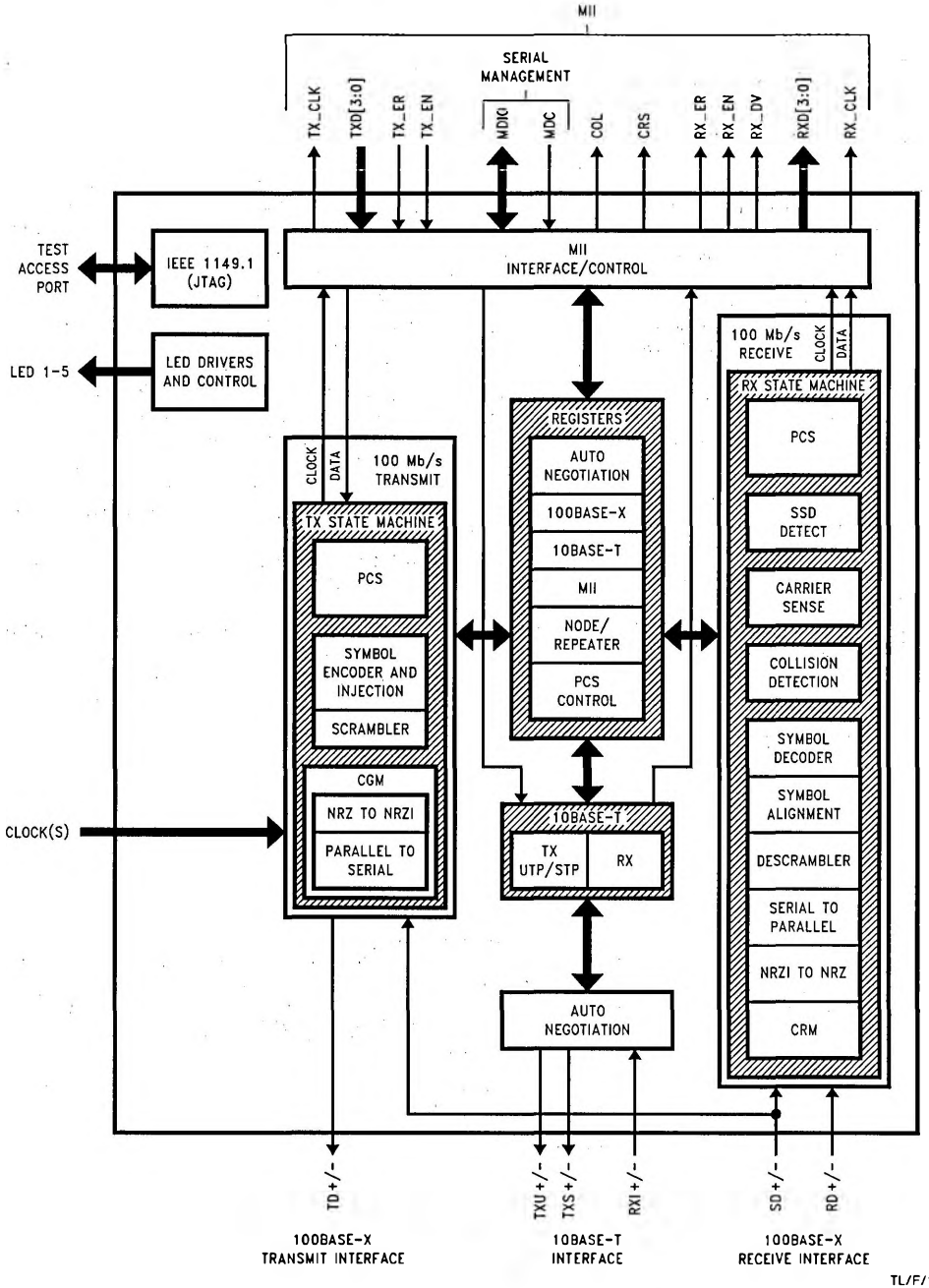
Block Diagram



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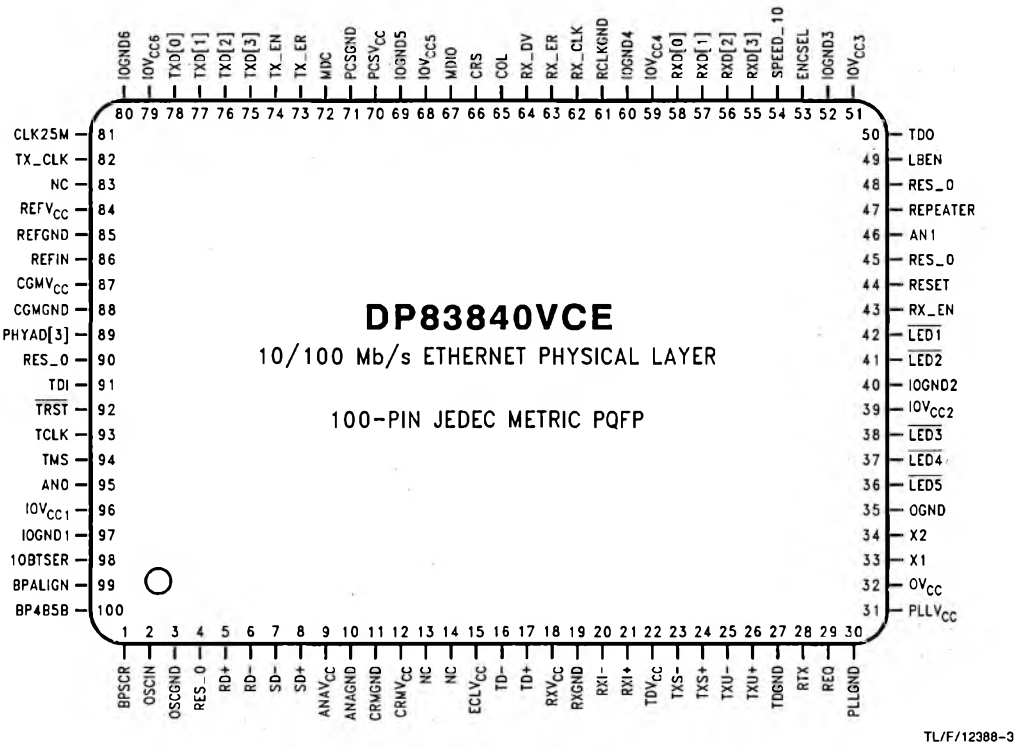

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FIGURE 1. DP83840 Pin Connection Diagram

2.0 Pin Description

The DP83840 pins are classified into the following interface categories (each interface is described in the sections that follow):

MII INTERFACE
100 Mb/s SERIAL PMD INTERFACE
10 Mb/s INTERFACE
CLOCK INTERFACE
DEVICE CONFIGURATION INTERFACE
LED INTERFACE
IEEE 1149.1 INTERFACE
PHY ADDRESS INTERFACE
MISCELLANEOUS PINS
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2.1 MII INTERFACE

Signal Name	Type	Pin #	Description
TX_CLK	O, Z	82	**TRANSMIT CLOCK:** Transmit clock output from the DP83840: — 25 MHz nibble transmit clock derived from Clock Generator Module's (CGM) PLL in 100BASE-TX mode — 2.5 MHz transmit clock in 10BASE-T nibble mode — 10 MHz transmit clock in 10BASE-T serial mode
TXD[3] TXD[2] TXD[1] TXD[0]	I, J	75 76 77 78	**TRANSMIT DATA:** Transmit data input pins for nibble data from the MII in 100 Mb/s or 10 Mb/s nibble mode (25 MHz for 100 Mb/s mode, 2.5 MHz for 10 Mb/s nibble mode). In 10 Mb/s serial mode, the TXD[0] pin is used as the serial data input pin. TXD[3:1] are ignored.
TX_EN	I, J	74	**TRANSMIT ENABLE:** Active high input indicates the presence of valid nibble data on TXD[3:0] for both 100 Mb/s or 10 Mb/s nibble mode. In 10 Mb/s serial mode, active high indicates the presence of valid 10 Mb/s data on TXD[0].
TX_ER	I, J	73	**TRANSMIT ERROR:** In 100 Mb/s mode, when this signal is high and TX_EN is active the HALT symbol is substituted for the actual data nibble. In 10 Mb/s mode, this input is ignored. In encoder bypass mode (BP_4B5B or BP_ALIGN) TX_ER becomes the TXD[4] pin, the fifth TXD data bit.
MDC	I, J	72	**MANAGEMENT DATA CLOCK:** Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 2.5 MHz.
MDIO	I/O, J	67	**MANAGEMENT DATA I/O:** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 4.7 kΩ pullup resistor.
CRS (PHYAD[2])	I/O, Z, J	66	**CARRIER SENSE:** This pin is asserted high to indicate the presence of carrier due to receive or transmit activities in 10BASE-T or 100BASE-X Half Duplex modes. In Repeater, Full Duplex, or Loopback mode a logic 1 indicates presence of carrier due only to receive activity. This is also the PHY address sensing (PHYAD[2]) pin for multiple PHY applications—see Section 2.8 for more details.
COL	O, Z, J	65	**COLLISION DETECT:** Asserted high to indicate detection of collision conditions in 10 Mb/s and 100 Mb/s Half Duplex modes. In 10BASE-T Half Duplex mode with Heartbeat asserted (bit 4, register 1Ch), it is also asserted for a duration of approximately 1 μs at the end of transmission to indicate CD heartbeat. In Full Duplex mode this signal is always logic 0. There is no heartbeat function in this mode.
RX_CLK	O, Z	62	**RECEIVE CLOCK:** Provides the recovered receive clock for different modes of operation: — 25 MHz nibble clock in 100 Mb/s mode — 2.5 MHz nibble clock in 10 Mb/s nibble mode — 10 MHz receive clock in 10 Mb/s serial mode

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE® output J = IEEE 1149.1 pin

2.0 Pin Description (Continued)

2.1 MII INTERFACE (Continued)

Signal Name	Type	Pin #	Description
RX_ER (PHYAD[4])	O, Z, J	63	**RECEIVE ERROR:** Asserted high to indicate that an invalid symbol has been detected inside a received packet in 100 Mb/s mode. In a 5B/4B decoder bypass mode (BP_4B5B or BP_ALIGN modes), RX_ER becomes RXD[4], the fifth RXD data bit of the 5B symbol. This is also the PHY address sensing (PHYAD[4]) pin for multiple PHY applications—see Section 2.8 for more details.
RX_DV	O, Z, J	64	**RECEIVE DATA VALID:** Asserted high to indicate that valid data is present on RXD[3:0].
RXD[3] RXD[2] RXD[1] RXD[0]	O, Z, J	55 56 57 58	**RECEIVE DATA:** Nibble wide receive data (synchronous to RX_CLK—25 MHz for 100BASE-X mode, 2.5 MHz for 10BASE-T nibble mode). Data is driven on the falling edge of RX_CLK. In 10 Mb/s serial mode, the RXD[0] pin is used as the data output pin. RXD[3:1] are don't care.
RX_EN	I, J	43	**RECEIVE ENABLE:** Active high enable for receive signals RXD[3:0], RX_CLK, RX_DV and RX_ER. A low on this input tri-states these output pins. For normal operation in a node application this pin should be pulled high.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.2 100 Mb/S SERIAL PMD INTERFACE

Signal Name	Type	Pin #	Description
SPEED_10	O, J	54	**SPEED 10 Mb/s:** Indicates 10 Mb/s operation when high. Indicates 100 Mb/s operation when low. This pin can be used to drive a low current LED to indicate 100 Mb/s speed if required.
ENCSEL (PHYAD[1])	I/O, J	53	**ENCODE SELECT:** Used to select binary or MLT-3 coding scheme in the PMD transceiver (at the DP83223, logic high selects binary coding scheme and logic low selects MLT-3 coding scheme). This is also the PHY address sensing (PHYAD[1]) pin for multiple PHY applications—see Section 2.8 for more details.
LBEN (PHYAD[0])	I/O, J	49	**LOOPBACK ENABLE:** This pin should be connected to the Loopback Enable pin of a DP83223 100 Mb/s Transceiver: 1 = Loopback enabled 0 = Loopback disabled In 10 Mb/s modes, this output has no meaning. This is also the PHY address sensing (PHYAD[0]) pin for multiple PHY applications—see Section 2.8 for more details.
TD− TD+	O (ECL)	16 17	**TRANSMIT DATA:** Differential ECL 125 Mb/s serialized transmit data outputs to the DP83223 Twister.
SD− SD+	I (ECL)	7 8	**SIGNAL DETECT:** Differential ECL signal detect inputs. Indicates that a signal is present at the DP83223 receive inputs as specified by the TP-PMD ANSI standard.
RD− RD+	I (ECL)	6 5	**RECEIVE DATA:** Differential ECL 125 Mb/s receive data inputs.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.0 Pin Description (Continued)

2.3 10 Mb/S INTERFACE

Signal Name	Type	Pin #	Description
REQ	I	29	**EQUALIZATION RESISTOR:** A resistor connected between this pin and GND or V_{CC} adjusts the equalization step amplitude on the 10BASE-T Manchester encoded transmit data (TXU+/− or TXS+/−). Typically no resistor is required for operation with cable lengths less than 100m. Great care must be taken to ensure system timing integrity when using cable lengths greater than 100m. Refer to the IEEE 802.3u standard, Clause 29 for more details on system topology issues. The equations to calculate this resistor value are still under investigation. Currently, this value must be determined empirically.
RTX	I	28	**EXTENDED CABLE RESISTOR:** A resistor connected between this pin and GND or V_{CC} adjusts the amplitude of the differential transmit outputs (TXU+/− or TXS+/−). Typically no resistor is required for operation with cable lengths less than 100m. Great care must be taken to ensure system timing integrity when using cable lengths greater than 100m. Refer to the IEEE 802.3u standard, Clause 29 for more details on system topology issues. The equations to calculate this resistor value are still under investigation. Currently, this value must be determined empirically.
TXU− TXU+	O	25 26	**UNSHIELDED TWISTED PAIR OUTPUT:** This differential output pair is the filtered 10BASE-T transmit data for UTP cable.
TXS− TXS+	O	23 24	**SHIELDED TWISTED PAIR OUTPUT:** This differential output pair is the filtered 10BASE-T transmit data for STP cable.
RXI− RXI+	I	20 21	**TWISTED PAIR RECEIVE INPUT:** These are the differential 10BASE-T receive data inputs for either STP or UTP.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.4 CLOCK INTERFACE

Signal Name	Type	Pin #	Description
REFIN	I	86	**REFERENCE INPUT:** 25 MHz TTL reference clock input. Can be supplied from an external oscillator module or from the CLK25M output.
CLK25M	O, Z	81	**25 MHz CLOCK OUTPUT:** Derived from the 50 MHz OSCIN input.
OSCIN	I	2	**OSCILLATOR INPUT:** 50 MHz ± 50 ppm external TTL oscillator input. If not used, pull down to GND with a 4.7 kΩ resistor.
X2	O	34	**CRYSTAL OSCILLATOR OUTPUT:** External 20 MHz ± 0.005% crystal connection. Used for 10BASE-T timing. When using an external 20 MHz oscillator connected to X1, leave this pin unconnected.
X1	I	33	**CRYSTAL OSCILLATOR INPUT:** External 20 MHz ± 0.005% crystal connection. Used for 10BASE-T timing and Auto-Negotiation. If not used, this pin should be tied to V_{CC} either directly or via a pull-up resistor—typically 4.7 kΩ. The DP83840 detects this condition, enables the internal ÷2.5 divider and switches the 10 Mb/s and Auto-Negotiation circuitry to the internally derived 20 MHz clock.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.0 Pin Description (Continued)

2.5 DEVICE CONFIGURATION INTERFACE

Signal Name	Type	Pin #	Description
AN0	I	95	**AN0:** This is a three level input pin (i.e., 1, M, 0) that works in conjunction with the AN1 pin to control the forced or advertised operating mode of the DP83840 according to the following table. The value on this pin is set by either connecting the input to GND or V_{CC} (0 or 1) or leaving it unconnected (M). The unconnected state, M, refers to the mid level ($V_{CC} \div 2$) set by internal resistors ($\sim$ 3 kΩ). This value is latched into the DP83840 at power-up/reset. See Section 3.9 for more details. **AN1 AN0 — Forced Mode** 0 M — 10BASE-T, Half-Duplex without Auto-Negotiation 1 M — 10BASE-T, Full Duplex without Auto-Negotiation M 0 — 100BASE-TX, Half-Duplex without Auto-Negotiation M 1 — 100BASE-TX, Full Duplex without Auto-Negotiation **AN1 AN0 — Advertised Mode** M M — All capable (i.e. Full Duplex for 10BASE-T and 100BASE-TX) advertised via Auto-Negotiation 0 0 — 10BASE-T, Half-Duplex advertised via Auto-Negotiation 0 1 — 10BASE-T, Full Duplex advertised via Auto-Negotiation 1 0 — 100BASE-TX, Half-Duplex advertised via Auto-Negotiation 1 1 — 100BASE-TX, Full Duplex advertised via Auto-Negotiation
AN1	I	46	**AN1:** This is a three level input pin (i.e., 1, M, 0) that works in conjunction with the AN0 pin to control the forced or advertised operating mode of the DP83840 according to the table given in the AN0 pin description above. The value on this pin is set by either connecting the input to GND or V_{CC} (0 or 1) or leaving it unconnected (M). This value is latched into the DP83840 at power-up/reset. See Section 3.9 for more details.
REPEATER	I, J	47	**REPEATER/NODE MODE:** Selects REPEATER mode when set high and NODE mode when set low. In REPEATER mode or NODE mode with Full Duplex configured, the Carrier Sense (CRS) output from the DP83840 is asserted due to receive activity only. In NODE mode, and not configured for Full Duplex operation, CRS is asserted due to either receive and transmit activity. At power-up/reset, the value on this pin (set by a pull-up or pull-down resistor, typically 4.7 kΩ) is latched to bit 12 of the PCS Configuration Register, address 17h.
10BTSER	I, J	98	**SERIAL/NIBBLE SELECT:** 10 Mb/s Serial Operation: When set high, this input selects serial data transfer mode. Manchester encoded transmit and receive data is exchanged serially with a 10 MHz clock rate on the least significant bits of the nibble-wide MII data buses, pins TXD[0] and RXD[0] respectively. This mode is intended for use with the DP83840 connected to a device (MAC or Repeater) that has a 10 Mb/s serial interface. Serial operation is not supported in 100 Mb/s mode, so for 100 Mb/s this input is ignored. 10 and 100 Mb/s Nibble Operation: When set low, this input selects the MII compliant nibble data transfer mode. Transmit and receive data is exchanged in nibbles on the TXD[3:0] and RXD[3:0] pins respectively. At power-up/reset, the value on this pin (set by a pull-up or pull-down resistor, typically 4.7 kΩ) is latched to bit 9 of the 10BASE-T Status Register, address 1Bh.
BPALIGN	I, J	99	**BYPASS ALIGNMENT:** Allows 100 Mb/s transmit and receive data streams to bypass all of the transmit and receive operations when set high. Refer to *Figures 4* and *5*. At power-up/reset, the value on this pin (set by a pull-up or pull-down resistor, typically 4.7 kΩ) is latched into bit 12 of the Loopback, Bypass and Receiver Error Mask Register, address 18h.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.0 Pin Description (Continued)

2.5 DEVICE CONFIGURATION INTERFACE (Continued)

Signal Name	Type	Pin #	Description
BP4B5B	I, J	100	**BYPASS 4B5B ENCODER/DECODER:** Allows 100 Mb/s transmit and receive data streams to bypass the 4B to 5B encoder and 5B to 4B decoder circuits when set high. At power-up/reset, the value on this pin (set by a pull-up or pull-down resistor, typically 4.7 kΩ) is latched into bit 14 of the Loopback, Bypass and Receiver Error Mask Register, address 18h.
BPSCR	I, J	1	**BYPASS SCRAMBLER/DESCRAMBLER:** Allows 100 Mb/s transmit and receive data streams to bypass the scrambler and descrambler circuits when set high. At power-up/reset, the value on this pin (set by a pull-up or pull-down resistor, typically 4.7 kΩ) is latched into bit 13 of the Loopback, Bypass and Receiver Error Mask Register, address 18h.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.6 LED INTERFACE

These outputs can be used to drive LEDs directly, or can be used to provide status information to a network management device. Refer to *Figure 12* for the LED connection diagram. An LED indication of 100 Mb/s operation can be obtained by connecting a low current LED (and its associated resistor) to the SPEED_10 pin (54). See Section 2.2.

Signal Name	Type	Pin #	Description
$\overline{\text{LED1}}$	O, J	42	**TRANSMIT LED:** Indicates the presence of transmit activity for 10 Mb/s and 100 Mb/s operation. Active low. If bit 2 (LED1_MODE) of the PCS Configuration Register (address 17h) is set high, then the $\overline{\text{LED1}}$ pin function is changed to indicate the status of the Disconnect Function as defined by the state of bit 5 (CON_STATUS) in the PHY address register (address 19h). The DP83840 incorporates a "monostable" function on the $\overline{\text{LED1}}$ output. This ensures that even minimum size packets generate adequate LED ON time to be visible.
$\overline{\text{LED2}}$	O, J	41	**RECEIVE LED:** Indicates the presence of any receive activity (CRS active) for 10 Mb/s and 100 Mb/s operation. Active low. The DP83840 incorporates a "monostable" function on the $\overline{\text{LED2}}$ output. This ensures that even minimum size packets generate adequate LED ON time to be visible.
$\overline{\text{LED3}}$	O, J	38	**LINK LED:** Indicates Good Link status for 10 Mb/s and 100 Mb/s operation. Active low.
$\overline{\text{LED4}}$	O, J	37	**POLARITY/FULL DUPLEX LED:** Indicates Good Polarity status for 10 Mb/s operation. Indicates Full Duplex mode status for 100 Mb/s operation. Active low. If bit 1 (LED4_MODE) in the PCS Configuration Register (address 17h) is set high, the $\overline{\text{LED4}}$ pin function is changed to indicate Full Duplex mode status for 10 Mb/s and 100 Mb/s operation.
$\overline{\text{LED5}}$	O, J	36	**COLLISION LED:** Indicates the presence of collision activity for 10 Mb/s and 100 Mb/s operation. This LED has no meaning for 10 Mb/s or 100 Mb/s Full Duplex operation. Active low.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.7 IEEE 1149.1 INTERFACE

The IEEE 1149.1 Standard Test Access Port and Boundary Scan (sometimes referred to as JTAG) interface signals allow system level boundary scan to be performed.

Signal Name	Type	Pin #	Description
TDO	O, Z	50	**TEST DATA OUTPUT:** Serial instruction/test output data for the IEEE 1149.1 scan chain. If Boundary-Scan is not implemented this pin should be left unconnected (NC).
TDI	I	91	**TEST DATA INPUT:** Serial instruction/test input data for the IEEE 1149.1 scan chain.
$\overline{\text{TRST}}$	I	92	**TEST RESET:** An asynchronous low going pulse will reset and initialize the IEEE 1149.1 test circuitry. If Boundary-Scan is not implemented, this pin should be left unconnected (NC) since it has an internal pull-up resistor (10 kΩ).

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.0 Pin Description (Continued)

2.7 IEEE 1149.1 INTERFACE (Continued)

Signal Name	Type	Pin #	Description
TCLK	I	93	**TEST CLOCK:** Test clock for the IEEE 1149.1 circuitry. This pin should be pulled to GND with an appropriate resistor (10 kΩ).
TMS	I	94	**TEST MODE SELECT:** Control input to the IEEE 1149.1 test circuitry. If Boundary-Scan is not implemented, this pin should be left unconnected (NC) since it has an internal pull-up resistor (10 kΩ).

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.8 PHY ADDRESS INTERFACE

It should be noted that while PHYAD[4:0] provides up to 32 unique PHY address options, an address selection of all zeros (00000) will result in a PHY isolation condition. See the Isolate bit description in the BMCR, address 00h, Section 4.2.

Signal Name	Type	Pin #	Description
LBEN (PHYAD[0])	I/O, J	49	**PHY ADDRESS [0]:** PHY address sensing pin (bit 0) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 kΩ) to this pin as required. The pull-up/pull-down status of this pin is latched into the PHYAD address register (address 19h) during power up/reset. This pin is also the Loopback Enable output pin (LBEN) for the 100 Mb/s Serial PMD Interface. See Section 2.2 for more details.
ENCSEL (PHYAD[1])	I/O, J	53	**PHY ADDRESS [1]:** PHY address sensing pin (bit 1) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 kΩ) to this pin as required. The pull-up/pull-down status of this pin is latched into the PHYAD address register (address 19h) during power up/reset. This pin is also the Encode Select output pin (ENCSEL) for the 100 Mb/s Serial PMD Interface. See Section 2.2 for more details.
CRS (PHYAD[2])	I/O, J	66	**PHY ADDRESS [2]:** PHY address sensing pin (bit 2) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 kΩ) to this pin as required. The pull-up/pull-down status of this pin is latched into the PHYAD address register (address 19h) during power up/reset. This pin is also the Carrier Sense output pin (CRS) for the MII Interface. See Section 2.1 for more details.
PHYAD[3]	I	89	**PHY ADDRESS [3]:** PHY address sensing pin (bit 3) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 kΩ) to this pin as required. The pull-up/pull-down status of this pin is latched into the PHYAD address register (address 19h) during power up/reset. Since this input does not have a dual function, it is a good choice for providing a non-zero PHY address to the DP83840.
RX_ER (PHYAD[4])	I/O, Z, J	63	**PHY ADDRESS [4]:** PHY address sensing pin (bit 4) for multiple PHY applications. PHY address sensing is achieved by strapping a pull-up/pull-down resistor (typically 10 kΩ) to this pin as required. The pull-up/pull-down status of this pin is latched into the PHYAD address register (address 19h) during power up/reset. This pin is also the Receive Error output pin (RX_ER) for the MII Interface. See Section 2.1 for more details.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.0 Pin Description (Continued)

2.9 MISCELLANEOUS

Signal Name	Type	Pin #	Description
RESET	I, J	44	**RESET:** Active high input that initializes the DP83840.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.10 POWER AND GROUND PINS

The power (V_{CC}) and ground (GND) pins of the DP83840 are grouped in pairs into four categories—TTL/CMOS Input pairs, TTL/CMOS Output and I/O pairs, 10 Mb/s pairs and 100 Mb/s pairs. Great care must be taken with the layout of the power and ground supplies to this device. Each of the four categories of pairs should have its own isolated supplies. More details of the power and ground layout requirements are given in Sections 5.2, 5.3 and 5.4.

Pin Names	Pin #	Description
GROUP A—TTL/CMOS INPUT SUPPLY PAIRS		
IOV_{CC1}, IOGND1	96, 97	TTL Input/Output Supply #1
IOV_{CC2}, IOGND2	39, 40	TTL Input/Output Supply #2
IOV_{CC3}, IOGND3	51, 52	TTL Input/Output Supply #3
$PCSV_{CC}$, PCSGND	70, 71	Physical Coding Sublayer Supply
GROUP B—TTL/CMOS OUTPUT AND I/O SUPPLY PAIRS		
IOV_{CC4}, IOGND4	59, 60	TTL Input/Output Supply #4
RCLKGND	61	Receive Clock Ground, No Paired V_{CC}
IOV_{CC5}, IOGND5	68, 69	TTL Input/Output Supply #5
IOV_{CC6}, IOGND6	79, 80	TTL Input/Output Supply #6
$REFV_{CC}$, REFGND	84, 85	25 MHz Clock Supply
GROUP C—10 Mb/s SUPPLY PAIRS		
RXV_{CC}, RXGND	18, 19	Receive Section Supply
TDV_{CC}, TDGND	22, 27	Transmit Section Supply
$PLLV_{CC}$, PLLGND	31, 30	Phase Locked Loop Supply
OV_{CC}, OGND	32, 35	Internal Oscillator Supply
GROUP D—100 Mb/s SUPPLY PAIRS		
OSCGND	3	External Oscillator Input Ground—No Paired V_{CC}
$ANAV_{CC}$, ANAGND	9, 10	Analog Section Supply
$CRMV_{CC}$, CRMGND	12, 11	Clock Recovery Module Supply
$ECLV_{CC}$	15	ECL Outputs Supply
$CGMV_{CC}$, CGMGND	87, 88	Clock Generator Module Supply

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

2.11 SPECIAL CONNECT PINS

Signal Name	Type	Pin #	Description
NC		13 14 83	**NO CONNECT:** These pins are reserved for future use. Leave them unconnected (floating).
RES_0		4 45	**RESERVED_0:** These pins are reserved for future use. Connect them to the nearest ground plane. For future upgradability, connect these pins to GND via 0Ω resistors.
RES_0	J	48 90	**RESERVED_0:** These pins are reserved for future use. Connect them to the nearest ground plane. For future upgradability, connect these pins to GND via 0Ω resistors.

I = TTL/CMOS input O = TTL/CMOS output Z = TRI-STATE output J = IEEE 1149.1 pin

3.0 Functional Description

The DP83840 10/100 Mb/s Ethernet Physical Layer integrates a 100BASE-T Physical Coding Sub-layer (PCS) and a complete 10BASE-T module in a single chip. It provides a standard Media Independent Interface (MII) to communicate between the Physical Signaling and the Medium Access Control (MAC) layers for both 100BASE-X and 10BASE-T operations. It interfaces to a 100 Mb/s Physical Medium Dependent (PMD) transceiver, such as the DP83223.

The 100BASE-X section of the device consists of the following functional blocks:

- Transmitter
- Receiver
- Clock Generation Module (CGM)
- Clock Recovery Module (CRM)

The 10BASE-T section of the device consists of the 10 Mb/s transceiver module with filters and an ENDEC module.

The 100BASE-X and 10BASE-T sections share the following functional blocks:

- PCS Control
- MII Registers
- IEEE 1149.1 Controller
- IEEE 802.3u Auto-Negotiation

Each of these functional blocks is described below.

3.1 PCS CONTROL

The IEEE 802.3u 100BASE-X Standard defines the Physical Coding Sublayer (PCS) as the transmit, receive and carrier sense functions. These functions within the DP83840 are controlled via external pins and internal registers via the MII serial management interface.

3.1.1 100BASE-X Bypass Options

The DP83840 incorporates a highly flexible transmit and receive channel architecture. Each of the major 100BASE-X transmit and receive functional blocks of the DP83840 are selectively bypassable to provide increased flexibility for various applications.

3.1.1.1 Bypass 4B5B and 5B4B

The 100BASE-X 4B5B symbol encoder in the transmit channel and the 100BASE-X 5B4B symbol decoder in the receive channel may be bypassed by setting the BP_4B5B bit in the LBREMR (bit 14, register address 18h). The default value for this bit is set by the BP4B5B pin 100 at power-up/reset.

3.1.1.2 Bypass Scrambler and Descrambler

The 100BASE-X scrambler in the transmit channel and the 100BASE-X descrambler in the receive channel may be bypassed by setting the BP_SCR bit in the LBREMR (bit 13, register address 18h). The default value for this bit is set by the BPSCR signal (pin 1) at power-up/reset.

3.1.1.3 Bypass NRZI Encoder and Decoder

The 100BASE-X NRZI encoder in the transmit channel and the 100BASE-X NRZI decoder in the receive channel may be bypassed by setting the NRZI_EN bit in the PCR (bit 15, register address 17h). The default for this bit is a 1, which enables the NRZI encoder and decoder.

3.1.1.4 Bypass Align

The 100BASE-X transmit channel operations (4B5B symbol encoder, scrambler and NRZ to NRZI) and the 100BASE-X receive channel operations (NRZI to NRZ, descrambler and 4B5B symbol decoding) may all be bypassed by setting the BP_ALIGN bit in the LBREMR (bit 12, register address 18h). The default value for this bit is set by the BP_ALIGN signal (pin 99) at power-up/reset.

The bypass align function is intended for those repeater applications where none of the transmit and receive channel operations are required.

3.1.2 Repeater Mode

The DP83840 Carrier Sense (CRS) operation depends on the value of the REPEATER bit in the PCR (bit 12, register address 17h). When set high, the CRS output (pin 66) is asserted for receive activity only. When set low, the CRS output is asserted for either receive or transmit activity.

The default value for this bit is set by the REPEATER pin 66 at power-up/reset.

3.1.3 MII Control

The DP83840 has 3 basic MII operating modes:

3.1.3.1 100 Mb/s Operation

For 100 Mb/s operation, the MII operates in nibble mode with a clock rate of 25 MHz. This clock rate is independent of bypass conditions.

In normal (non-bypassed) operation the MII data at RXD[3:0] and TXD[3:0] is nibble wide. In bypass mode (BP_4B5B or BP_ALIGN set) the MII data takes the form of 5-bit symbols. The lowest significant 4 bits appear on TXD[3:0] and RXD[3:0] as normal, and the most significant bits (TXD[4] and RXD[4]) appear on the TX_ER and RX_ER pins respectively.

3.1.3.2 10 Mb/s Nibble Mode Operation

For 10 Mb/s nibble mode operation, the MII clock rate is 2.5 MHz. The 100BASE-X bypass functions do not apply to 10 Mb/s operation. This is the default 10 Mb/s mode of operation.

3.1.3.3 10 Mb/s Serial Mode Operation

For applications that have external ENDECs for 10 Mb/s operation, the DP83840 accepts Manchester encoded serial data on the TXD[0] input and provides Manchester encoded serial data output on RXD[0] with a clock rate of 10 MHz.

This mode is selected by setting the 10BT_SER bit in the 10BTSR (bit 9, register address 1Bh). The default value for this bit is set by the 10BTSER pin 98 at power-up/reset.

3.2 MII SERIAL MANAGEMENT REGISTER ACCESS

The MII specification defines a set of thirty-two 16-bit status and control registers that are accessible through the serial management data interface pins MDC and MDIO. The DP83840 implements all the required MII registers and a subset of optional registers. The registers are fully described in Section 4. The serial management access protocol is described below.

3.2.1 Serial Management Access Protocol

The serial control interface consists of two pins, Management Data Clock (MDC) and Management Data Input/Output (MDIO). MDC has a maximum clock rate of 2.5 MHz. The MDIO line is bi-directional and may be shared by up to 32 devices. The MDIO frame format is shown in Table I.

3.0 Functional Description (Continued)

The MDIO pin requires a pull-up resistor (4.7 kΩ) which, during IDLE condition, will pull MDIO high. Prior to initiating any transaction, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide the DP83840 with a sequence that can be used to establish synchronization.

The DP83840 waits until it has received this sequence before responding to any other transaction.

The Start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state.

Turnaround is an idle bit time inserted between the Register Address field and the Data field. To avoid contention, no device actively drives the MDIO signal during the first bit of Turnaround during a read transaction. The addressed DP83840 drives the MDIO with a zero for the second bit of Turnaround and follows this with the required data. *Figure 2* shows the timing relationship between MDC and the MDIO as driven/received by the Station Management Entity (STA) and the DP83840 (PHY) for a typical register read access.

For write transactions, the station management entity writes data to an addressed DP83840 eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity inserting <10> for these two bits. *Figure 3* shows the timing relationship for a typical MII register write access.

3.2.2 PHY Address Sensing

The DP83840 can be set to respond to any of the possible 32 PHY addresses. Note that each DP83840 connected to a common MII must have a unique address.

The DP83840 provides five PHY address pins, the state of which are latched into the PHY Address Register (PAR) at system power-up/reset. These pins are described in Section 2.8.

3.2.3 MII Management

The MII may be used to connect PHY devices to MAC or repeater devices in 10/100 Mb/s systems.

The management interface of the MII allows the configuration and control of multiple PHY devices, the gathering of status and error information, and the determination of the type and abilities of the attached PHY(s).

3.3 100BASE-X TRANSMITTER

The 100BASE-X transmitter consists of functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled 125 Mb/s serial data stream. This data stream may be routed either to a twisted pair PMD such as the DP83223 TWISTER for 100BASE-TX signaling, or to an optical PMD for 100BASE-FX applications. The block diagram in *Figure 4* provides an overview of each functional block within the 100BASE-X transmit section.

The Transmitter section consists of the following functional blocks:

- Symbol Encoder and Injection block (bypass option)
- Scrambler block (bypass option)
- NRZ to NRZI encoder block (bypass option)

The bypass option for each of the functional blocks within the 100BASE-X transmitter provides flexibility for applications such as 100 Mb/s repeaters where data conversion is not always required.

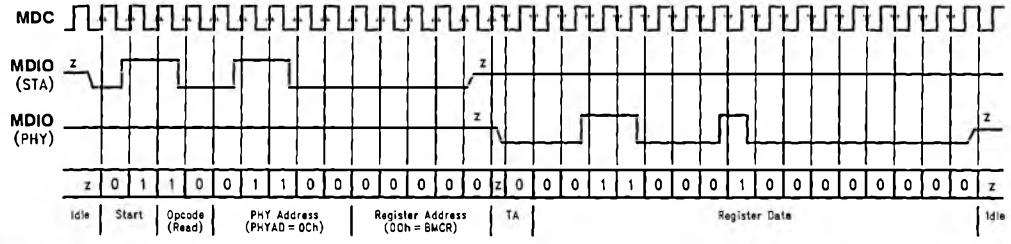

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FIGURE 2. Typical MDC/MDIO Read Operation

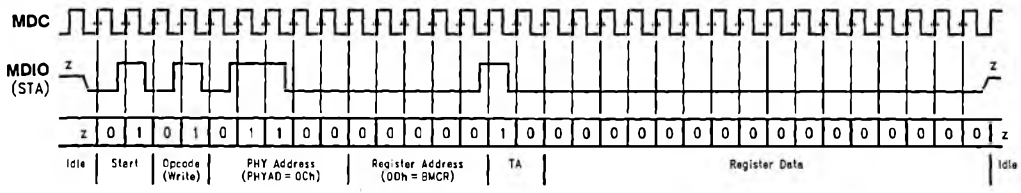

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FIGURE 3. Typical MDC/MDIO Write Operation

TABLE I. MII Management Serial Protocol

MII Management Serial Protocol	<idle> <start> <op code> <device addr> <reg addr> <turnaround> <data> <idle>
Read Operation	<idle> <01> <10> <AAAAA> <RRRRR> <Z0> <xxxx xxxx xxxx xxxx> <idle>
Write Operation	<idle> <01> <01> <AAAAA> <RRRRR> <10> <xxxx xxxx xxxx xxxx> <idle>

3.0 Functional Description (Continued)

3.3.1 100 Mb/s Transmit State Machine

The DP83840 implements the 100BASE-X transmit state machine diagram as given in the IEEE 802.3u Standard, Clause 24.

3.3.2 Symbol Encoding and Injection

The symbol encoder converts 4 bit (4B) nibble data generated by the MAC into 5 bit (5B) symbols for transmission. This conversion is required to allow control symbols to be combined with data symbols. Refer to Table II for 4B to 5B symbol mapping details.

The symbol encoder substitutes the first 8 bits of the MAC preamble with a J/K symbol pair (11000 10001). The symbol encoder continues to replace subsequent 4B codes with corresponding 5B symbols. At the end of the transmit packet, the symbol encoder injects the T/R symbol pair indicating end of frame.

The symbol encoder continuously injects IDLE symbols into the transmit data stream until the next transmit packet is detected.

3.3.3 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted pair cable (for 100BASE-TX applications). By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the PMD and on the cable would peak at frequencies related to repeating 5B sequences (i.e., continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is combined with the NRZ 5B data from the symbol encoder via an X-OR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB.

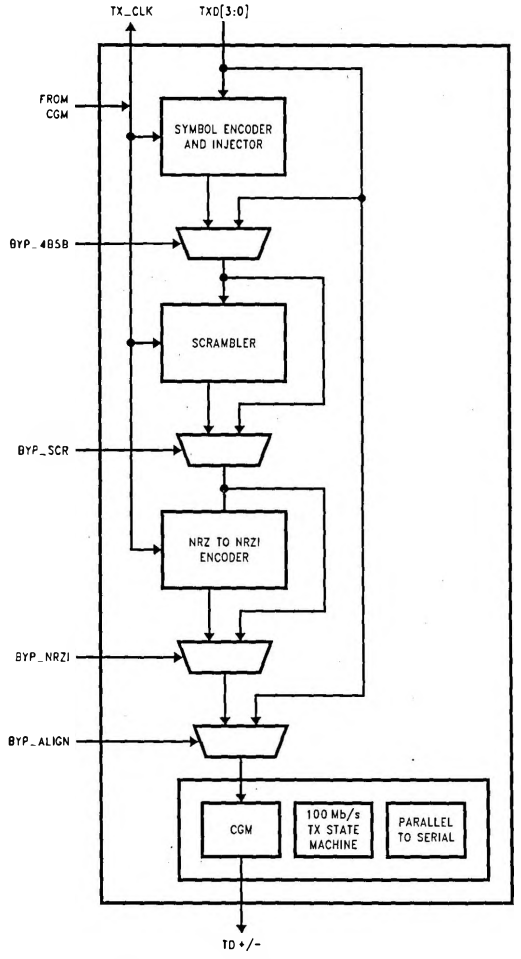

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FIGURE 4. 100BASE-X Transmitter

3.0 Functional Description (Continued)

3.3.4 NRZ to NRZI Encoder

After the transmit data stream is scrambled, the data must be NRZI encoded in order to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 unshielded twisted pair cable.

3.4 100BASE-X RECEIVER

The 100BASE-X receiver consists of several functional blocks which are required to recover and condition the 125 Mb/s receive data stream as specified by the IEEE 802.3u Standard. The 125 Mb/s receive data stream may originate from a twisted pair transceiver such as the DP83223 TWISTER in a 100BASE-TX application. Alternatively, the receive data stream may be generated by an optical receiver as in a 100BASE-FX application. The block diagram in *Figure 5* provides an overview of each functional block within the 100BASE-X receive section.

The Receiver block consists of the following functional blocks:

- Clock Recovery block
- NRZI to NRZ decoder block (bypass option)
- Descrambler block (bypass option)
- Symbol Alignment block (bypass option)
- 5B/4B Symbol Decoder block (bypass option)
- Collision Detect block
- Carrier Sense block
- Stream Decoder block
- 100 Mb/s Receive State Machine

The bypass option for each of the functional blocks within the 100BASE-X receiver provides flexibility for applications such as 100 Mb/s repeaters where data conversion is not always required.

3.4.1 Clock Recovery

The Clock Recovery Module (CRM) accepts 125 Mb/s scrambled NRZI data stream from an external PMD receiver (DP83223). The CRM locks onto the 125 Mb/s data stream and extracts a 125 MHz reference clock. The extracted and synchronized clock and data are used as required by the synchronous receive operations.

The CRM is implemented using an advanced digital Phase Locked Loop (PLL) architecture that replaces sensitive analog circuits. Using digital PLL circuitry allows the DP83840 to be manufactured and specified to tighter tolerances.

3.4.2 NRZI to NRZ

In a typical application the NRZI to NRZ decoder is required in order to present NRZ formatted data to the descrambler.

The receive data stream, as recovered by the PMD receiver, is in NRZI format, therefore the data must be decoded to NRZ before reaching the descrambler. With the receive data in NRZ format, the descrambler can properly synchronize to the scrambled data.

3.4.3 Descrambler

A 5-bit parallel (symbol wide) descrambler is used to descramble the receive NRZ data. To reverse the data scrambling process, the descrambler has to generate an identical data scrambling sequence (N) in order to recover the original unscrambled data (UD) from the scrambled data (SD) as represented in the equations:

$$SD = UD \oplus N \quad UD = SD \oplus N$$

Synchronization of the descrambler to the original scrambling sequence (N) is achieved based on the knowledge that the incoming scrambled data stream consists of scrambled IDLE data. After the descrambler has recognized sufficient IDLE symbols, where an IDLE symbol in 5B NRZ is equal to five consecutive ones (11111), it will synchronize to the receive data stream and generate unscrambled data in the form of unaligned 5B symbols.

In order to maintain synchronization, the descrambler must continuously monitor the validity of the unscrambled data that it generates. To ensure this, a line state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler the hold timer starts a 722 μs countdown. Upon detection of sufficient IDLE symbols within the 722 μs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the line state monitor does not recognize sufficient unscrambled IDLE symbols within the 722 μs period, the entire descrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.4.4 Symbol Alignment

The Symbol Alignment module operates on unaligned 5-bit data from the descrambler (if the descrambler is not bypassed) and converts it into 5B symbol data (5 bits). Symbol alignment occurs after the J/K symbol pair is detected. Once the J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.0 Functional Description (Continued)

TABLE II. 4B5B Symbol Encoding/Decoding

Symbol	5B Symbol Code	4B Nibble Code
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES		
H	00100	Halt Symbol—To be transmitted on TX_ER
I	11111	Inter Packet Idle Symbol—0000*
J	11000	First Start of Packet Symbol—0101*
K	10001	Second Start of Packet Symbol—0101*
T	01101	First End of Packet Symbol—0000*
R	00111	Second End of Packet Symbol—0000*
INVALID CODES		
V	00000	0110 or 0101**
V	00001	0110 or 0101**
V	00010	0110 or 0101**
V	00011	0110 or 0101**
V	00101	0110 or 0101**
V	00110	0110 or 0101**
V	01000	0110 or 0101**
V	01100	0110 or 0101**
V	10000	0110 or 0101**
V	11001	0110 or 0101**

*Control symbols I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

**Normally, invalid codes (V) are mapped to 6h on RXD[3:0] with RX_ER asserted. If the CODE_ERR bit in the LBREMR (bit 4, register address 18h) is set, the invalid codes are mapped to 5h on RXD[3:0] with RX_ER asserted.

3.0 Functional Description (Continued)

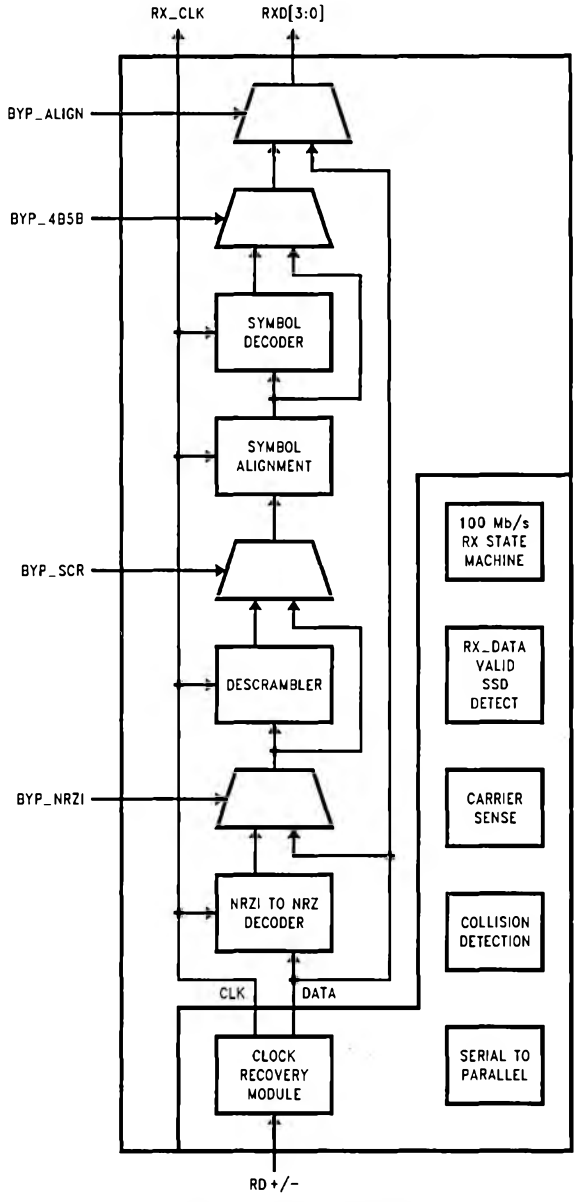

FIGURE 5. 100BASE-X Receiver

3.0 Functional Description (Continued)

3.4.5 Symbol Decoder

The Symbol Decoder functions as a look up table that translates incoming 5B symbols into 4B nibbles. The Symbol Decoder first detects the J/K symbol pair preceded by IDLE symbols and replaces the symbol with MAC preamble. Specifically, the J/K 10-bit symbol pair is replaced by the nibble pair 1010 1010. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the T/R symbol pair denoting the End of Stream Delimiter (ESD).

3.4.6 Collision Detect (Half Duplex)

Half Duplex collision detection for 100 Mb/s follows the model of 10BASE-T. Collision detection is indicated by the COL pin of the MII.

For Full Duplex applications the COL signal is never asserted.

3.4.7 Carrier Sense

Carrier Sense (CRS) is asserted upon the detection of two non-contiguous zeros occurring within any 10-bit boundary of the receive data stream.

The carrier sense function is independent of symbol alignment. For 100 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 100 Mb/s Full Duplex operation, CRS is asserted only during packet reception.

When the IDLE symbol pair is detected in the receive data stream, CRS is deasserted.

In REPEATER mode (pin 47/bit 12, register address 17h), CRS is only asserted due to receive activity.

3.4.8 100 Mb/s Receive State Machine

The DP83840 implements the 100BASE-X receive state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24.

3.5 CLOCK GENERATION MODULE

The Clock Generation Module (CGM) within the DP83840 can be configured for several different applications. This offers the flexibility of selecting a clocking scheme that is best suited for a given design.

This section describes the operation of the CGM from a device perspective as well as its applications within a system such as an adapter or repeater.

3.5.1 Device Requirements

For 100 Mb/s operation the DP83840 requires either a 50 MHz reference at the OSCIN pin or a 25 MHz reference at the REFIN pin.

If 10BASE-T operation and/or Auto-Negotiation functions are required, a 20 MHz reference is also required. This can be derived either internally from the 50 MHz reference or externally from a 20 MHz crystal or oscillator.

The DP83840 will accept various clock reference inputs. Each of these is described as follows.

3.5.1.1 Single 50 MHz Reference

A 50 MHz oscillator can be used to drive the OSCIN input. This reference is internally divided by two and then routed to the CLK25M output pin. By connecting the CLK25M output directly to the REFIN input pin, the 25 MHz reference is allowed to drive the 100 Mb/s module. The 50 MHz signal is also divided by 2.5 internally to provide the 20 MHz reference directly to the 10 Mb/s module. This option is shown in *Figure 6*. It should be noted that the ÷2.5 circuitry adds some jitter to the 10 Mb/s performance.

The 10BASE-T module within the DP83840 will automatically switch to the 20 MHz reference (sourced by the internal ÷2.5 circuit) upon detection of inactivity on the X1 input pin. When not in use, the X1 input pin should be tied to V_{CC} either directly or via a 4.7 kΩ pull-up resistor.

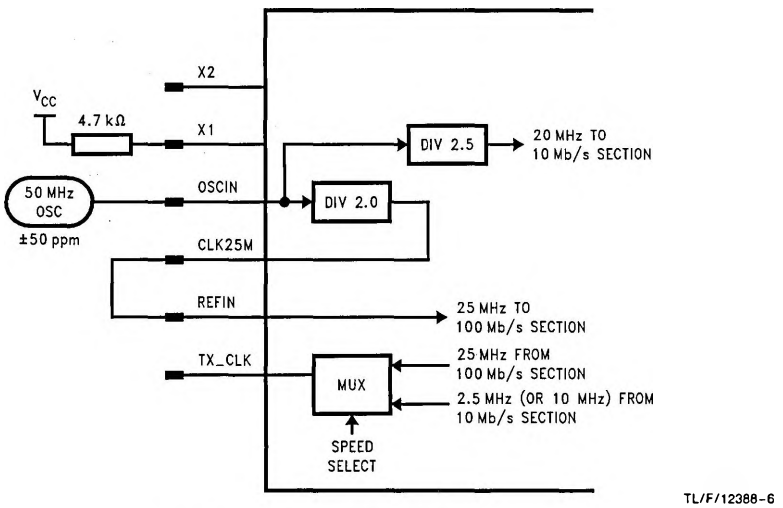

FIGURE 6. Single 50 MHz Reference

3.0 Functional Description (Continued)

3.5.1.2 50 MHz and 20 MHz Reference

For improved jitter performance in the 10 Mb/s module, an external 20 MHz oscillator can be used to drive the X1 pin. Alternatively, a 20 MHz crystal network can be connected across pins X1 and X2 to provide the required reference for the 10 Mb/s module. The 100 Mb/s module must still receive a 25 MHz reference which can be provided by a 50 MHz oscillator as described in 3.5.1.1. This option is shown in *Figure 7* (20 MHz oscillator module) and *Figure 8* (20 MHz crystal) below.

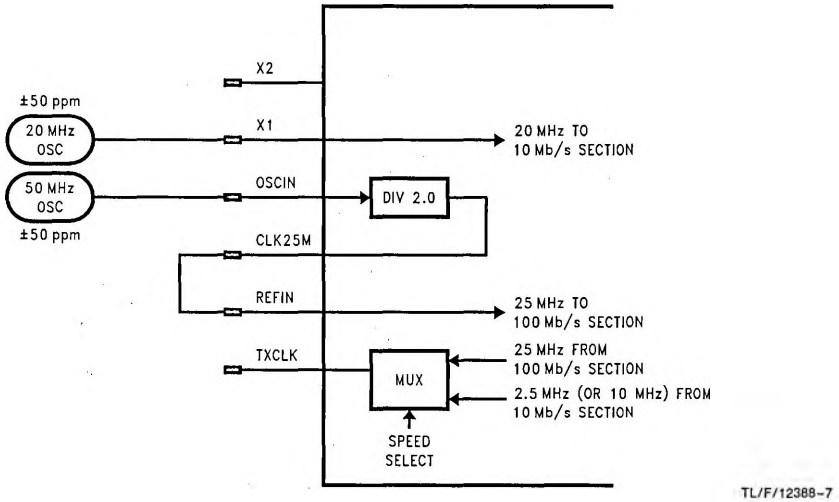

FIGURE 7. 50 MHz and 20 MHz Reference

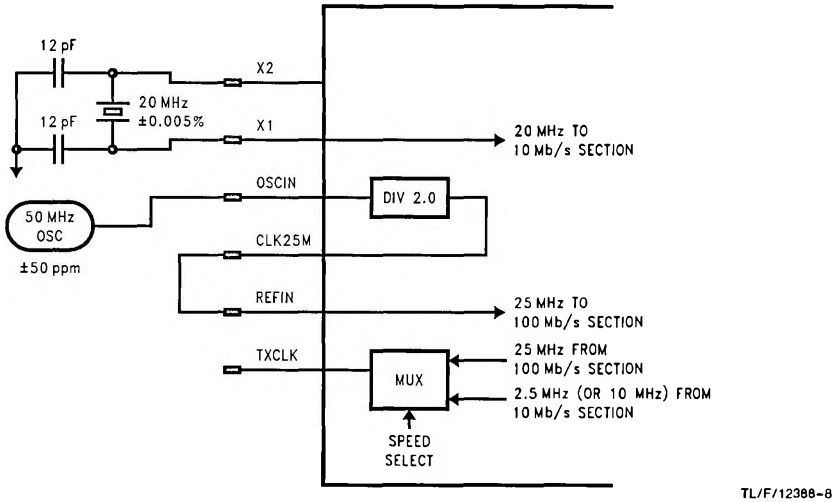

FIGURE 8. 50 MHz Reference and 20 MHz Crystal

3.0 Functional Description (Continued)

3.5.1.3 25 MHz and 20 MHz Reference

A 25 MHz reference, either from an oscillator or a system clock can directly drive the 100 Mb/s module via the REFIN input.

A separate 20 MHz reference from either an oscillator or a crystal network must be provided to the X1 and X2 inputs as described in 3.5.1.2. This option is shown in *Figure 9* below.

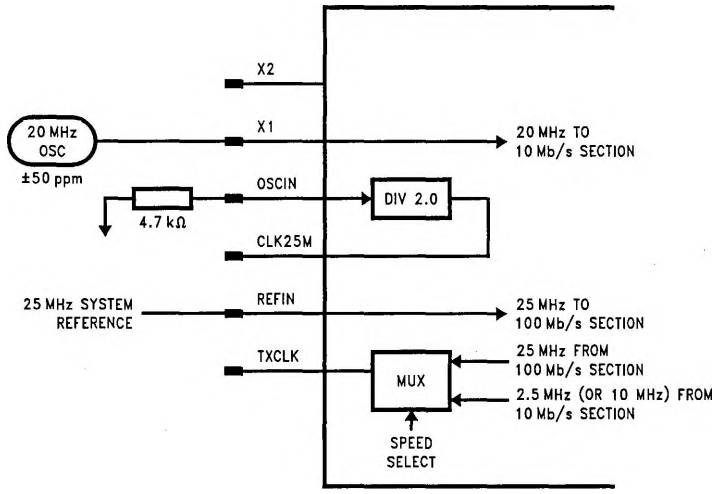

FIGURE 9. 25 MHz and 20 MHz Reference

3.0 Functional Description (Continued)

3.5.2 System Clocking

The DP83840 clock options help to simplify single port adapter designs as well as multi-port repeaters. The TX_CLK allows MII data to be received in either parallel or serial modes as described in Section 3.1.3. The standard MII interface clock rate options are as follows:

TX_CLK = 25 MHz for 100 Mb/s nibble mode

TX_CLK = 2.5 MHz for 10 Mb/s nibble mode

Additionally, the DP83840 provides:

TX_CLK = 10 MHz for 10 Mb/s serial mode

3.5.2.1 Adapter Clock Distribution Example

In most single port adapter applications, where only one DP83840 is required, providing a single 50 MHz oscillator reference is sufficient for deriving the required MAC and PHY layer clocks. Based on the 50 MHz reference, the DP83840 can generate its own internal 20 MHz reference for the 10 Mb/s module. Additionally, the DP83840 can generate the required 25 MHz reference for its 100 Mb/s module.

During 100 Mb/s operation the 25 MHz reference generated by the DP83840 is available at the TX_CLK output pin. This can be used for synchronization with the MAC layer device. During 10 Mb/s operation the TX_CLK pin sources either a 2.5 MHz or 10 MHz reference to the MAC layer device. *Figure 10* provides an example of the clock distribution in a typical node design based on the DP83840.

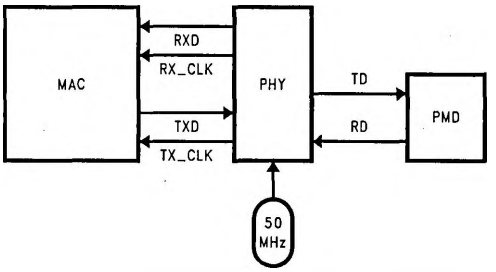

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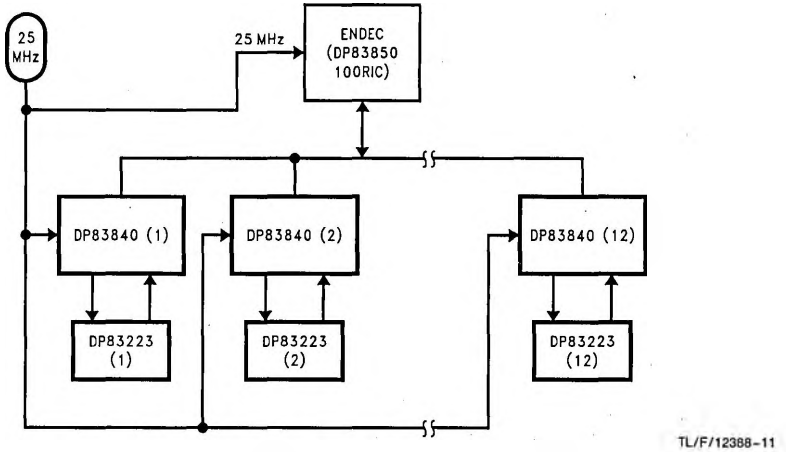
FIGURE 10. Typical Adapter Clock and Data Interconnections

3.5.2.2 Repeater Clock Distribution Example

The clock distribution within a multi-port repeater can be designed in a variety of ways. *Figure 11* provides a simplified example of a timing distribution scheme in a 100 Mb/s only repeater design. It should be noted that in order to support Auto-Negotiation, a 20 MHz reference would be required for each DP83840 device. Due to the demanding timing constraints required to maintain standards compliance, great care must be taken in the design and layout of a multi-port repeater system. The example provided in *Figure 11* illustrates interconnection only and should not be considered as a final working design.



TL/F/12388–11

FIGURE 11. Typical 100 Mb/s Repeater Clock Interconnection

3.0 Functional Description (Continued)

3.6 CLOCK RECOVERY MODULE

The Clock Recovery Module (CRM) is part of the 100 Mb/s receive channel. The 10 Mb/s clock recovery is independent from the CRM.

The CRM contains a Phase Locked Loop that tracks the signal frequency of the incoming 125 Mb/s data stream at the RD+/− inputs. The CRM extracts a synchronous 125 MHz clock from this data (the data rate on the cable is 125 Mb/s due to 4B5B encoding). The CRM obtains its initial frequency and stability from its own internal VCO and then adjusts the frequency as required to match the incoming data stream frequency. The CRM maintains control of the PLL's loop gain to minimize the lock time as well as to minimize the jitter after phase lock has been acquired.

When the Signal Detect (SD+/−) inputs become active, the CRM attempts to acquire lock. The CRM loses lock when the SD+/− inputs become de-asserted.

The CRM generates a 125 MHz clock synchronous with the receive data stream and presents both the clock and data to the rest of the 100 Mb/s receive section. The CRM is not synchronous with the local clock present at the REFIN input to the CGM.

The RX_CLK signal at the MII interface is derived from the CRM 125 Mb/s clock during 100 Mb/s operation. The RX_CLK frequency is set to 25 MHz for nibble-wide receive data passing to the MAC and/or ENDEC.

3.7 10BASE-T TRANSCEIVER MODULE

The 10BASE-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard. An external filter is not required on the 10BASE-T interface since this is integrated inside the DP83840.

3.7.1 Operational Modes

The DP83840 has 2 basic 10 Mb/s operational modes:

— Half Duplex mode

— Full Duplex mode

3.7.1.1 Half Duplex Mode

In Half Duplex mode the DP83840 functions as a standard IEEE 802.3 10BASE-T transceiver with fully integrated filtering.

3.7.1.2 Full Duplex Mode

In Full Duplex mode the DP83840 is capable of simultaneously transmitting and receiving without asserting the collision signal. The DP83840's 10 Mb/s ENDEC is designed to encode and decode simultaneously.

3.7.2 Smart Squelch

The Smart Squelch is responsible for determining when valid data is present on the differential receive inputs (RXI±). The DP83840 implements an intelligent receive squelch on the RXI± differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. Smart squelch operation is independent of the 10BASE-T operational mode.

The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-T standard) to determine the validity of data on the twisted pair inputs.

The receive squelch threshold level can be lowered for use in longer cable or STP applications. This is achieved by setting the LSS bit in the 10BTCR (bit 2, register address 1Ch).

3.7.3 Collision Detection

For Half Duplex, a 10BASE-T collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

If the ENDEC is transmitting when a collision is detected, the collision is not reported until seven bits have been received while in the collision state. This prevents a collision being reported incorrectly due to noise on the network. The COL signal remains set for the duration of the collision.

When heartbeat is enabled, approximately 1 μs after the transmission of each packet a Signal Quality Error (SQE) signal of approximately 10 bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

3.7.4 Link Pulse Detection/Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-T standard. Each link pulse is nominally 100 ns in duration and is transmitted every 16 ms ± 8 ms, in the absence of transmit data.

Link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10BASE-T twisted pair transmitter, receiver and collision detection functions.

When the link integrity function is disabled, the 10BASE-T transceiver will operate regardless of the presence of link pulses.

In 10 Mb/s ENDEC loopback mode (bit 11, register address 18h), transmission and reception paths can be tested regardless of the incoming link status.

3.7.5 Jabber Function

The Jabber function monitors the DP83840's output and disables the transmitter if it attempts to transmit a longer than legal sized packet. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than approximately 26 ms.

Once disabled by the Jabber function, the transmitter stays disabled for the entire time that the ENDEC module's internal transmit enable is asserted. This signal has to be de-asserted for approximately 750 ms (the "unjab" time) before the Jabber function re-enables the transmit outputs.

3.7.6 Transmit Outputs

There are two pairs of 10BASE-T output signals. One pair for UTP cable (TXU+/−) and one pair for STP cable (TXS+/−).

Selection between 100Ω UTP and 150Ω STP cable operation is accomplished using the UTP/STP bit in the 10BASE-T Configuration Register (bit 3, register address 1Ch). Only one set of outputs is active at a time. Selecting UTP will TRI-STATE STP and vice versa.

The TXU+/− and TXS+/− outputs of the DP83840 are internally filtered and require no additional external filtering. See Section 3.7.11 for more details.

3.7.7 Status Information

10BASE-T Status Information is available on the LED output pins of the DP83840. Transmit activity, receive activity, link

3.0 Functional Description (Continued)

status, link polarity and collision activity information is output to the five LED output pins ($\overline{LED1}$ to $\overline{LED5}$). See Section 2.6 for more information on these outputs.

If required the LED outputs can be used to provide digital status information to external circuitry.

The Link LED output ($\overline{LED3}$, pin #38) indicates Good Link status for both 10 and 100 Mb/s modes. In Half Duplex 10BASE-T mode, $\overline{LED3}$ indicates link status.

The link integrity function can be disabled. When disabled, the transceiver will operate regardless of the presence of link pulses and the Link LED will stay lit continuously.

3.7.8 Automatic Link Polarity Detection

The DP83840's 10BASE-T Transceiver Module incorporates an automatic link polarity detection circuit. When seven consecutive link pulses or three consecutive receive packets with inverted End-of-Packet pulses are received, bad polarity is reported.

A polarity reversal can be caused by a wiring error at either end of the UTP/STP cable, usually at the Main Distribution Frame (MDF) or patch panel in the wiring closet.

The bad polarity condition is latched and the $\overline{LED4}$ output is asserted. The DP83840's 10BASE-T Transceiver Module corrects for this error internally and will continue to decode received data correctly. This eliminates the need to correct the wiring error immediately.

3.7.9 10BASE-T Internal Loopback

When the 10BT_LPBK bit in the LBREMR (bit 11, register address 18h) is set, 10BASE-T transmit data is looped back in the ENDEC to the receive channel. The transmit drivers and receive input circuitry are disabled in transceiver loopback mode, isolating the transceiver from the network.

Loopback is used for diagnostic testing of the data path through the transceiver without transmitting on the network or being interrupted by receive traffic.

3.7.10 Transmit and Receive Filtering

External 10BASE-T filters are not required when using the DP83840 as the required signal conditioning is integrated.

Only isolation/step-up transformers and impedance matching resistors are required for the 10BASE-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30 dB.

3.7.11 Typical Node Application

An example of the 10BASE-T interface is shown in *Figure 12*. The TXS+/− signals are used for STP and the TXU+/− signals for UTP. Standard UTP applications do not require connection of the TXS+/− outputs. The output resistor values are chosen to match the transmit output impedance to the impedance of the twisted pair cable.

The DP83840 10BASE-T outputs require a 1:2 step-up isolation transformer in order to match the cable impedance. The 10BASE-T inputs require a 1:1 isolation transformer and appropriate line termination. Refer to *Figure 12*.

3.8 IEEE 1149.1 CONTROLLER

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits.

The standard provide a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques. It also provides a means of accessing and controlling design-for-test features built into the digital integrated circuits. Such features include internal scan paths and self-test functions as well as other features intended to support service applications in the assembled product. The IEEE 1149.1 Boundary Scan Architecture document should be referenced for additional detail.

The circuitry defined by this standard allows test instructions and associated data to be input serially into a device. The instruction execution results are output serially.

The DP83840 reserves five pins, called the Test Access Port (TAP), to provide test access: TMS, TCK, Test Data Input (TDI), Test Data Output (TDO) and Test Reset (TRST). These signals are described in Section 2.7. To ensure race-free operation all input and output data is synchronous to the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK while output signal (TDO) is clocked on the falling edge.

3.8.1 Test Logic

The IEEE 1149.1 Test Logic consists of a Test Access Port (TAP) controller, an instruction register, and a group of test data registers including Bypass, Device Identification and Boundary Scan registers.

The TAP controller is a synchronous 16 state machine that responds to changes at the TMS and TCK signals.

This controls the sequence of operations by generating clock and control signals to the instruction and test data registers. The control signals switch TDI and TDO between instruction and test data registers.

The DP83840 implements 4 basic instructions: ID_Code, bypass, Sample/Preload and Extest. Upon reset, the ID_Code instruction is selected by default. If the ID_Code instruction is not supported, the bypass instruction is selected instead.

3.8.1.1 ID_Code Instruction

The ID_Code instruction allows users to select the 32-bit IDCODE register and interrogate the contents which consist of the manufacturer's ID, part ID and the version number.

3.8.1.2 Bypass Instruction

The bypass instruction uses the bypass register. The bypass register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the DP83840 when test operation is not required. This allows more rapid movement of test data to and from other testable devices in the system.

3.8.1.3 Sample/Preload Instruction

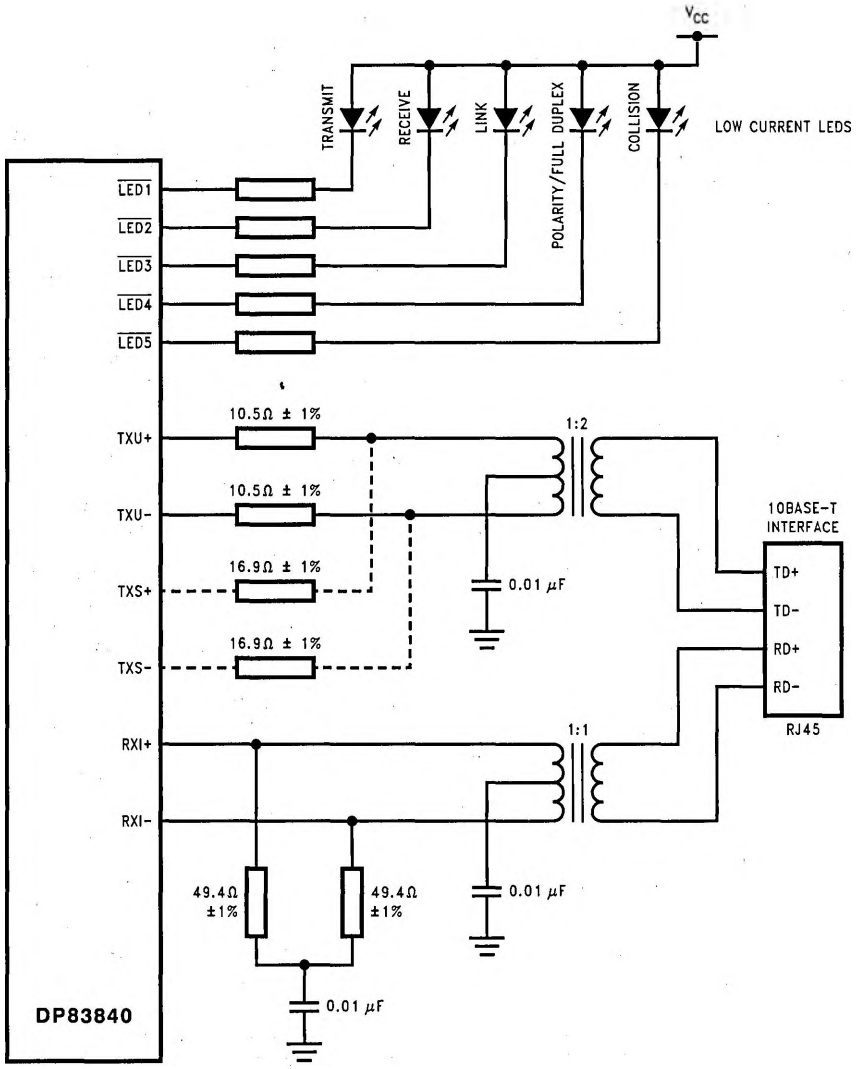
The Sample/Preload instruction allows scanning of the boundary-scan register without causing interference to the normal operation of the on-chip system logic.

Two functions are performed when this instruction is selected.

3.0 Functional Description (Continued)

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload allows an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells which are connected to system output pins. This ensures that known data is driven through the system output pins upon entering the Extest instruction.



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Note: Resistors from TXS+/− outputs can be added if STP cable support is required.

FIGURE 12. Typical 10BASE-T (UTP) Node Application

3.0 Functional Description (Continued)

Without Preload, indeterminate data would be driven until the first scan sequence has been completed. The shifting of data for the Sample and Preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

3.8.1.4 Extest Instruction

The Extest instruction allows circuitry external to the DP83840 (typically the board interconnections) to be tested.

Prior to executing the Extest instruction, the first test stimulus to be applied will be shifted into the boundary-scan registers using the Sample/Preload instruction. Thus, when the change to the Extest instruction takes place, known data will be driven immediately from the DP83840 to its external connections.

This provides stimulus to the system input pins of adjacent devices on the assembled printed circuit boards. *Figure 13* below illustrates the IEEE 1149.1 architecture.

3.8.2 Device Testing

IEEE 1149.1 provides a simple solution for testing many of the standard static pin parametrics. Reasonably accurate limits may be tested as a functional pattern.

The IEEE 1149.1 test circuitry is tested itself as a consequence of testing pin parametrics. Specific tests are:

- TRI-STATE conditions of TDO when serial shift between TDI and TDO is not selected
- Input leakage of TCK, TMS, TDI and TRST
- Output has TRI-STATE leakage of TDO
- Opens and shorts of TCK, TMS, TDI, TRST, and TDO
- IDCODE register, the bypass register and the TAP controller state machine sequences

Open and shorted pins can be identified by placing an alternating bit pattern on the I/O pins. Any shorted bond wires would either cause an input to be misinterpreted in the inputs scan phase, or the test comparator would fail an output during data scan.

Repeating the test with the inverse bit pattern provides coverage of V_{CC} and GND short/open circuits.

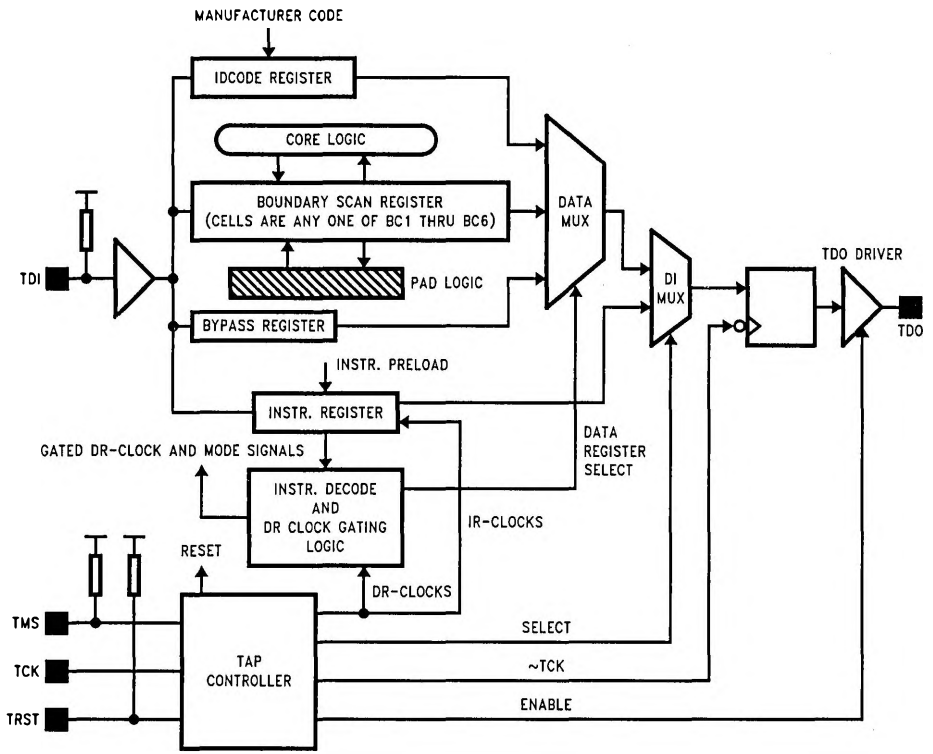

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FIGURE 13. IEEE 1149.1 Architecture

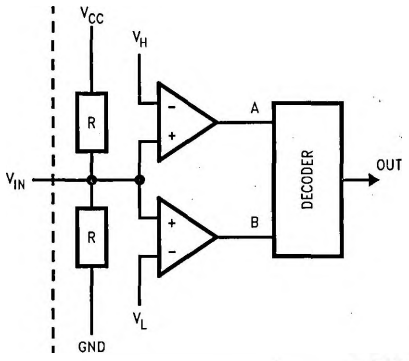
3.0 Functional Description (Continued)

3.9 IEEE 802.3u AUTO-NEGOTIATION

The Auto-Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulses (FLP) Bursts provide the signaling used to communicate Auto-Negotiation abilities between two devices at each end of a link segment. For further detail regarding Auto-Negotiation, refer to clause 28 of the IEEE 802.3u specification. The DP83840 supports four different Ethernet protocols, so the inclusion of Auto-Negotiation ensures that the highest performance protocol will be selected based on the ability of the Link Partner. The Auto-Negotiation function within the DP83840 can be controlled either by internal register access or by use of the AN1 and AN0 (pins 46 and 95).

3.9.1 Auto-Negotiation Pin Control

The state of AN0 and AN1 determines whether the DP83840 is forced into a specific mode or Auto-Negotiation will advertise a specific ability or set of abilities as given in Table III. Pins AN0 and AN1 are implemented as tri-level control pins which are configured by connecting them to V_{CC}, GND or by leaving them unconnected (refer to *Figure 14*). The state of AN0 and AN1 determines the Auto-Negotiation mode upon power-up/reset. This state is not reflected in the BMCR. The Auto-Negotiation function selected at power-up/reset can be changed at any time by writing to the Basic Mode Command Register (BMCR) at address 00h.



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V_{IN}	A	B	OUT
0V	L	L	L
$V_{CC} \div 2$	L	H	M
V_{CC}	H	H	H

FIGURE 14. Tri-Level Pin Control

3.9.2 Auto-Negotiation Register Control

When Auto-Negotiation is enabled, the DP83840 transmits the abilities programmed into the Auto-Negotiation Advertisement Register (ANAR) at address 04h via FLP Bursts. Any combination of 10 Mb/s, 100 Mb/s, Half-Duplex, and Full-Duplex modes may be selected. The DP83840 will advertise all available abilities by default. Auto-Negotiation controls the exchange of configuration information. Upon successful Auto-Negotiation, the abilities reported by the Link Partner are stored in the Auto-Negotiation Link Partner Ability Register (ANLPAR) at address 05h.

The contents of the ANLPAR register are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by Auto-Negotiation by comparing the contents of the ANAR and ANLPAR registers and then selecting the technology whose bit is set in both the ANAR and ANLPAR of highest priority relative to the following list.

Auto-Negotiation Priority Resolution:

1. 100BASE-TX Full Duplex (Highest Priority)
2. 100BASE-T4
3. 100BASE-TX Half Duplex
4. 10BASE-T Full Duplex
5. 10BASE-T Half Duplex (Lowest Priority)

The Basic Mode Control Register (BMCR) at address 00h provides control of enabling, disabling, and restarting of the Auto-Negotiation function. When Auto-Negotiation is disabled the Speed Selection bit in the BCMR (bit 13, register address 00h) controls switching between 10 Mb/s or 100 Mb/s operation, while the Duplex Mode bit (bit 8, register address 00h) controls switching between full duplex operation and half duplex operation. The Speed Selection and Duplex Mode bits have no effect on the mode of operation when the Auto-Negotiation Enable bit (bit 12, register address 00h) is set.

The Basic Mode Status Register (BMSR) at address 01h indicates the set of available abilities for technology types (bits 15 to 11, register address 01h), Auto-Negotiation ability (bit 3, register address 01h), and Extended Register Capability (bit 0, register address 01h). These bits are permanently set to indicate the full functionality of the DP83840 (only the 100BASE-T4 bit is not set since the DP83840 does not support that function, while it does support all the other functions).

The BMSR also provides status on:

1. Whether Auto-Negotiation is complete (bit 5, register address 01h)
2. Whether the Link Partner is advertising that a remote fault has occurred (bit 4, register address 01h)
3. Whether a valid link has been established (bit 2, register address 01h)

The Auto-Negotiation Advertisement Register (ANAR) at address 04h indicates the Auto-Negotiation abilities to be advertised by the DP83840. All available abilities are transmitted by default, but any ability can be suppressed by writing to the ANAR. Updating the ANAR to suppress an ability is one way for a management agent to change (force) the technology that is used.

The Auto-Negotiation Link Partner Ability Register (ANLPAR) at address 05h indicates the abilities of the Link Partner as indicated by Auto-Negotiation communication. The contents of this register are considered valid when the Auto-Negotiation Complete bit (bit 5, register address 01h) is set.

3.0 Functional Description (Continued)

TABLE III. Auto-Negotiation Mode Select

AN1 (Pin 46)	AN0 (Pin 95)	Action	Mode
FORCED MODES			
0	M	BMCR (00h) Bit 12 = 0, Bit 13 = 0, Bit 8 = 0 ANAR (04h) Bits 5 to 8 Set to Default Values	Auto-Negotiation Disabled with Only Half-Duplex 10BASE-T Forced
1	M	BMCR (00h) Bit 12 = 0, Bit 13 = 0, Bit 8 = 1 ANAR (04h) Bits 5 to 8 Set to Default Values	Auto-Negotiation disabled with Only Full-Duplex 10BASE-T Forced
M	0	BMCR (00h) Bit 12 = 0, Bit 13 = 1, Bit 8 = 0 ANAR (04h) Bits 5 to 8 Set to Default Values	Auto-Negotiation disabled with Only Half-Duplex 100BASE-X Forced
M	1	BMCR (00h) Bit 12 = 0, Bit 13 = 1, Bit 8 = 1 ANAR (04h) Bits 5 to 8 Set to Default Values	Auto-Negotiation disabled with Only Full-Duplex 100BASE-X Forced
ADVERTISED MODES			
M	M	BMCR (00h) Bit 12 = 1 ANAR (04h) Bits 5 to 8 = 1	Auto-Negotiation Enabled for All Possible Protocols (Half or Full Duplex for 10BASE-T or 100BASE-X)
0	0	BMCR (00h) Bit 12 = 1 ANAR (04h) Bit 5 = 1, Bits 6 to 8 = 0	Auto-Negotiation Enabled with Only Half-Duplex 10BASE-T Available
0	1	BMCR (00h) Bit 12 = 1 ANAR (04h) Bit 5 = 0, Bit 6 = 1, Bits 7 and 8 = 0	Auto-Negotiation Enabled with Only Full-Duplex 10BASE-T Available
1	0	BMCR (00h) Bit 12 = 1 ANAR (04h) Bit 5 and 6 = 0, Bit 7 = 1, Bit 8 = 0	Auto-Negotiation Enabled with Only Half-Duplex 100BASE-X Available
1	1	BMCR (00h) Bit 12 = 1 ANAR (04h) Bit 5 to 7 = 0, Bit 8 = 1	Auto-Negotiation Enabled with Only Full-Duplex 100BASE-X Available

"M" indicates logic mid level ($V_{CC} \div 2$) "1" indicates logic high level "0" indicates logic low level

The Auto-Negotiation Expansion Register (ANER) at address 06h indicates additional Auto-Negotiation status. The ANER provides status on:

1. Whether a Multiple Link Fault has occurred (bit 4, register address 06h)
2. Whether the Link Partner supports the Next Page function (bit 3, register address 06h)
3. Whether the DP83840 supports the Next Page function (bit 2, register address 06h). The DP83840 does not support the Next Page function.
4. Whether the current page being exchanged by Auto-Negotiation has been received (bit1, register address 06h)
5. Whether the Link Partner supports Auto-Negotiation (bit 0, register address 06h)

3.9.3 Auto-Negotiation Parallel Detection

The DP83840 in conjunction with the DP83223 transceiver supports the Parallel Detection function as defined in the IEEE 802.3u specification. Parallel Detection requires both the 10 Mb/s and 100 Mb/s receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation, yet is transmitting link signals that the 100BASE-TX or 10BASE-T PMAs recognize as valid link signals. In the event that more than one PMA indicates a valid link, the Multiple Link Fault bit (bit 4, register address 06h) will be set.

As an example, when the Link Partner supports 100BASE-TX but does not support Auto-Negotiation, Parallel Detection will allow the DP83840 to negotiate to 100 Mb/s operation by detecting a valid set of IDLEs even though no Link Code Words were exchanged through FLP Bursts.

3.0 Functional Description (Continued)

3.10 RESET OPERATION

The DP83840 can be reset either by hardware or software. A hardware reset may be accomplished either by asserting the RESET pin (pin 44) during normal operation, or upon powering up the device. A software reset is accomplished by setting the reset bit in the Basic Mode Control Register (bit 15, address 00h).

3.10.1 Power-Up Reset

When V_{CC} is first applied to the DP83840 it takes some amount of time for power to actually reach the nominal 5V potential. This initial power-up time can be referred to as a V_{CC} ramp when V_{CC} is "ramping" from 0V to 5V. When the initial V_{CC} ramp reaches approximately 4V, the DP83840 begins an internal reset operation which must be allowed sufficient time, relative to the assertion and deassertion of the RESET pin, to reset the device. There are two methods for guaranteeing successful reset upon device power-up.

The first method accounts for those designs that utilize a special power up circuit which, through hardware, will assert the RESET pin upon power-up. In this case, the deassertion (falling edge) of the RESET pin must not occur until at least 500 μs after the time at which the V_{CC} ramp initially reached the 4V point.

The second method accounts for those applications which produce a reset pulse sometime after the initial power-up of the device. In this case, it is recommended that a positive pulse, with a duration of at least 1 μs, be applied to the RESET pin no sooner than 500 μs after the point in time where the initial V_{CC} ramp reached 4V.

In both methods described above, it is important to note that the logic levels present at each of the hardware configuration pins of the DP83840 (see list below) are also latched into the device as a function of the reset operation. These hardware configuration values are guaranteed to be latched into the DP83840 2 μs after the deassertion of the RESET pin.

The hardware configuration values latched into the DP83840 during the reset operation are dependent on the logic levels present at the following device pins upon power-up:

Pin #	Primary Function	Latched In at Reset
49	LBEN	PHYAD[0]
53	ENCSEL	PHYAD[1]
66	CRS	PHYAD[2]
89	PHYAD[3]	PHYAD[3]
63	RX_ER	PHYAD[4]
95	AN0	AN0
46	AN1	AN1
47	REPEATER	REPEATER
98	10BTSER	10BTSER
99	BPALIGN	BPALIGN
100	BP4B5B	BP4B5B
1	BPSCR	BPSCR

During the power-up reset operation the $\overline{\text{LED1}}$ through $\overline{\text{LED5}}$ pins are undefined and the SPEED_10 pin will be asserted.

3.10.2 Hardware Reset

A hardware Reset is accomplished by applying a positive pulse, with a duration of at least 1 μs, to the RESET pin of the DP83840 during normal operation. This will reset the device such that all registers will be reset to default values and the hardware configuration values will be re-latched into the device (similar to the Power-Up reset operation).

3.10.3 Software Reset

A software reset is accomplished by setting bit 15 of the Basic Mode Control Register (address 00h). This bit is self clearing and, when set, will return a value of "1" until the software reset operation has completed. The software reset will only force the register bits with a given default state to that default state. Hardware configuration values will not be latched into the device as a result of a software reset.

3.11 LOOPBACK OPERATION

The DP83840 supports several different modes of loopback operation for diagnostic purposes.

3.11.1 10BASE-T Loopback

The loopback options for 10BASE-T operation can be selected either by asserting the Loopback bit (bit 14) in the Basic Mode Control Register (address 00h), or by asserting the 10BT_LPBK bit (bit 11) in the Loopback, Bypass and Receiver Error Mask Register (address 18h). Asserting either of these bits will cause the 10BASE-T data present at the transmit MII data inputs to be routed back to the receive MII data outputs. During this loopback mode, the Manchester encoded 10BASE-T data will not be present at either the TXU+/− or TXS+/− serial differential outputs.

Normal 10BASE-T operation, in order to be standard compliant, also loops back the MII transmit data to the MII receive data. However, the data is also allowed to be passed through the 10BASE-T transmitter and out either the TXU+/− or TXS+/− outputs as well.

3.11.2 100BASE-X Loopback

The loopback options for 100BASE-X operation can be selected by asserting the Loopback bit (bit 14) in the Basic Mode Control Register (address 00h), or by selecting the desired mode as determined by the LB[1:0] (bits 8 and 9) in the Loopback, Bypass and Receiver Error Mask Register (address 18h).

Asserting the Loopback bit (bit 14) in the Basic Mode Control Register (address 00h) will cause the same loopback of MII transmit to MII receive as described previously in the 10BASE-T loopback section, except at 25 MHz due to 100BASE-X operation.

The LB[1:0] bits (bits 8 and 9) of the LBREMR (address 18h) allow for three different modes of operation:

1. bit 8 = 0, bit 9 = 0; Normal operation without loopback
2. bit 8 = 0, bit 9 = 1; PMD loopback operation
3. bit 8 = 1, bit 9 = 0; Remote Loopback

3.0 Functional Description (Continued)

The first mode allows normal operation without any form of loopback.

The second mode asserts the LBEN output of the DP83840 which, when connected to the LBEN input of the twisted pair transceiver (DP83223A), forces the twisted pair transceiver into loopback mode. Therefore, when the DP83840 is transmitting 100BASE-X serial data from its serial TD+/− outputs to the twisted pair transceiver, this data is immediately routed back to the RD+/− 100BASE-X serial inputs of the DP83840 device.

The third mode selects the Remote Loopback operation. In this mode, the DP83840 device serves as a "remote loopback" for the far end partner. Serial data received off the twisted pair cable is routed, via the DP83223A, into the RD+/− serial inputs of the DP83840 where it is then routed back to the TD+/− serial outputs of the DP83840 and finally launched back onto the twisted pair cable, via the DP83223A, and sent back to the far-end partner.

In each of the 100BASE-X loopback modes, except for Remote Loopback, the assertion of the loopback function will result in a 330 μs down-time where the 100BASE-TX descrambler must reacquire synchronization with the scrambled data stream before any valid data will appear at the receive MII RXD[3:0] outputs.

3.12 ALTERNATIVE 100BASE-X OPERATION

The DP83840 10/100 Physical Layer device supports one standard and three alternative modes when operating at 100 Mb/s.

3.12.1 Translational (normal) Mode

The first mode is referred to as the "Translational" mode. This is the standard and most commonly used operating mode where all transmit and receive functions are enabled in order to condition the data as it flows through the Physical Layer between the MAC and cable. All of the transmit and receive blocks as depicted in *Figures 4* and *5* are enabled (not bypassed).

3.12.2 Transparent Mode

The second mode is referred to as "Transparent". In this mode, the 4B/5B translators in both the transmit and receive sections are bypassed as might be required in certain repeater applications. This is accomplished either by configuring the BP4B5B pin (100) of the DP83840 to a logic high level prior to power-up/hardware reset or by setting the BP_4B5B bit (bit 14) of the LBREMR register (address 18h).

In "Transparent" mode, all remaining functional blocks within the 100BASE-X transmit and receive sections are still operational. This allows the 5B serial symbol on the twisted pair to be presented as descrambled data, without conversion to 4B, to the MII. Since the MII normally only carries a nibble wide word, the fifth bit, which is the new MSB, is carried on the RX_ER and TX_ER signals for receive and transmit operations respectively.

In the "Transparent" mode, all of the clock to data timing for both MII transmit and MII receive operations remains the same as in "Translational" mode. However, upon reception of a packet, the /J/K/ start of stream delimiter is not replaced by the /5/5/ MAC preamble nor is the /T/R/ end of stream delimiter removed from the packet before presentation to the MII receive RXD[3:0] and RX_ER outputs. Similarly, the transmit MII data TXD[3:0] and TX_ER must already have /J/K/ and /T/R/ packet delimiters in place. Therefore, the repeater controller device is responsible for receiving the packet delimiters intact as well as transmitting these delimiters intact back to the DP83840 device(s).

The receive data valid flag, RX_DV, operates the same during "Transparent" mode as it does in "Translational" mode. Additionally, Idles are passed to and from the MII as /00000/.

Finally, the "Transparent" mode of operation will operate the same when the DP83840 is in either node mode or repeater mode with the only difference being CRS functionality. As in "translational" mode, if the DP83840 is configured for repeater operation, the CRS signal will be suppressed during transmit such that only actual network collisions will be flagged.

3.12.3 Phaser Mode

The final mode of operation at 100 Mb/s is referred to as the "Phaser" mode. This mode might be used for those applications where the system design requires only the clock recovery and clock generation functions of the DP83840. This is accomplished either by configuring the BPALIGN pin (99) of the DP83840 to a logic high level prior to power-up/hardware reset or by setting the BP_ALIGN bit (bit 12) of the LBREMR register (address 18h).

In "Phaser" mode, all of the conditioning blocks in the transmit and receive sections of the 100BASE-X section are bypassed (refer to *Figures 4* and *5*). Therefore, whatever 5B data is presented to the MII transmit inputs (TXD[3:0] and TX_ER) of the DP83840 is simply serialized and output to the DP83223A twisted pair transceiver to be sent out over the twisted pair cable. Similarly, the 100BASE-X serial data received at the RD+/− inputs of the DP83840 are shifted into 5-bit parallel words and presented to the MII receive outputs RXD[3:0] and RX_ER. All data, including Idles, passes through the DP83840 unaltered other than for serial/parallel conversions.

In the "Phaser" mode, all of the clock to data timing for both MII transmit and MII receive operations remains the same as in "Translational" mode. Additionally, the "Phaser" mode will operate the same when the DP83840 is in either node mode or repeater mode with the only difference being CRS functionality. As in "translational" mode, if the DP83840 is configured for repeater operation, the CRS signal will be suppressed during transmit such that only actual network collisions will be flagged.

3.12.4 100BASE-FX Mode

The DP83840 will allow 100BASE-FX functionality by bypassing the scrambler and descrambler. This can be accomplished either through hardware configuration or via software.

The hardware configuration is set simply by tying the BPSCR pin (1) high with a 4.7 kΩ resistor and then cycling power or resetting the DP83840. The software setting is accomplished by setting the BP_SCR bit (bit 13) of the LBREMR register (address 18h) via MII serial management.

It is important to bypass the disconnect function during 100BASE-FX operation by setting the F_CONNECT bit (bit 5) in the PGR register (address 17h).

4.0 Registers

The MII supports up to 32 word-wide registers per addressable connected device. The DP83840's register allocation is as shown below. Each register is described in the Sections 4.2 to 4.17 that follow. Section 3.2 describes the MII serial access control method.

Address	Register Name	Description
00h	BMCR	Basic Mode Control Register
01h	BMSR	Basic Mode Status Register
02h	PHYIDR1	PHY Identifier Register #1
03h	PHYIDR2	PHY Identifier Register #2
04h	ANAR	Auto-Negotiation Advertisement Register
05h	ANLPAR	Auto-Negotiation Link Partner Ability Register
06h	ANER	Auto-Negotiation Expansion Register
7h–Fh	Reserved	Reserved for Future Assignments by the MII Working Group
10h–11h	Reserved	Reserved for PHY Specific Future Assignments by Vendor
12h	DCR	Disconnect Counter Register
13h	FCSCR	False Carrier Sense Counter Register
14h	Reserved	Reserved—Do Not Read/Write to this Register
15h	RECR	Receive Error Counter Register
16h	SRR	Silicon Revision Register
17h	PCR	PCS Sub-Layer Configuration Register
18h	LBREMR	Loopback, Bypass and Receiver Error Mask Register
19h	PAR	PHY Address Register
1Ah	Reserved	Reserved for PHY Specific Future Assignment by Vendor
1Bh	10BTSR	10BASE-T Status Register
1Ch	10BTCR	10BASE-T Configuration Register
1Dh–1Fh	Reserved	Reserved for Future Use—Do Not Read/Write to These Registers

4.1 KEY TO DEFAULTS

In the register descriptions that follow, the default column takes the form:

<reset value>, <access type> / <attribute(s)>

Where:

<reset value>:

1	Bit Set to Logic One
0	Bit Set to Logic Zero
X	No Default Value
(Pin #)	Value Latched in from Pin # at Reset

<access type>:

RO = Read Only
RW = Read/Write

<attribute(s)>:

L = Latching
SC = Self Clearing
P = Value Permanently Set

4.0 Registers (Continued)

4.2 BASIC MODE CONTROL REGISTER (BMCR)

Address 00h

Bit	Bit Name	Default	Description
15	Reset	0, RW/SC	**RESET:** 1 = Software Reset 0 = Normal Operation This bit sets the status and control registers of the PHY to their default states. This bit, which is self-clearing, returns a value of one until the reset process is complete.
14	Loopback	0, RW	**LOOPBACK:** 1 = Loopback Enabled 0 = Normal Operation The loopback function enables MII transmit data to be routed to the MII receive data path. Setting this bit may cause the descrambler to lose synchronization and produce a 330 μs "dead time" before any valid data will appear at the MII receive outputs. This bit takes priority over the loopback control bits 8 and 9 in the LBREMR register (address 18h).
13	Speed Selection	1, RW	**SPEED SELECT:** 1 = 100 Mb/s 0 = 10 Mb/s Link speed is selected by this bit or by Auto-Negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored).
12	Auto-Negotiation Enable	1, RW	**AUTO-NEGOTIATION ENABLE:** 1 = Auto-Negotiation Enabled—bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled—bits 8 and 13 determine the link speed and mode.
11	Power Down	0, RW	**POWER DOWN:** 1 = Power Down 0 = Normal Operation The power-down mode is not currently implemented. Setting this bit has no effect.
10	Isolate	(PHYAD = 00000), RW	**ISOLATE:** 1 = Isolates the DP83840 from the MII with the exception of the serial management. When this bit is asserted, the DP83840 does not respond to TXD[3:0], TX_EN, and TX_ER inputs, and it presents a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL and CRS outputs. The CLK_25M output stays active and the DP83840 still responds to serial management transactions. 0 = Normal Operation If the PHY Address is set to 00000 the Isolate bit will be set upon power-up/reset.
9	Restart Auto-Negotiation	0, RW/SC	**RESTART AUTO-NEGOTIATION:** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 of this register cleared), this bit has no function and should be cleared. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated by the DP83840, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal Operation

4.0 Registers (Continued)

4.2 BASIC MODE CONTROL REGISTER (BMCR) (Continued)

Bit	Bit Name	Default	Description
8	Duplex Mode	1, RW	**DUPLEX MODE:** 1 = Full Duplex operation. Duplex selection is allowed when Auto-Negotiation is disabled (bit 12 of this register is cleared). With Auto-Negotiation enabled, this bit reflects the duplex capability as specified in bits 11 to 15 of the BMSR register (address 1h). 0 = Half Duplex Operation
7	Collision Test	0, RW	**COLLISION TEST:** 1 = Collision Test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_ER. 0 = Normal Operation
6:0	Reserved	X, RO	**RESERVED:** Write as 0, read as don't care.

4.3 BASIC MODE STATUS REGISTER (BMSR)

Address 01h

Bit	Bit Name	Default	Description
15	100BASE-T4	0, RO/P	**100BASE-T4 CAPABLE:** 1 = DP83840 able to perform in 100BASE-T4 mode 0 = DP83840 not able to perform in 100BASE-T4 mode
14	100BASE-TX Full Duplex	1, RO/P	**100BASE-TX FULL DUPLEX CAPABLE:** 1 = DP83840 able to perform 100BASE-TX in full duplex mode 0 = DP83840 not able to perform 100BASE-TX in full duplex mode
13	100BASE-TX Half Duplex	1, RO/P	**100BASE-TX HALF DUPLEX CAPABLE:** 1 = DP83840 able to perform 100BASE-TX in half duplex mode 0 = DP83840 not able to perform 100BASE-TX in half duplex mode
12	10BASE-T Full Duplex	1, RO/P	**10BASE-T FULL DUPLEX CAPABLE:** 1 = DP83840 able to perform 10BASE-T in full duplex mode 0 = DP83840 not able to perform 10BASE-T in full duplex mode
11	10BASE-T Half Duplex	1, RO/P	**10BASE-T HALF DUPLEX CAPABLE:** 1 = DP83840 able to perform 10BASE-T in half duplex mode 0 = DP83840 not able to perform 10BASE-T in half duplex mode
10:6	Reserved	0, RO	**RESERVED:** Write as 0, read as don't care.
5	Auto-Negotiation Complete	0, RO	**AUTO-NEGOTIATION COMPLETE:** 1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Remote Fault	0, RO/L	**REMOTE FAULT:** 1 = Remote Fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DP83840 implementation specific. This bit is set if the RF bit in the ANLPAR (bit 13, register address 05h) is set. 0 = No remote fault condition detected
3	Auto-Negotiation Ability	1, RO/P	**AUTO CONFIGURATION ABILITY:** 1 = DP83840 is able to perform Auto-Negotiation 0 = DP83840 is not able to perform Auto-Negotiation

4.0 Registers (Continued)

4.3 BASIC MODE STATUS REGISTER (BMSR) (Continued)

Address 01h

Bit	Bit Name	Default	Description
2	Link Status	0, RO/L	**LINK STATUS:** 1 = Valid link established (for either 10 Mb/s or 100 Mb/s operation) 0 = Link not established The criteria for link validity is implementation specific. The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to become cleared and remain cleared until it is read via the management interface.
1	Jabber Detect	0, RO/L	**JABBER DETECT:** 1 = Jabber condition detected 0 = No Jabber This bit is implemented with a latching function so that the occurrence of a jabber condition causes it to become set until it is cleared by a read to this register by the management interface or by a DP83840 reset. This bit only has meaning in 10 Mb/s mode.
0	Extended Capability	1, RO/P	**EXTENDED CAPABILITY:** 1 = Extended register capable 0 = Basic register capable only

4.4 PHY IDENTIFIER REGISTER #1 (PHYIDR1)

Address 02h

The PHY Identifier Registers #1 and #2 together form a unique identifier for the DP83840. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

National Semiconductor's IEEE assigned OUI is 080017h.

Bit	Bit Name	Default	Description
15:0	OUI_MSB	<00 1000 0000 0000 00>, RO/P	**OUI MOST SIGNIFICANT BITS:** This register stores bits 3 to 18 of the OUI (080017h) to bits 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

4.5 PHY IDENTIFIER REGISTER #2 (PHYIDR2)

Address 03h

Bit	Bit Name	Default	Description
15:10	OUI_LSB	<01 0111>, RO/P	**OUI LEAST SIGNIFICANT BITS:** Bits 19 to 24 of the OUI (080017h) are mapped to bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	<00 0000>, RO/P	**VENDOR MODEL NUMBER:** Six bits of vendor model number mapped to bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	<0000>, RO/P	**MODEL REVISION NUMBER:** Four bits of vendor model revision number mapped to bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major DP83840 device changes.

4.0 Registers (Continued)

4.6 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (ANAR)

Address 04h

This register contains the advertised abilities of this DP83840 device as they will be transmitted to its Link Partner during Auto-Negotiation.

Bit	Bit Name	Default	Description
15	NP	0, RO/P	**NEXT PAGE INDICATION:** 0 = Not Next Page able 1 = Next Page able The DP83840 is not Next Page capable so this bit is permanently set to 0.
14	ACK	0, RO/P	**ACKNOWLEDGE:** 1 = Reception of Link Partner ability data acknowledged 0 = Not acknowledged The DP83840's Auto-Negotiation state machine will automatically control this bit in the outgoing FLP bursts, setting it at the appropriate time during the Auto-Negotiation process. Software should not attempt to write to this bit.
13	RF	0, RW	**REMOTE FAULT:** 1 = Advertises that this device has detected a Remote Fault 0 = No Remote Fault detected
12:10	Reserved	X, RW	**RESERVED:** Write as 0, read as don't care.
9	T4	0, RO/P	**100BASE-T4 SUPPORT:** 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 not supported The DP83840 does not support 100BASE-T4 so this bit is permanently set to 0.
8	TX_FD	1, RW	**100BASE-TX FULL DUPLEX SUPPORT:** 1 = 100BASE-TX Full Duplex is supported by the local device 0 = 100BASE-TX Full Duplex not supported
7	TX	1, RW	**100BASE-TX SUPPORT:** 1 = 100BASE-TX is supported by the local device 0 = 100BASE-TX not supported
6	10_FD	1, RW	**10BASE-T FULL DUPLEX SUPPORT:** 1 = 10BASE-T Full Duplex is supported by the local device 0 = 10BASE-T Full Duplex not supported
5	10	1, RW	**10BASE-T SUPPORT:** 1 = 10BASE-T is supported by the local device 0 = 10BASE-T not supported
4:0	Selector	<00001>, RW	**PROTOCOL SELECTION BITS:** These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD

4.0 Registers (Continued)

4.7 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (ANLPAR)

Address 05h

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation.

Bit	Bit Name	Default	Description
15	NP	0, RO	**NEXT PAGE INDICATION:** 0 = Link Partner not Next Page able 1 = Link Partner is Next Page able
14	ACK	0, RO	**ACKNOWLEDGE:** 1 = Link Partner acknowledges reception of the ability data word 0 = Not acknowledged The DP83840's Auto-Negotiation state machine will automatically control the use of this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
13	RF	0, RO	**REMOTE FAULT:** 1 = Remote Fault indicated by Link Partner 0 = No Remote Fault indicated by Link Partner
12:10	Reserved	X, RO	**RESERVED:** Write as 0, read as don't care.
9	T4	0, RO	**100BASE-T4 SUPPORT:** 1 = 100BASE-T4 is supported by the Link Partner 0 = 100BASE-T4 not supported by the Link Partner
8	TX_FD	0, RO	**100BASE-TX FULL DUPLEX SUPPORT:** 1 = 100BASE-TX Full Duplex is supported by the Link Partner 0 = 100BASE-TX Full Duplex not supported by the Link Partner
7	TX	0, RO	**100BASE-TX SUPPORT:** 1 = 100BASE-TX is supported by the Link Partner 0 = 100BASE-TX not supported by the Link Partner
6	10_FD	0, RO	**10BASE-T FULL DUPLEX SUPPORT:** 1 = 10BASE-T Full Duplex is supported by the Link Partner 0 = 10BASE-T Full Duplex not supported by the Link Partner
5	10	0, RO	**10BASE-T SUPPORT:** 1 = 10BASE-T is supported by the Link Partner 0 = 10BASE-T not supported by the Link Partner
4:0	Selector	<00000>, RO	**PROTOCOL SELECTION BITS:** Link Partner's binary encoded protocol selector.

4.0 Registers (Continued)

4.8 AUTO-NEGOTIATION EXPANSION REGISTER (ANER)

Address 06h

Bit	Bit Name	Default	Description
15:5	Reserved	0, RO	**RESERVED:** Always 0.
4	MLF	0, RO	**MULTIPLE LINK FAULT:** 1 = Multiple Link Fault—indicates that it was not possible to resolve the connection because the Link Partner did not support Auto-Negotiation or was unable to distinguish a common ability. 0 = No Multiple Link Fault This Feature is not currently supported in the DP83840.
3	LP_NP_ABLE	0, RO	**LINK PARTNER NEXT PAGE ABLE:** Status indicating if the Link Partner supports Next Page negotiation. A one indicates that the Link Partner does support Next Page. This Feature is not currently supported in the DP83840.
2	NP_ABLE	0, RO/P	**NEXT PAGE ABLE:** Indicates if this node is able to send additional "Next Pages". The DP83840 is not Next Page Able, so this bit is always zero.
1	PAGE_RX	0, RO	**LINK CODE WORD PAGE RECEIVED:** This bit is set when a new Link Code Word Page has been received. This bit is automatically cleared when the Auto-Negotiation Link Partner Ability Register (ANLPAR register 05h) is read by management. This Feature is not currently supported in the DP83840.
0	LP_AN_ABLE	0, RO	**LINK PARTNER AUTO-NEGOTIATION ABLE:** A one in this bit indicates that the Link Partner supports Auto-Negotiation.

4.9 DISCONNECT COUNTER REGISTER (DCR)

Address 12h

Bit	Bit Name	Default	Description
15:0	DCNT[15:0]	<0000h>, RW/SC	**DISCONNECT COUNTER:** This 16-bit counter increments for each disconnect event. Each time this DP83840 and its Link Partner are disconnected from each other, the counter increments. This counter automatically rolls over to 0000h.

4.10 FALSE CARRIER SENSE COUNTER REGISTER (FCSCR)

Address 13h

Bit	Bit Name	Default	Description
15:0	FCSCNT[15:0]	<0000h>, RW/SC	**FALSE CARRIER EVENT COUNTER:** This 16-bit counter increments for each false carrier event, that is, when carrier sense is asserted without J/K symbol detection. This counter freezes when full (at FFFFh).

4.0 Registers (Continued)

4.11 RECEIVE ERROR COUNTER REGISTER (RECR)

Address 15h

Bit	Bit Name	Default	Description
15:0	RXERCNT[15:0]	<0000h>, RW/SC	**RX__ER COUNTER:** This 16-bit counter is incremented for each packet in which a receive error is detected. If there are one or more receiver error conditions during a valid packet reception (i.e. no collision occurred during packet reception), the counter is incremented once at the end of packet reception. This counter rolls over when full.

4.12 SILICON REVISION REGISTER (SRR)

Address 16h

Bit	Bit Name	Default	Description
15:8	SIREV[15:8]	<00h>, RO/P	**ARCHITECTURE LEVEL:** This number will be incremented at the next major architectural change to the device.
7:8	SIREV[7:0]	<00h>, RO/P	**CIRCUIT ENHANCEMENT LEVEL:** This number will be incremented at the next minor circuit change to the device.

4.13 PCS CONFIGURATION REGISTER (PCR)

Address 17h

Bit	Bit Name	Default	Description
15	NRZI__EN	1, RW	**NRZI ENABLE:** 1 = NRZI encoding and decoding of the transmit and receive data streams 0 = NRZI encoding and decoding disabled
14	Reserved	X, RO	**RESERVED:** Write as 0, read as don't care.
13	TO__DIS	0, RW	**TIMEOUT DISABLE:** 1 = Timeout Counter in the descrambler section of the receiver disabled 0 = Timeout Counter enabled
12	REPEATER	(Pin #47), RW	**REPEATER/NODE MODE:** 1 = Repeater mode 0 = Node mode In repeater mode the Carrier Sense (CRS) output from the DP83840 is asserted due to receive activity only. In node mode, and not configured for Full Duplex operation, CRS is asserted due to either receive or transmit activity. The value of the REPEATER pin 47 (set by a pull-up or pull-down resistor, typically 4.7 kΩ) is latched into this bit at power-up/reset.
11	ENCSEL	0, RW	**ENCODER MODE SELECT:** 1 = External transceiver binary encoding 0 = External transceiver MLT3 encoding This bit drives the DP83840's ENCSEL signal (pin 53). ENCSEL should be connected to the ENCSEL input of a DP83223 Twister.
10:8	Reserved	X, RO	**RESERVED:** Write as 0, read as don't care.
7	CLK25MDIS	0, RW	**CLK25M DISABLE:** 1 = CLK25M output clock signal (pin 81) tri-stated 0 = CLK25M enabled This helps reduce ground bounce and power consumption should this output not be required. For applications requiring the CLK25M output, leave this bit set to 0. See Section 3.5 for more details.

4.0 Registers (Continued)

4.13 PCS CONFIGURATION REGISTER (PCR) (Continued)

Address 17h

Bit	Bit Name	Default	Description
6	F_LINK_100	1, RW	**FORCE GOOD LINK IN 100 Mb/s:** 1 = Normal 100 Mb/s operation 0 = Force 100 Mb/s Good Link status This bit is useful for diagnostic purposes.
5	F_CONNECT	0, RW	**FORCE DISCONNECT FUNCTION BYPASS:** 1 = Force Link Disconnect Function to be bypassed 0 = Normal operation
4	TX_OFF	0, RW	**FORCE TRANSMIT OFF:** 1 = TD+ and TD− 100 Mb/s outputs forced to be inactive 0 = Normal 100 Mb/s transmission enabled
3	Reserved	X, RO	**RESERVED:** Write as 0, read as don't care.
2	LED1_MODE	0, RW	**LED1 MODE SELECT:** 1 = $\overline{\text{LED1}}$ output (pin 42) configured to indicate connection status (CON_STATUS, bit 5 of the PAR, address 19h). This is useful for network management purposes in 100BASE-TX mode. 0 = Normal $\overline{\text{LED1}}$ operation—10 Mb/s and 100 Mb/s transmission activity
1	LED4_MODE	0, RW	**LED4 MODE SELECT:** 1 = $\overline{\text{LED4}}$ output (pin 37) configured to indicate Full Duplex mode status for 10 Mb/s and 100 Mb/s operation 0 = $\overline{\text{LED4}}$ output configured to indicate Polarity in 10BASE-T mode or Full Duplex in 100BASE-TX mode
0	Reserved	X, RO	**RESERVED:** Write as 0, read as don't care.

4.14 LOOPBACK, BYPASS AND RECEIVER ERROR MASK REGISTER (LBREMR)

Address 18h

Bit	Bit Name	Default	Description
15	Reserved	1, RW	**RESERVED:** Write as 1, read as don't care.
14	BP_4B5B	(Pin# 100), RW	**BYPASS 4B5B ENCODING AND 5B4B DECODING:** The value of the BP4B5B pin (100) is latched into this bit at power-up/reset. 1 = 4B5B encoder and 5B4B decoder functions bypassed 0 = Normal 4B5B and 5B4B operation
13	BP_SCR	(Pin# 1), RW	**BYPASS SCRAMBLER/DESCRAMBLER FUNCTION:** The value of the BPSCR pin (1) is latched into this bit at power-up/reset. 1 = Scrambler and descrambler functions bypassed 0 = Normal scrambler and descrambler operation
12	BP_ALIGN	(Pin# 99), RW	**BYPASS SYMBOL ALIGNMENT FUNCTION:** The value of the BPALIGN pin (99) is latched into this bit at power-up/reset. 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
11	10BT_LPBK	0, RW	**10BASE-T ENCODER/DECODER LOOPBACK:** 1 = Data loopback in the 10BASE-T ENDEC enabled 0 = Normal Operation
10	Reserved	(pin# 49), RW	**RESERVED:** Write as 0, read as don't care.

4.0 Registers (Continued)

4.14 LOOPBACK, BYPASS AND RECEIVER ERROR MASK REGISTER (LBREMR) (Continued)

Bit	Bit Name	Default	Description
9:8	LB[1:0]	<00>, RW	**LOOPBACK CONTROL BITS 1:0 :** These bits control the 100 Mb/s loopback function as follows: **LB1 LB0 Mode** 0 0 Normal Mode 0 1 DP83223 Twister Loopback 1 0 Remote Loopback—Received data is looped back to the transmit channel at the MII. This is useful for bit error rate testings. 1 1 Reserved Note that Twister Loopback, like the internal loopback described in the BMCR bit 14 (address 00h), will produce a "dead time" of 330 μs before any valid data appears at the RXD outputs.
7:5	Reserved	0, RW	**RESERVED:** Write as 0, read as don't care.
4	CODE_ERR	0, RW	**CODE ERRORS:** 1 = Forces code errors to be reported with the value 5h on RXD[3:0] and with RX_ER set to 1 0 = Forces code errors to be reported with the value 6h on RXD[3:0] and with RX_ER set to 1
3	PE_ERR	0, RW	**PREMATURE END ERRORS:** 1 = Forces premature end errors to be reported with the value 4h on RXD[3:0] and with RX_ER set to 1 0 = Forces premature end errors to be reported with the value 6h on RXD[3:0] and with RX_ER set to 1 Premature end errors are caused by the detection of two IDLE symbols in the receive data stream prior to the T/R symbol pair denoting end of stream delimiter.
2	LINK_ERR	0, RW	**LINK ERRORS:** 1 = Forces link errors to be reported with the value 3h on RXD[3:0] and with RX_ER set to 1 0 = Data is passed to RXD[3:0] unchanged and with RX_ER set to 0
1	PKT_ERR	0, RW	**PACKET ERRORS:** 1 = Forces packet errors (722 μs timeout) to be reported with the value 2h on RXD[3:0] and with RX_ER set to 1 0 = Data is passed to RXD[3:0] unchanged and with RX_ER set to 0
0	Reserved	0, RW	**RESERVED:** Write as 0, read as don't care.

4.0 Registers (Continued)

4.15 PHY ADDRESS REGISTER (PAR)

Address 19h

Bit	Bit Name	Default	Description
15:7	Reserved	0, RO	**RESERVED:** Write as 0, read as don't care.
6	SPEED_10	RO	**SPEED INDICATION:** This bit indicates the current operational speed of the DP83840. 1 = 10 Mb/s operation 0 = 100 Mb/s operation This bit is only valid if a good link condition has been met. Good link is indicated when bit 2 of the BMSR (address 01h) is set.
5	CON_STATUS	0, RO/L	**CONNECT STATUS:** This bit indicates the status of the disconnect function. The connect status is optionally muxed out through the $\overline{\text{LED1}}$ pin when the $\overline{\text{LED1}}$_MODE register bit (bit 2 of the PCR, address 17h) is asserted. 1 = Valid link connection detected 0 = Valid link connection not detected
4:0	PHYADDR[4:0]	(PHYAD), RW	**PHY ADDRESS BITS 4:0:** The values of the PHYAD[4:0] pins are latched to this register at power-up/reset. See Section 2.8 for the description of these pins. The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY. A PHY address of <00000> will cause the Isolate bit of the BMCR (bit 10, register address 00h) to be set.

4.16 10BASE-T STATUS REGISTER (10BTSR)

Address 1Bh

Bit	Bit Name	Default	Description
15:10	Reserved	0, RO	**RESERVED:** Write as 0, read as don't care.
9	10BT_SER	(Pin#98), RW	**10BASE-T SERIAL MODE:** The value on the 10BTSER pin (98) is latched into this bit at power-up/reset. 1 = 10BASE-T serial mode selected (see Sections 2.5 and 3.1.3.3 for more details) 0 = 10BASE-T nibble mode selected (see Section 3.1.3.2) Serial mode is not supported for 100 Mb/s operation.
8:0	Reserved	0, RO	**RESERVED:** Write as 0, read as don't care.

4.0 Registers (Continued)

4.17 10BASE-T CONFIGURATION REGISTER (10BTCR)

Address 1Ch

Bit	Bit Name	Default	Description
15:6	Reserved	0, RO/P	**RESERVED:** Write as 0, read as don't care.
5	LP_EN	1, RW	**LINK PULSE ENABLE:** 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced When configured for 100 Mb/s operation with Auto-Negotiation enabled, clearing this bit will force the DP83840 into 10 Mb/s operation with link pulses disabled. If the DP83840 has been configured for 100 Mb/s operation with Auto-Negotiation disabled, this bit will not affect operation.
4	HBE	1, RW	**HEARTBEAT ENABLE:** 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the DP83840 is configured for Full Duplex operation, this bit will be ignored (the collision/ heartbeat function has no meaning in Full Duplex mode).
3	UTP/STP	1, RW	**UTP/STP MEDIA SELECT:** Selects between the Unshielded Twisted Pair (UTP) transmit outputs (TXU+/−) and the Shielded Twisted Pair (STP) transmit outputs (TXS+/−). 1 = UTP selected 0 = STP selected Only one output pair (TXU+/− or TXS+/−) may be selected at one time. The pair that is not selected will tri-state.
2	LSS	0, RW	**LOW SQUELCH SELECT:** Selects between standard 10BASE-T receiver squelch threshold and a reduced squelch threshold that is useful for longer cable applications and/or STP operation. 1 = Low Squelch Threshold selected 0 = Normal 10BASE-T Squelch Threshold selected
1	Reserved	0, RO	**RESERVED:** Write as 0, read as don't care.
0	JABEN	1, RW	**JABBER ENABLE:** Enables or disables the Jabber function when the DP83840 is in 10BASE-T Full Duplex or 10BASE-T Transceiver Loopback mode (10BT_LPBK bit 11 in the LBREMR, address 18h). 1 = Jabber function enabled 0 = Jabber function disabled

5.0 DP83840 Application

5.1 TYPICAL BOARD LEVEL APPLICATION

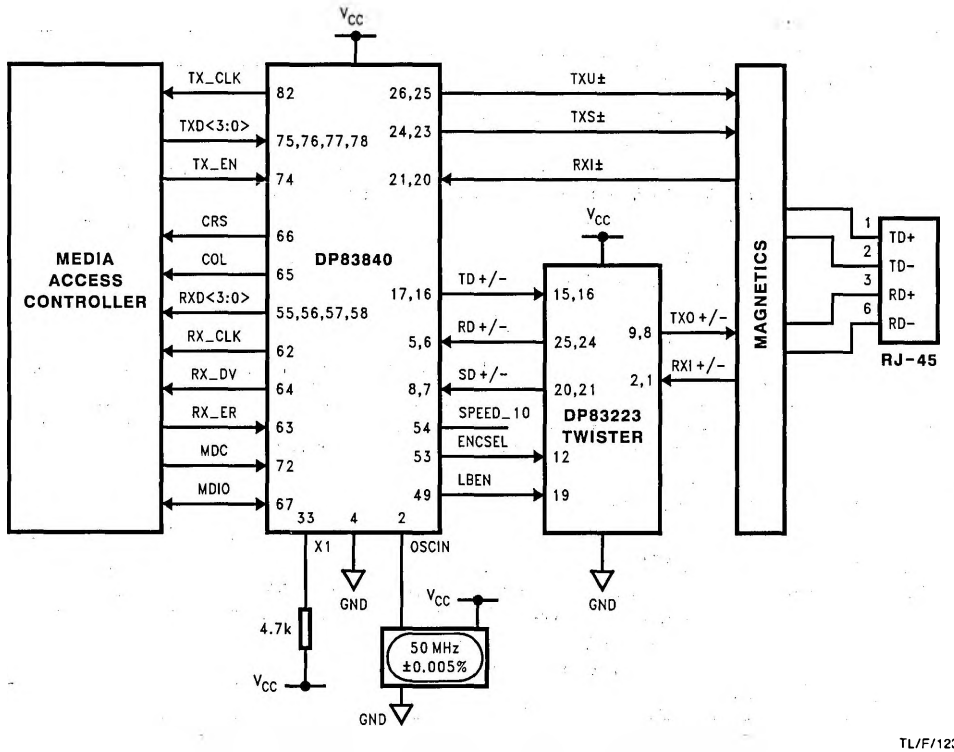


FIGURE 15. Typical Implementation of a 10/100 Mb/s Ethernet Node

Figure 15 shows a typical implementation of a 10/100 Mb/s Ethernet node application. This is given only to indicate the major circuit elements of such a design. It is not intended to be a full circuit diagram.

5.0 DP83840 Application (Continued)

The TD, SD and RD ECL differential signals must be terminated by a standard ECL load of 50Ω to a voltage source of 2V lower than V_{CC} or the equivalent circuit: a Thevenin equivalent of 130Ω to GND accompanied by 82Ω to V_{CC}.

5.2 LAYOUT RECOMMENDATIONS

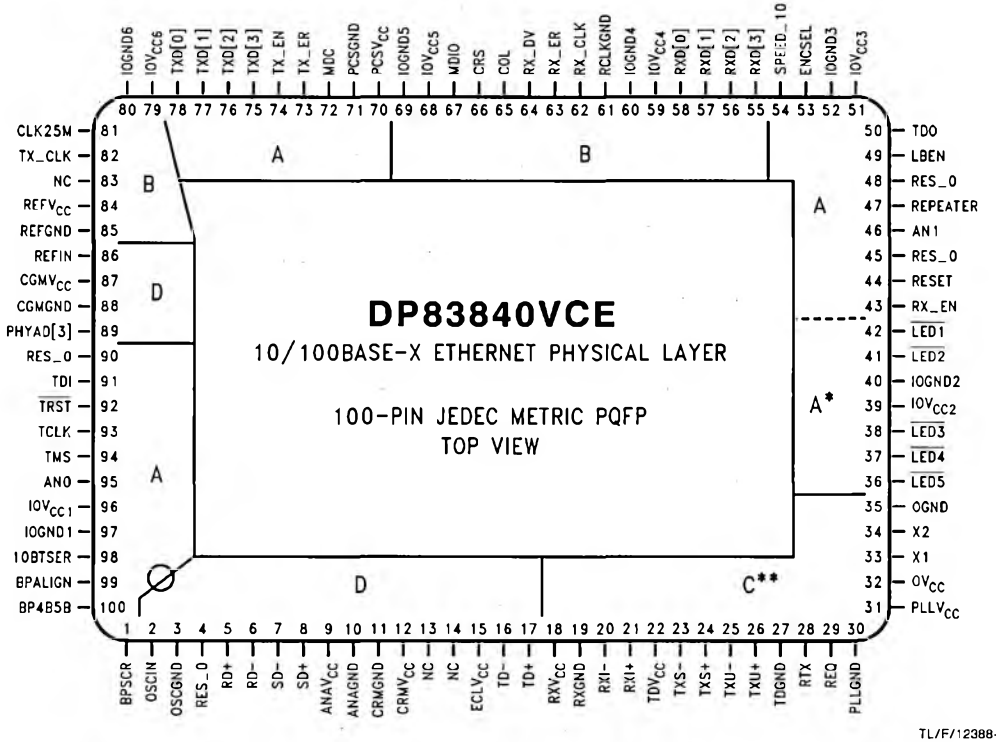
The V_{CC} and Ground pins of the DP83840 are divided into 4 separate groups (as previously described in Section 2.10) to minimize ground bounce and cross talk as given in Table IV below.

TABLE IV. Supply Groupings

Group	Description
A	TTL/CMOS Inputs V_{CC} and GND Supply Pairs
B	TTL/CMOS Outputs V_{CC} and GND Supply Pairs
C	10BASE-T Circuitry V_{CC} and GND Supply Pairs
D	100BASE-X Circuitry V_{CC} and GND Supply Pairs

5.2.1 Signal Groupings vs V_{CC} and GND Pairs

Figure 16 below shows how the signal pins are associated with the 4 groups of supply pins.



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*Pins 36 through 42 should preferably be grouped as "B" according to the table in Section 5.2, however, they are assigned as "A" to avoid further fragmentation of the power and ground planes. It is recommended that low current LEDs be used to minimize ground bounce caused by switching currents.

**Group C requires that the PLL supply pins are further partitioned with a single point of return to the digital supply. See Section 5.3 for more details.

FIGURE 16. Power and Ground Grouping

5.0 DP83840 Application (Continued)

5.3 PLANE PARTITIONING

The diagrams in *Figures 17* and *18* illustrate one approach to the partitioning of the power and ground planes at the board level. The A, B, C, and D plane notations reference the layout recommendations given in Section 5.2. The "E" plane notation shows additional partitioning that is required by the DP83223 Twister transceiver device.

As indicated by the component placement in *Figure 17*, the distance between the 50 MHz oscillator (OSC) and the DP83840 should be minimized. This also applies to the 20 MHz crystal (X1) if it is included in the design.

Minimizing all signal trace lengths and using micro strip impedance control methods for the 100 Mb/s interconnections is recommended.

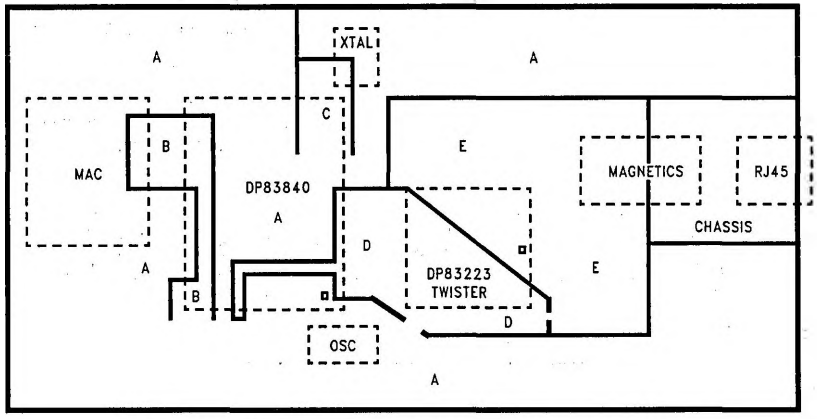

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FIGURE 17. Recommended Ground Plane (GND) Partitioning

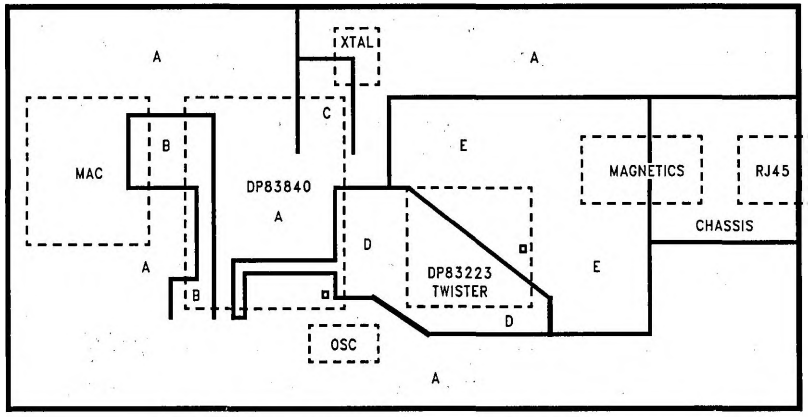

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FIGURE 18. Recommended Power Plane (V_{CC}) Partitioning

5.0 DP83840 Application (Continued)

5.4 POWER AND GROUND FILTERING

Sufficient filtering between the DP83840 power and ground pins placed as near to these pins as possible is recommended. *Figure 19* suggests filtering for each power and ground pair as well as special consideration for the sensitive analog and PLL power pins.

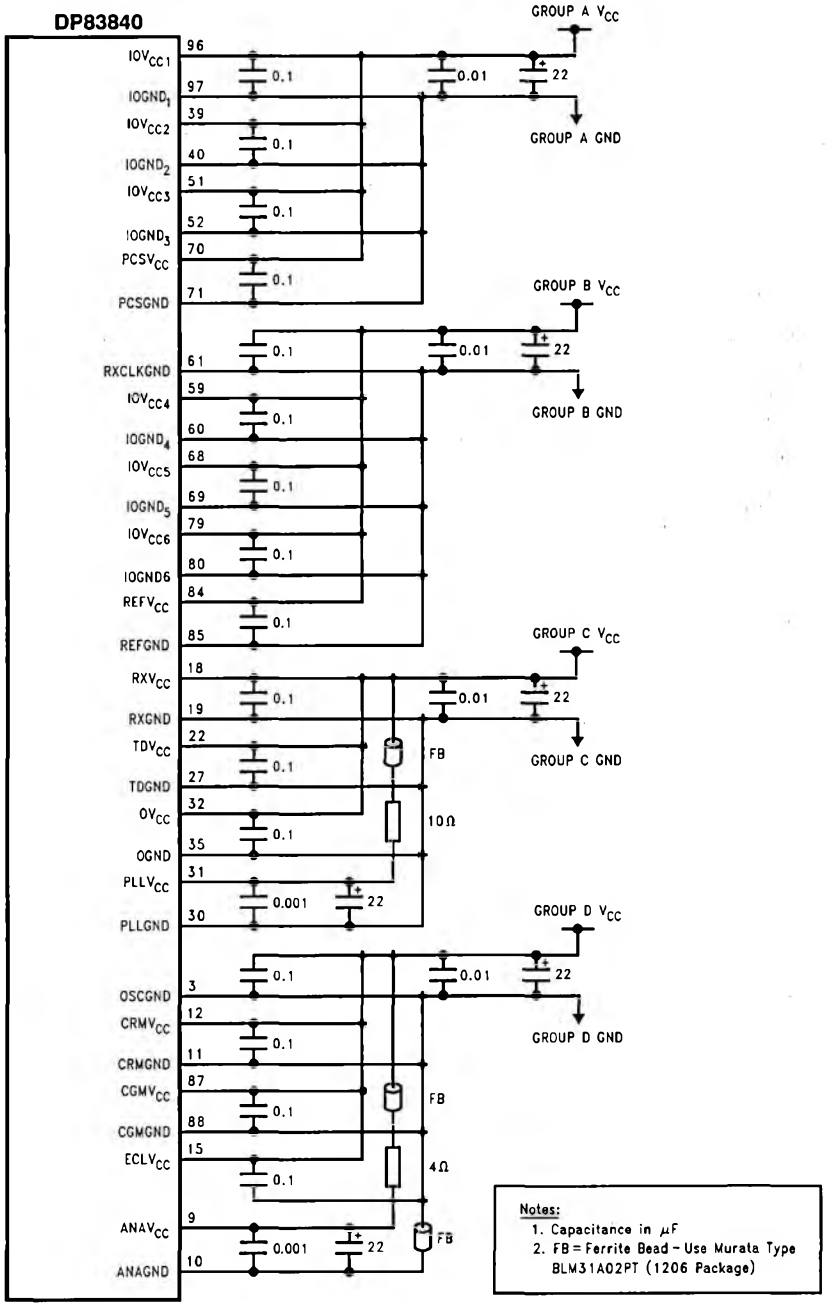

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FIGURE 19. Recommended Power and Ground Filtering for Node Applications

6.0 DC and AC Specifications

6.1 RATINGS AND OPERATING CONDITIONS

6.1.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
Input Voltage (DC_{IN})	−0.5V to V_{CC} + 0.5V
Output Voltage (DC_{OUT})	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C
ECL Signal Output Current	−50 mA
ESD Protection	2000V

6.1.2 Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Ambient Temperature (T_A)	0		70	°C
REFIN Input Frequency (25 MHz)	−50		+50	ppm
REFIN Input Duty Cycle	35		65	%
OSCIN Input Frequency (50 MHz)	−50		+50	ppm
OSCIN Input Duty Cycle	35		65	%
Crystal Specifications:				
Crystal Center Frequency (X_{FC})		20		MHz
Crystal Freq. Calibration (X_{CAL})	−10		10	ppm
Crystal Freq. Stability (X_{STAB}) (Over Temperature)	−10		10	ppm
Crystal Aging (X_{AGING})	−10		10	ppm

6.2 DC SPECIFICATIONS

Symbol	Pin Types	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	I (except RXI+/−) I/O I/O, Z	Input High Voltage		2.0			V
	AN0 and AN1 Input Pins		I_{IH} = 2 mA	V_{CC} − 1.0			V
V_{IL}	I (except RXI+/−) I/O I/O, Z	Input Low Voltage				0.8	V
	AN0 and AN1 Input Pins		I_{IL} = −2 mA			1.0	V
V_{IM}	AN0 and AN1 Inputs Only	Input Mid Level Voltage	Pin Unconnected	(V_{CC}÷2) − 0.7	2.5	(V_{CC}÷2) + 0.7	V
I_{IH}	I I/O I/O, Z	Input High Current	V_{IN} = V_{CC}			−10	µA
	X1 Input		X2 = N.C.			−100	
I_{IL}	I I/O I/O, Z	Input Low Current	V_{IN} = GND			10	µA
	X1 Input		X2 = N.C.			100	
	TMS, TDI, $\overline{TRST}$ Inputs					1	mA
V_{OH}	O O, Z I/O I/O, Z	Output High Voltage	I_{OH} = −4 mA	V_{CC} − 0.5			V
	TX_CLK Pin			V_{CC} − 1.5			
V_{OL}	O O, Z I/O I/O, Z	Output Low Voltage	I_{OL} = 4 mA			0.4	V

6.0 DC and AC Specifications (Continued)

6.2 DC SPECIFICATIONS (Continued)

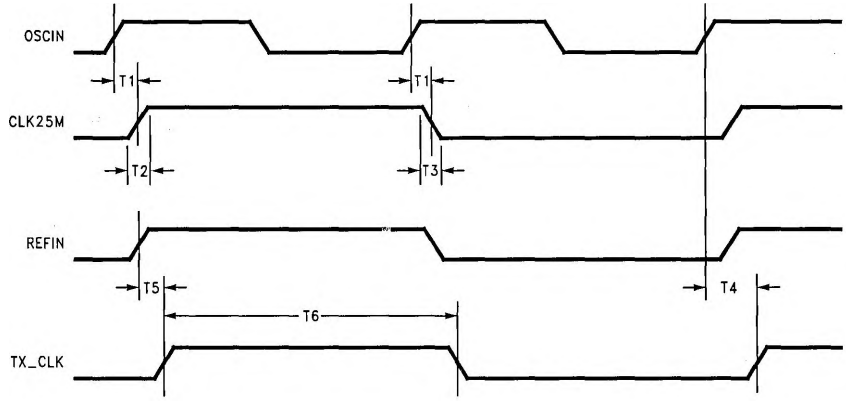
Symbol	Pin Types	Parameter	Conditions	Min	Typ	Max	Units
I_{OZ1}	I/O, Z O, Z	TRI-STATE Leakage	$V_{OUT} = V_{CC}$			10	μA
I_{OZ2}	I/O, Z O, Z	TRI-STATE Leakage	V_{OUT} = GND			−10	μA
R_{OL}	TXU+/− TXS+/−	Low Level Output Impedance			5		Ω
R_{OH}	TXU+/− TXS+/−	High Level Output Impedance			5		Ω
C_{IN}	I	Input Capacitance					pF
C_{OUT}	O Z	Output Capacitance					pF
V_{TH1}	RXI+/−	10BASE-T Receive Threshold		±300		±585	mV
V_{DIFF}	I (ECL)	Input Voltage Differential	Both Inputs Tested Together	150			mV
V_{CM}	I (ECL)	Common Mode Voltage	Both Inputs Tested Together, V_{DIFF} = 300 mV	V_{CC} − 2.0		V_{CC} − 0.5	V
I_{INECL}	I (ECL)	Input Current	$V_{IN} = V_{CC}$ or GND	−200		200	μA
V_{OHECL}	O (ECL)	Output High Voltage	$V_{IN} = V_{IH\ max}$	V_{CC} − 1.075		V_{CC} − 0.830	V
V_{OLECL}	O (ECL)	Output Low Voltage	$V_{IN} = V_{IL\ max}$	V_{CC} − 1.860		V_{CC} − 1.570	V
I_{CC}		Total Supply Current			360	400	mA

6.0 DC and AC Specifications (Continued)

6.3 AC SPECIFICATIONS

6.3.1 CGM Clock Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	OSCIN to CLK25M Delay	OSCIN = 50 MHz		10		ns
T2	CLK25M Rise Time	10% to 90%		5		ns
T3	CLK25M Fall Time	90% to 10%		5		ns
T4	OSCIN to TX_CLK Delay	10 Mb/s Operation (MII Nibble Mode)		10		ns
T4a	OSCIN to TX_CLK Delay	10 Mb/s Operation (MII Serial Mode)		10		ns
T5	REFIN to TX_CLK Delay	100 Mb/s Operation	−3.0		+3.0	ns
T6	TX_CLK Duty Cycle	10 Mb/s Nibble (2.5 MHz), 10 Mb/s Serial (10 MHz), 100 Mb/s Nibble (25 MHz)	35		65	%



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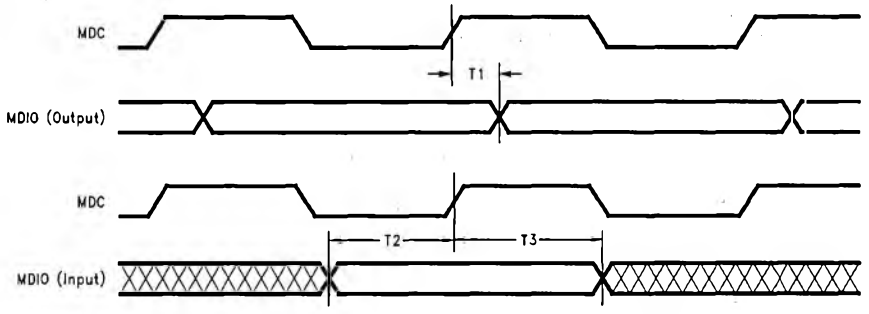
6.0 DC and AC Specifications (Continued)

6.3.2 MII Serial Management Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	MDC to MDIO (Output) Delay Time		0		300	ns
T2	MDIO (Input) to MDC Set Time		10			ns
T3	MDIO (Input) to MDC Hold Time		10			ns



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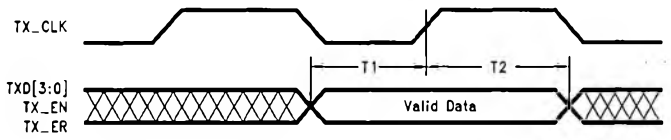
6.3.3 Transmit MII Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	TXD[3:0], TX_EN Data Setup to TX_CLK	10 Mb/s Nibble Mode	5			ns
T1a	TXD[0], Data Setup to TX_CLK	10 Mb/s Serial Mode (Note 1)	10			ns
T1b	TX_EN Data Setup to TX_CLK	10 Mb/s Serial Mode (Note 1)	30			ns
T1c	TXD, TX_EN, TX_ER Data Setup to TX_CLK	100 Mb/s Nibble Mode	5			ns
T2	TXD, TX_EN Data Hold from TX_CLK	10 Mb/s Nibble Mode	3			ns
T2a	TXD[0] Data Hold from TX_CLK	10 Mb/s Serial Mode (Note 1)	5			ns
T2b	TX_EN Data Hold from TX_CLK	10 Mb/s Serial Mode (Note 1)	5			ns
T2c	TXD, TX_EN, TX_ER Data Hold from TX_CLK	100 Mb/s Nibble Mode	3			ns

Note 1: The 10 Mb/s serial mode of operation is an additional feature of the DP83840 and is independent of the MII specifications.



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6.0 DC and AC Specifications (Continued)

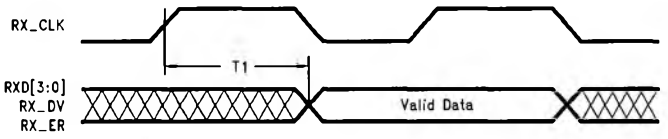
6.3.4 Receive MII Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	RX_CLK to RXD, RX_DV Delay	10 Mb/s Nibble, 10 Mb/s Serial, 100 Mb/s Nibble (Notes 1, 2)	25		35	ns
T1a	RX_CLK to RXD[3:0], RX_DV, RX_ER Delay	100 Mb/s BP_ALIGN Mode (Note 3)	−5		6	ns

Note 1: RXD[3:0], RX_DV, and RX_ER are clocked out of the DP83840 on the falling edge of RX_CLK. However, in order to specify this parameter without the RX_CLK duty cycle affecting it, the timing is taken from the previous rising edge of RX_CLK.

Note 2: The 10 Mb/s serial mode of operation is an additional feature of the DP83840 and is independent of the MII specifications.

Note 3: While in the BP_ALIGN mode of operation, RXD[3:0], RX_DV and RX_ER are clocked out of the DP83840 on the rising edge of RX_CLK. Refer to Section 3.1.1.4.



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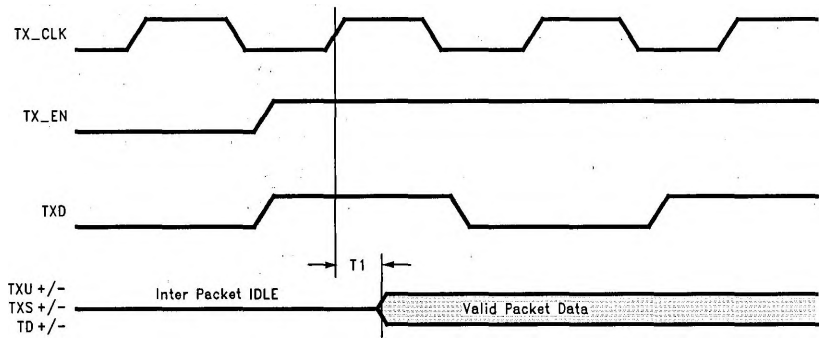
6.3.5 Transmit Packet Timing (Start of Packet)

Parameter	Description	Notes	Min	Typ	Max	Units
T1	TX_CLK to TXU+/− Latency				10	bits
T1a	TX_CLK to TD+/− Latency	(Notes 1, 2)			10	bits

Note 1: 100BASE-TX Transmit Latency maximum limit equals 14 bit times.

Note 2: The latency of the DP83840 combined with the DP83223/A equals 11 bit times.



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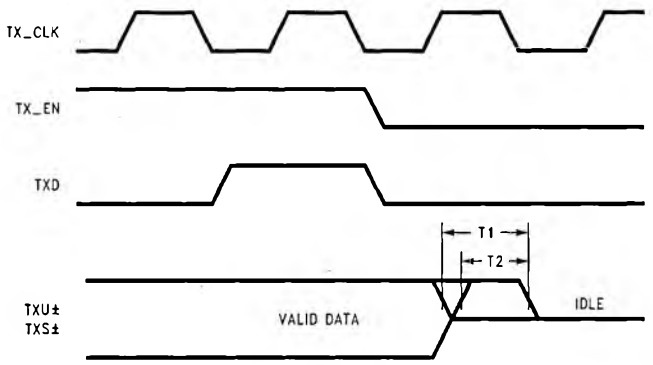
6.0 DC and AC Specifications (Continued)

6.3.6 Transmit Packet Timing (End of Packet)

Parameter	Description	Notes	Min	Typ	Max	Units
T1	End of Packet High Time	"1" As the Last Bit of the Packet, (10 Mb/s Only)	250			ns
T2	End of Packet High Time	"0" As the Last Bit of the Packet, (10 Mb/s Only)	250			ns



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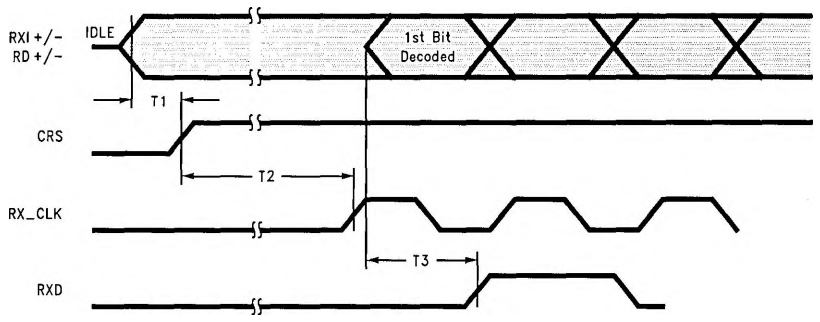
6.3.7 Receive Packet Timing (Start of Packet)

Parameter	Description	Notes	Min	Typ	Max	Units
T1	Carrier Sense on Delay	10 Mb/s Nibble,Serial			10	bits
T1a	Carrier Sense on Delay	100 Mb/s Nibble			10	bits
T2	Decoder Acquisition Time	10 Mb/s		1100	2200	ns
T3a	Receive Data Latency	10 Mb/s Nibble, Serial			20.3	bits
T3b	Receive Data Latency	100 Mb/s Nibble (Notes 1, 2)			20.3	bits
T3c	Receive Data Lateny	100 Mb/s BP_ALIGN			20.3	bits

Note 1: 100BASE-TX Receive Latency maximum limits equals 23 bit times.

Note 2: The latency of the DP83840 combined with the DP83223 equals 21 bit times.



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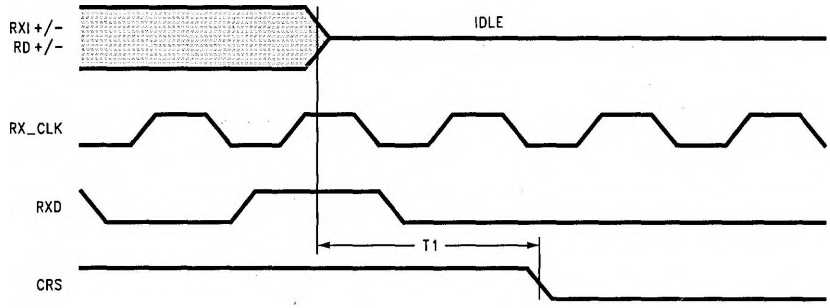
6.0 DC and AC Specifications (Continued)

6.3.8 Receive Packet Timing (End of Packet)

Parameter	Description	Notes	Min	Typ	Max	Units
T1	Carrier Sense Off Delay	10 Mb/s			8	bits
T1a	Carrier Sense Off Delay	100 Mb/s			8	bits



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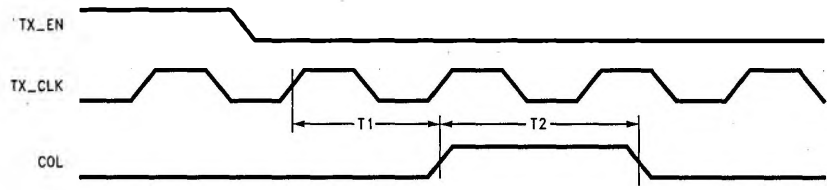
6.3.9 Heartbeat Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	Collision Detect Heartbeat Delay	10 Mb/s (Note 1)	0.6		1.6	μs
T2	Collision Detect Heartbeat Duration	10 Mb/s (Note 1)	0.5		1.5	μs

Note 1: The Heartbeat function operates during 10 Mb/s half-duplex. In 100 Mb/s half-duplex mode COL is used to indicate collisions. Since collisions cannot occur during full-duplex mode, the Heartbeat function is not implemented.



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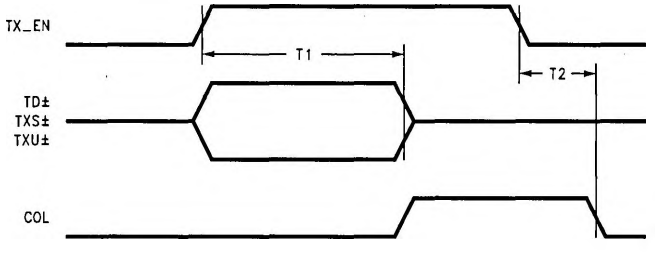
6.0 DC and AC Specifications (Continued)

6.3.10 Jabber Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	Jabber Activation Time	10 Mb/s Half Duplex		26		ms
T2	Jabber Deactivation Time	10 Mb/s Half Duplex		410		ms



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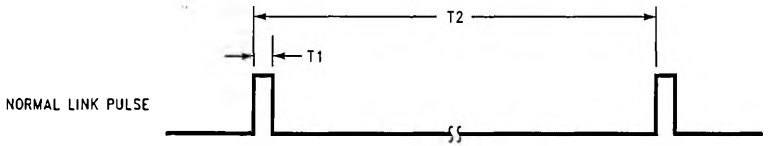
6.3.11 10BASE-T Normal Link Pulse Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	Normal Link Pulse Width			100		ns
T2	Normal Link Pulse Period		8		24	ms



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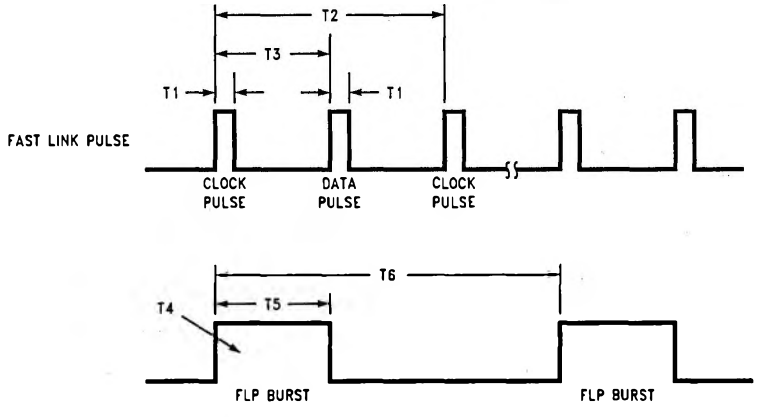
6.0 DC and AC Specifications (Continued)

6.3.12 Auto-Negotiation Fast Link Pulse (FLP) Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	Clock, Data Pulse Width			100		ns
T2	Clock Pulse to Clock Pulse Period		111	125	139	μs
T3	Clock Pulse to Data Pulse Period	Data = 1	55.5		69.5	μs
T4	Number of Pulses in a Burst		17		33	#
T5	Burst Width			2		ms
T6	FLP Burst to FLP Burst Period		8		24	ms



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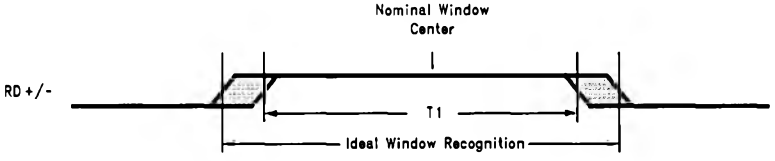
6.3.13 CRM Window Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	CRM Window Recognition Region	(Note 1)	−3		3	ns

Note 1: The ideal window recognition region is ±4 ns.



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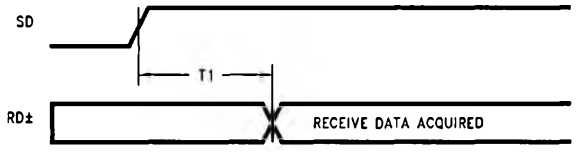
6.0 DC and AC Specifications (Continued)

6.3.14 CRM Acquisition Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	CRM Receive Clock Acquisition Time	With SD Asserted			100	μs



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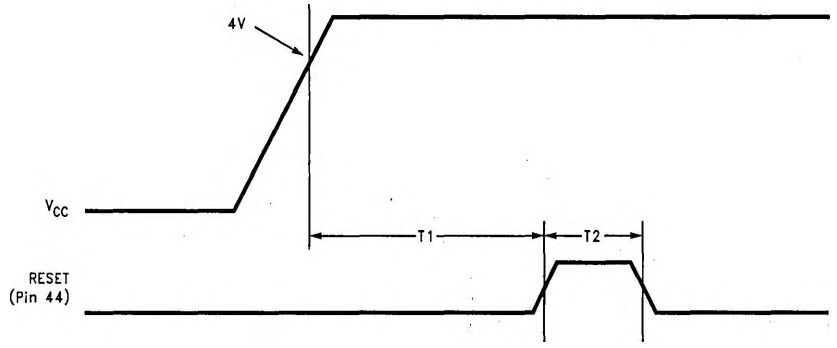
6.3.15 Reset Timing

Parameter	Description	Notes	Min	Typ	Max	Units
T1	Internal Reset Time	(Note 1)	500			μs
T2	Hardware RESET Pulse Width	(Note 2)	1			μs

Note 1: This timing assumes the use of a RESET pulse as opposed to RESET assertion immediately upon power-up. Either way, the deassertion of RESET must occur no sooner than 500 μs after initial power-up.

Note 2: The Hardware Configuration pin values will be latched into the device no later then 2 μs after the falling edge of RESET (refer to Section 3.10 for further detail).



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