National Semiconductor

DP8459 All-Code Data Synchronizer

General Description

The DP8459 Data Synchronizer is an integrated phase locked loop circuit which has been designed for application in magnetic hard disk, flexible (floppy) disk, optical disk, and tape drive memory systems for data re-synchronization and clock recovery with any standard recording code, operating to 25 Mb/s. The DP8459 is provided in a 28-pin PCC package. Zero phase start is employed during both data and reference clock lock sequences for rapid acquisition. An optional (Customer-controlled) synchronization field frequency-acquisition feature guarantees lock, accommodating the preamble types used with GCR (Group Code Recording), MFM (Modified Frequency Modulation), the [1,N] run length limited (RLL) codes, and either of the standard 2,7 RLL codes. Precise synchronization window generation is achieved via an internal, self-aligning delay line which remains accurate independent of temperature, power supply, external component and IC process variations. The DP8459 also incorporates a digitally controlled (MICROWIRE™ bus compatible) strobe function with 5-bit resolution which allows for margin testing, error recovery routines, and precise window calibration. The PLL filter resides external to the chip, with two ports provided to allow significant design flexibility. Synchronization pattern detection circuitry issues a PREAMBLE DETECTED signal when a pre-determined length of the user-selected pattern is encountered. All digital input and output signals are TTL compatible and a single, +5V power supply is required. The DP8459V is offered as a DP8459V-10 (250 Kbit/sec thru 10 Mbits/sec) or DP8459V-25 (250 Kbits/sec thru 25 Mbit/sec), see AC Electrical Characteristics.

Features

- Fully integrated dual-gain PLL
- Zero phase start lock sequence
- 250 Kbit/sec–25 Mbit/sec data rate range
- Frequency lock capability (optional) for all standard recording codes
- Digital window strobe control, 5-bit resolution
- Two-port PLL filter network
- PLL free-run (Coast) control for optical disk defects
- Synchronization pattern (preamble lock) detection
- Non-glitching multiplexed read/write clock output
- +5V supply
- DP8459 supplied in 28-pin plastic chip carrier (PCC) and 40-pin TapePak packages

Connection Diagrams

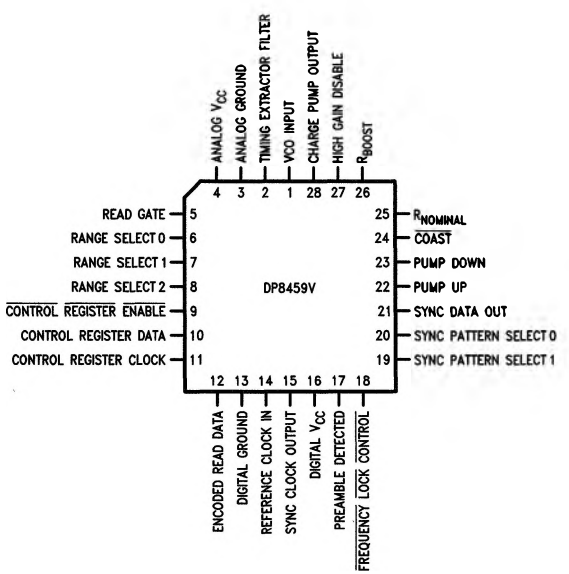

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FIGURE 1. DP8459 In 28-Pin Plastic Chip Carrier (PCC) V-Type Package Order Number DP8459V-10 or DP8459V-25

Contents

Connection Diagrams (Continued)

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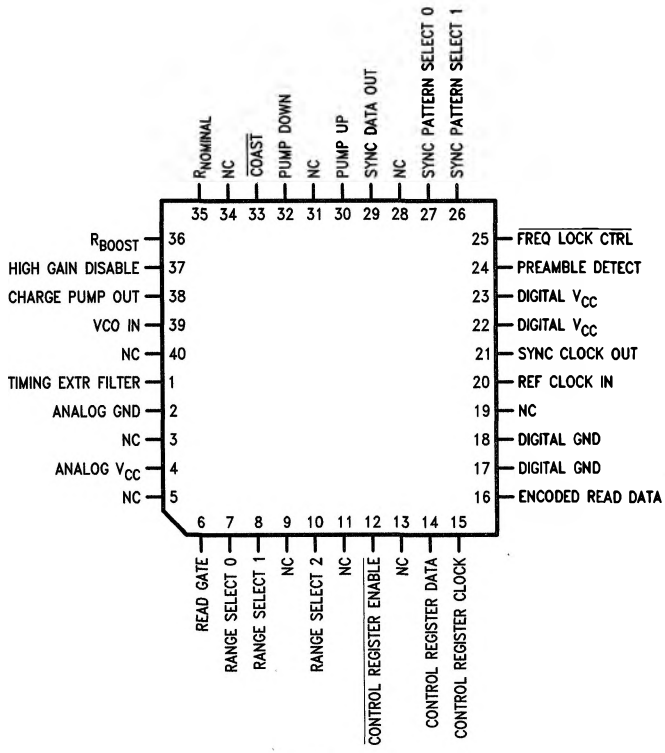

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Top View

Order Number DP8459TP-10 or DP8459TP-25
See NS Package TP40A

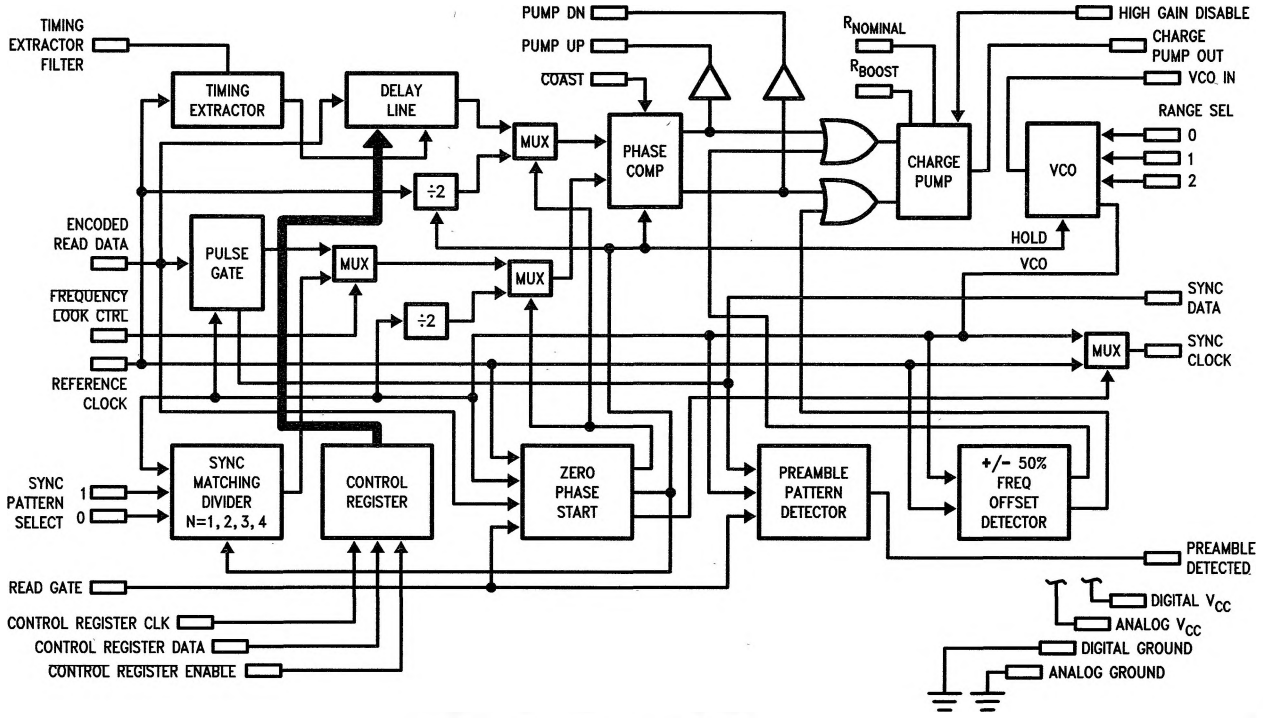

FIGURE 2. DP8459 System Block Diagram

1.0 Pin Descriptions

DP8459 28-pin PCC package

Pin #	
POWER SUPPLY	
16	**DIGITAL V_{CC}:** 5.0V ±5%. (Note 1)
4	**ANALOG V_{CC}:** 5.0V ±5%. (Note 1)
13	**DIGITAL GROUND.**
3	**ANALOG GROUND.**
TTL LEVEL LOGIC INPUTS	
5	**READ GATE (RG):** Read mode control input, active high (logical-one). Assertion causes the PLL to lock to the ENCODED READ DATA, employing a zero phase start routine. Deassertion causes the PLL to lock the REFERENCE CLOCK input, also employing a zero phase start routine. READ GATE timing is allowed to be fully asynchronous.
6, 7, 8	**RANGE SELECT 0, 1, 2 (RS0, RS1, RS2):** Control the operating frequency range of the VCO. A 2:1 continuously variable sub-range is available within each of 6 allowed selections, enabling the VCO to operate at any frequency within a 96:1 range from 500 kHz to 50 MHz.
9	**$\overline{\text{CONTROL REGISTER ENABLE}}$ ($\overline{\text{CRE}}$):** A logical Low level allows the CONTROL REGISTER CLOCK to clock data into the Control Register via the CONTROL REGISTER DATA input; a logical HIGH level latches the register data and issues the information to the appropriate circuitry.
10	**CONTROL REGISTER DATA (CRD):** Control Register data input.
11	**CONTROL REGISTER CLOCK (CRC):** Negative edge triggered Control Register clock input.
12	**ENCODED READ DATA (ERD):** Incoming TTL-level data derived from the storage media; issued from a pulse detector circuit. Each positive edge represents a single recorded code bit.
14	**REFERENCE CLOCK (RFC):** A reference frequency input **required** for DP8459 operation. The RFC frequency must be accurate and highly stable (crystal or servo derived) and equivalent to the 2F frequency for the MFM or [2,7] codes (i.e., equal to, but not derived from the VCO frequency).
18	**$\overline{\text{FREQUENCY LOCK CONTROL}}$ ($\overline{\text{FLC}}$):** Selects or de-selects the frequency lock function during a READ operation. Has no effect with READ GATE deasserted; frequency lock is automatically employed for the full duration of time READ GATE is deasserted regardless of the level of the $\overline{\text{FLC}}$ input. With READ GATE high and $\overline{\text{FLC}}$ low (logical-zero) the PLL is forced to lock to the pattern frequency selected via the SYNC PATTERN SELECT inputs. When high (logical-one) frequency lock action is terminated and the PLL employs a pulse gate to accommodate random disk data patterns. $\overline{\text{FLC}}$ may be tied to PREAMBLE DETECTED output pin for self-regulated frequency lock control. $\overline{\text{FLC}}$ timing is allowed to be fully asynchronous.
20 19	**SYNC PATTERN SELECT 0, 1 (SP0, SP1):** Control inputs for selection of the preamble type being employed. These inputs determine the pattern to which the PLL will frequency-lock during preamble acquisition (if frequency lock is employed) and for which the PREAMBLE DETECTED circuitry searches.
24	**$\overline{\text{COAST}}$ ($\overline{\text{CST}}$):** Control for Coast function. The Coast function may be activated when READ GATE is either high or low. When the $\overline{\text{COAST}}$ input is low (logical-zero), the phase comparator is disabled and held in a cleared state, allowing the VCO to coast regardless of ENCODED READ DATA input activity (READ GATE high) or REFERENCE CLOCK input activity (READ GATE low). No other circuit functions are disturbed. When high (logical-one), the phase comparator operates normally.
27	**HIGH-GAIN DISABLE (HGD):** Charge Pump gain switch control. When low (logical-zero), the charge pump input current is the combined value of the currents at both R_{BOOST} and $R_{NOMINAL}$ pins. When high (logical-one), charge pump input current is taken from the $R_{NOMINAL}$ pin only. HGD may be tied either to READ GATE or PREAMBLE DETECTED for self-regulated gain control.

Note 1: These pins should *always* be tied together; they are not intended to be used with separate power supplies.

1.0 Pin Descriptions (Continued)

DP8459 28-pin PCC package

Pin #	
TTL LEVEL LOGIC OUTPUTS	
15	**SYNCHRONIZED CLOCK (SCK):** Issues the VCO signal following READ GATE assertion and completion of zero phase start sequence; issues REFERENCE CLOCK input signal when READ GATE is deasserted. Multiplexer switching is achieved without glitches.
17	**PREAMBLE DETECTED (PDT):** Issues a high level (logical-one) following assertion of READ GATE, completion of the zero phase start sequence, and the detection of approximately 32 sequential pulses of 1T, 2T or 3T period preamble, or 16 sequential pulses of 4T period preamble, depending on state of SYNC PATTERN SELECT inputs (T = VCO period). Following preamble detection, the output remains latched high until de-assertion of READ GATE. The PDT output will be at a logical zero state whenever READ GATE is inactive.
21	**SYNCHRONIZED DATA (SD):** A reconstructed replica of the ENCODED READ DATA signal, time-stabilized and synchronized to the SYNCHRONIZED CLOCK output.
22	**PUMP UP (PU):** Active HIGH whenever the phase comparator issues a pump-up signal to the charge pump. The PU pin is an open-emitter output requiring an external passive pull down resistor whenever in active use. The output should be allowed to float when not needed.
23	**PUMP DOWN (PD):** Active HIGH whenever the phase comparator issues a pump-down signal to the charge pump. The PD pin is an open-emitter output requiring an external passive pull down resistor whenever in active use. The output should be allowed to float when not needed.
ANALOG SIGNAL PINS	
28	**CHARGE PUMP OUTPUT:** The output of the high-speed, switching bi-directional current source circuitry of the charge pump. The external, passive PLL filter network is established between this pin, the VCO INPUT pin, and ground.
1	**VCO INPUT:** The high-impedance control voltage input to the voltage controlled oscillator (VCO). The external, passive PLL filter network is established between this pin, the CHARGE PUMP OUTPUT pin, and ground.
2	**TIMING EXTRACTOR FILTER:** A pin for the connection of external, passive components employed to stabilize the delay line timing extraction circuitry. Delay accuracy is not a function of external component values or tolerances.
25	**$R_{NOMINAL}$:** A resistor is tied between this pin and V_{CC} to set the charge pump *nominal* operating current. The current is internally multiplied by 2 for charge pump use.
26	**R_{BOOST}:** A resistor is tied between this pin and V_{CC} to set the charge pump *boost* (or adder) current. The R_{BOOST} resistor is effectively paralleled with the $R_{NOMINAL}$ resistor when the HIGH GAIN DISABLE input is inactive (logical-zero); thus the sum of the resistor currents sets the total input current. The input current is multiplied by 2 within the charge pump circuitry.

2.0 Circuit Operation

In the non-Read mode, the DP8459 PLL is locked to the REFERENCE CLOCK signal. This permits the VCO to remain at a frequency very close to the encoded data clock rate while the PLL is "idling" and thus will minimize the frequency step and associated lock time encountered at the initiation of lock to ENCODED READ DATA. Frequency acquisition is employed in the non-Read mode to ensure lock.

Note: The REFERENCE CLOCK signal is employed by circuitry which sets the time delay of the internal delay line. This requires the REFERENCE CLOCK signal to be present *at all times* at a stable and accurate frequency for proper DP8459 operation.

At the assertion of READ GATE, which is allowed to be done asynchronously (no timing requirements), and following the completion of two subsequent VCO cycles, the DP8459 VCO is stopped momentarily and restarted in accurate phase alignment with the second data bit which arrives following the VCO pause. This minimization of phase misalignment between the ENCODED READ DATA and the VCO (referred to as zero phase start, or ZPS) significantly reduces data lock acquisition time.

The DP8459 incorporates a preamble-specific frequency acquisition feature which may be employed at the user's option. The frequency acquisition feature is intended specifically for use within hard or pseudo-hard sectored systems where READ GATE is asserted only within a preamble. With the READ GATE active (logical-one) and the $\overline{\text{FREQUENCY LOCK CONTROL}}$ ($\overline{\text{FLC}}$) input active (logical-zero), the DP8459 will be forced to lock to the exact preamble frequency selected at the SYNC PATTERN SELECT inputs. The frequency discriminating action of the PLL provided in this mode produces a lock-in range equivalent to the available VCO operating range and thus eliminates the possibility of fractional-harmonic lock. Windowing (pulse gate action; see Pulse Gate, Section 2.1) is not employed in the frequency acquisition mode and thus quadrature lock is prevented (see National Semiconductor Application Note AN-414, APPS Mass Storage Handbook #1, 1986, for an explanation of typical false lock modes). The DP8459 will remain in the frequency acquisition mode until the $\overline{\text{FLC}}$ input is deactivated (logical-one). In ordinary hard sectored or pseudo-hard sectored operation, the PREAMBLE DETECTED (PDT) output is tied to the $\overline{\text{FLC}}$ input for automatic switching from frequency acquisition to phase lock following internal detection of the selected preamble by the DP8459. The Customer may choose to intervene in this path and extend the frequency lock period. However, the DP8459 *must* be placed in the phase lock mode ($\overline{\text{FLC}}$ deactivated—logical-one) prior to encountering the end of the preamble, or loss of lock will result. Switching of the $\overline{\text{FLC}}$ input may be done asynchronously (no set-up or hold timing requirements).

The PREAMBLE DETECTED (PDT) output will become active (logical-one) following READ GATE assertion, completion of the ZPS sequence and the subsequent detection of approximately 32 ENCODED READ DATA (ERD) pulses of the 1T, 2T or 3T preamble types, or 16 ENCODED READ DATA (ERD) pulses of the 4T preamble type (see specification tables), and will remain active (logical-one) until deassertion of READ GATE.

The Customer has the option of employing an elevated PLL bandwidth during preamble acquisition (or at any other time) for an extended capture range. An R_{BOOST} pin is provided to allow for an increase in charge pump gain above the level set by the $R_{NOMINAL}$ pin. When the HIGH GAIN DISABLE pin (HGD) is inactive (logical-zero), the R_{BOOST} resistor is electrically paralleled with the $R_{NOMINAL}$ for an elevated charge pump gain. When HIGH GAIN DISABLE is active (logical-one), only the $R_{NOMINAL}$ resistor is employed to set the pump current. The Charge Pump throughput gain is $I_{CPO} = 2 \times I_{Rp}$ where $I_{Rp} = 0.25V_{CC}/R_p$, $R_p = R_{NOM}$ with HGD high, and $R_p = R_{NOM} || R_{BOOST}$ with HGD low. The Customer may choose to configure the system for high gain prior to DP8459 preamble detection by tying the HGD pin to the PDT output pin, or for high gain only during REFERENCE CLOCK lock by tying the HGD pin to the READ GATE pin. Other configurations may be employed, if desired.

The DP8459 issues a clock waveform from the SYNCHRONIZED CLOCK output which is derived from the REFERENCE CLOCK input when the READ GATE is inactive (logical-zero), and from the VCO signal following READ GATE assertion (logical-one) and completion of the zero phase start sequence. The REFERENCE CLOCK signal is issued from the SYNCHRONIZED CLOCK output during non-Read activity and may be used as a write clock, if desired. Once data lock is achieved and the SYNCHRONIZED CLOCK output is issuing VCO, the SYNCHRONIZED DATA output and the SYNCHRONIZED CLOCK output are held in a fixed, specified timing relationship for use by decoding/deserializing circuitry. The SYNCHRONIZED CLOCK output multiplexer switching is achieved without glitches, i.e., no pulse is narrower than 50% of the VCO or REFERENCE CLOCK period.

The DP8459 provides a $\overline{\text{COAST}}$ control input which serves to clear the phase comparator and disable charge pump action whenever taken to an active, logical-zero level. This function is made available to allow the PLL to be set to free-run, undisturbed, while a detectable defect is being read from the media in a region where re-initiation of the lock procedure is impractical (e.g., data field). External data controller circuitry is responsible for the detection of the defect and issuance of the $\overline{\text{COAST}}$ command. The primary application of this feature is expected to be optical disk bright-spot avoidance, though it will lend itself to other applications as well.

As in the previous family of National Semiconductor data separators/synchronizers, the DP8459 provides phase comparator activity information to the Customer. The phase comparator's pump-up and pump-down outputs are brought out to separate pins, PUMP UP (PU) and PUMP DOWN (PD). The outputs are of the open-emitter type, requiring an external "pull-down" resistor when in active use. These outputs serve to indicate the relative displacement of the current data bit with respect to the internal VCO phase (window center). When in completely stabilized lock with no bit displacement, the output(s) will issue a pulse of a finite, minimum-valued width for each arriving data pulse. If any data pulse is displaced with respect to the VCO phase, the corresponding output pulse will widen by an amount equivalent to the bit displacement. These output signals may be integrat-

2.0 Circuit Operation (Continued)

ed over time and employed to determine the average magnitude of media bit shift. Additionally, the pulse widening/narrowing effect bit displacement has on the PU/PD outputs produces an amplitude modulation of the output's waveform. The waveform envelope, when observed with a relatively slow oscilloscope time base, can be employed for observation of PLL dynamics. This is particularly useful if intrusive probing of the PLL filter nodes is not desirable.

It is strongly recommended that the PU/PD outputs be left "floating" (unconnected to any net or circuit element, including the output pull-down resistor) in any application where they are not specifically needed. This will serve to minimize unnecessary, spurious digital switching transients in the vicinity of the DP8459, and thus improve noise performance.

The DP8459 provides a wide operating data rate range to facilitate use within a broad base of applications, including multiple data rate systems or constant density recording (CDR). In order to achieve the specified 250 kbit /sec to 25 Mbit/sec span, the operation of the VCO has been divided into 6 contiguous frequency sub-ranges, with approximately a 2:1 ratio between adjacent range selections. Three inputs are provided for selecting of the sub-ranges, RANGE SELECT 0, 1 and 2. Some code type restrictions have been placed on the higher ranges of operating VCO frequency. See *Figure 3* for the operating data rate truth table and allowed code type versus VCO range selection.

The DP8459 allows for flexible synchronization window strobe control. The inputs CONTROL REGISTER DATA (CRD), CONTROL REGISTER CLOCK (CRC), and CONTROL REGISTER ENABLE ($\overline{CRE}$) are configured to permit interfacing of the DP8459 to the MICROWIRE™ (or equivalent) bus for entry of strobe information. Information is serially shifted into the CONTROL REGISTER via the CRD and CRC pins whenever the $\overline{CRE}$ pin is active (logical-zero). When the $\overline{CRE}$ pin is inactive (logical-one), CRD and CRC are ignored. The strobe function allows the Customer to shift the synchronization window in 31 equal steps of magnitude $t_S = M \times [1.8\% \times \tau_{VCO}]$ from approximately 27% early to 27% late with respect to nominal window position. This function may be employed for margin testing (eg., approximately ±12%) or error recovery read re-try operations (eg., approximately ±2% to ±3%). Additionally, this feature allows the Customer to align the center of the synchronization window to within one half strobe step of ideal, regardless of the initial performance or specification of the DP8459. This window centering function may be performed completely within the drive system itself (auto-alignment) given the employment of an intelligent window alignment routine. Such a routine would be configured to determine the maximum error free early and late window positions via the strobe function, and then would fix the DP8459 window in the arithmetic mean position (Section 4.3.3). See *Figure 4* for a window strobe truth table.

Note: In all DP8459 applications, provision must be made to load the appropriate information into the Control Register.

RANGE SELECT Input (Note 1)			VCO Range MHz	Equivalent NRZ Data Rate	Minimum N (Allowed Code Type)			
2	1	0		MFM or 2,7 (Mbit/sec)	1 (GCR)	2 (MFM; 1, N)	3 (2,7)	4 (2,7)
1	1	X	0.50 ≤ Fvco ≤ 1.25	0.250≤ Fnrz ≤ 0.625	√	√	√	√
1	0	1	1.25 < Fvco ≤ 2.5	0.625< Fnrz ≤ 1.25	√	√	√	√
1	0	0	2.5 < Fvco ≤ 5	1.25< Fnrz ≤ 2.5	√	√	√	√
0	1	1	5 < Fvco ≤ 10	2.5< Fnrz ≤ 5	√	√	√	√
0	1	0	10 < Fvco ≤ 20	5< Fnrz ≤ 10	N/A	√	√	√
0	0	X	20 < Fvco ≤ 50 (Note 3)	10< Fnrz ≤ 25	N/A	√	√	√

Note 1: N/A—Not Allowed.

Note 2: Operation slightly beyond listed range boundaries may be acceptable in some applications. At or near range boundaries, range selection should be made to place the operating frequency near the UPPER boundary; e.g., use RS2 = 0, RS1 = 1, and RS0 = 0 for 10 Mb/s.

Note 3: 20 MHz < Fvco ≤ 38 MHz for 1, N codes.

FIGURE 3. Code Type Allowance Versus VCO Frequency Range

2.0 Circuit Operation (Continued)

Strobe Bit					Strobe	Window Strobe
4	3	2	1	0	Word M	T_S (Typical)
0	1	1	1	1	−15	$-0.270 \times \tau_{VCO}$
0	1	1	1	0	−14	$-0.252 \times \tau_{VCO}$
0	1	1	0	1	−13	$-0.234 \times \tau_{VCO}$
0	1	1	0	0	−12	$-0.216 \times \tau_{VCO}$
0	1	0	1	1	−11	$-0.198 \times \tau_{VCO}$
0	1	0	1	0	−10	$-0.180 \times \tau_{VCO}$
0	1	0	0	1	−9	$-0.162 \times \tau_{VCO}$
0	1	0	0	0	−8	$-0.144 \times \tau_{VCO}$
0	0	1	1	1	−7	$-0.126 \times \tau_{VCO}$
0	0	1	1	0	−6	$-0.108 \times \tau_{VCO}$
0	0	1	0	1	−5	$-0.090 \times \tau_{VCO}$
0	0	1	0	0	−4	$-0.072 \times \tau_{VCO}$
0	0	0	1	1	−3	$-0.054 \times \tau_{VCO}$
0	0	0	1	0	−2	$-0.036 \times \tau_{VCO}$
0	0	0	0	1	−1	$-0.018 \times \tau_{VCO}$
0	0	0	0	0	0	0
1	0	0	0	0	0	0
1	0	0	0	1	1	$0.018 \times \tau_{VCO}$
1	0	0	1	0	2	$0.036 \times \tau_{VCO}$
1	0	0	1	1	3	$0.054 \times \tau_{VCO}$
1	0	1	0	0	4	$0.072 \times \tau_{VCO}$
1	0	1	0	1	5	$0.090 \times \tau_{VCO}$
1	0	1	1	0	6	$0.108 \times \tau_{VCO}$
1	0	1	1	1	7	$0.126 \times \tau_{VCO}$
1	1	0	0	0	8	$0.144 \times \tau_{VCO}$
1	1	0	0	1	9	$0.162 \times \tau_{VCO}$
1	1	0	1	0	10	$0.180 \times \tau_{VCO}$
1	1	0	1	1	11	$0.198 \times \tau_{VCO}$
1	1	1	0	0	12	$0.216 \times \tau_{VCO}$
1	1	1	0	1	13	$0.234 \times \tau_{VCO}$
1	1	1	1	0	14	$0.252 \times \tau_{VCO}$
1	1	1	1	1	15	$0.270 \times \tau_{VCO}$

FIGURE 4. Window Strobe Truth Table

Customers who employ the DP8459 in a system without a MICROWIRE™ (or functionally equivalent) bus configuration and who wish to fix the synchronization window in the nominal position while deselecting the test mode need only load all-zero's into the Control Register following power-up; this may be easily achieved in some system configurations (requiring no additional hardware) by tying $\overline{CRE}$ to RG, tying CRC to ERD and tying CRD to ground, providing the necessary waveforms are present for register loading prior to the first read operation.

The DP8459 provides two pins for PLL filtering purposes, CHARGE PUMP OUTPUT (CPO) and VCO INPUT (VCOI). These provide the Customer with great flexibility in fliter design, permitting high-order filter functions for optimization of PLL lock characteristics and bit jitter rejection. For basic 3rd order applications, CPO and VCOI may be tied together (single-node) with a simple lead-lag, $C \| (R+C)$ filter tied between these pins and ground. More esoteric filter designs may be implemented if the pins are electrically separated and a two-port filter network is established between CPO, VCOI, and ground. National Semiconductor supplies initial PLL filter recommendations for the single-node configuration within this data sheet with the qualifying statement that they are very general in nature, intended primarily for production testing of static window margin, and are NOT optimized for any particular disk system. For optimum performance, the Customer should pursue a filter design which is individualized and tailored to the requirements of the specific system involved. This is particularly true for the two-port filtering technique. See *Figure 5* for initial single-node filter design recommendations.

2.0 Circuit Operation (Continued)

Code	MFM	MFM	MFM	2,7	2,7	Units
Rate	0.500	2	5	10	20	Mbit/sec
VCO freq.	1	4	10	20	40	MHz
Sync bytes	12	12	12	12	12	bytes
pulses/byte	8	8	8	4	4	flux tran's
sync length	192	48	19.2	9.6	4.8	μs
sync freq	0.500	2	5	5	10	MHz
N_{sync}	2	2	2	4	4	none
N_{max}/N_{min}	4/2	4/2	4/2	8/3	8/3	none
ζ_{min}	0.5	0.5	0.5	0.5	0.5	none
ζ_{max}	0.7	0.7	0.7	0.8	0.8	none
ζ_{sync}	0.7	0.7	0.7	0.7	0.7	none
ω_{sync}	35	144	353	606	1230	Krad/sec
C1	0.5	0.12	0.05	0.018	8200 pF	μF*
R1	82	82	82	150	150	Ω
C2	0.01 μF	2700	1000	510	200	pF

Note 1: Preamble (sync) natural frequency chosen yields phase error ≤ 0.01 radians at sync field end, given a 1% frequency step at READ GATE assertion. Rnom = Rboost = 2.4k for all above loop filter selections. HGD is tied to RG, $\overline{FLC}$ is tied to PD and CPO is tied to VCOI as well as to the loop filter components.

Note 2: Component values are listed for purposes of window specification testing and correlation. These values do not necessarily yield optimum performance in actual system applications. PLL dynamics and code characteristics are presented for Customer information and convenience only. See Section 3.1.

*Unless otherwise noted.

FIGURE 5. Test Conditions and Component Values for Static Window Truncation Testing

The DP8459 VCO is constrained at all times to operate within a frequency swing of approximately ±50% of the frequency present at the REFERENCE CLOCK input. Internal frequency detector/comparator circuitry senses when the VCO overruns the 50% boundary and forces the charge pump to move the VCO back toward the REFERENCE CLOCK frequency until the 50% constraint is again satisfied—thus preventing VCO runaway in the event of loss of lock or during extended periods where ENCODED READ DATA is not present. Additionally, this technique causes the filter node voltage to behave as if a voltage clamp were present at the Charge Pump Output, preventing the control voltage, in the event of loss of lock, from drifting outside of its operating range and inadvertently extending lock recovery time.

A special test mode feature has been incorporated into the DP8459 which allows a specific input pin to change function and act as an excitation source (substitute VCO) for clocking internal logic circuitry. When the last bit in the CONTROL REGISTER is taken to a logical ONE, the VCO is stopped, and the HGD input is redirected to act as a clock source for the VCO divider circuitry. Additionally, the Delay Line and Timing Extractor blocks are disabled when the Test Mode is entered, and thus the device will not function normally and should not be operated in this mode for purposes other than internal gate exercising. Further information regarding application of the Test Mode will be furnished at the Customer's request: contact National Semiconductor Logic Marketing Group or Logic Applications Group.

2.1 Functional Block Description

PULSE GATE

The function of the Pulse Gate within the DP8459 is twofold. First, the block contains the ECL flip-flop which captures each arriving ENCODED READ DATA bit and transmits the bit to the SYNCHRONIZED DATA output. The very high switching speed of the bit-capture ECL flip-flop minimizes the portion of window margin loss caused by flip-flop metastability at window boundaries. Second, the Pulse Gate regulates the transmission of the VCO waveform into the Phase Comparator, allowing only one VCO pulse to pass with each arriving ENCODED READ DATA pulse. See *Figure 6* for a simplified logical representation of the Pulse Gate block. The one-to-one data/VCO pulse ratio produced by the Pulse Gate permits the multiple-harmonic nature of encoded data to be accommodated by the phase/frequency comparator. During the non-Read mode or during the portion of the Read mode within which the Customer has set the $\overline{FREQUENCY\ LOCK\ CONTROL}$ pin to a logical-zero (low), the Pulse Gate is inactive (bypassed) and the VCO frequency is divided as appropriate to match the incoming frequency source (ENCODED READ DATA or the REFERENCE CLOCK input).

2.1 Functional Block Description (Continued)

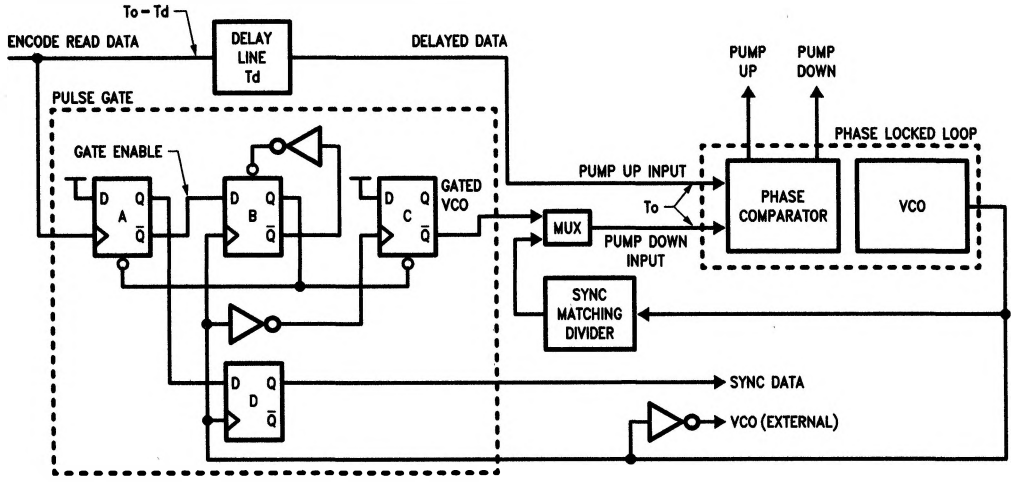

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FIGURE 6. Simplified Diagram of Window Generation Circuitry

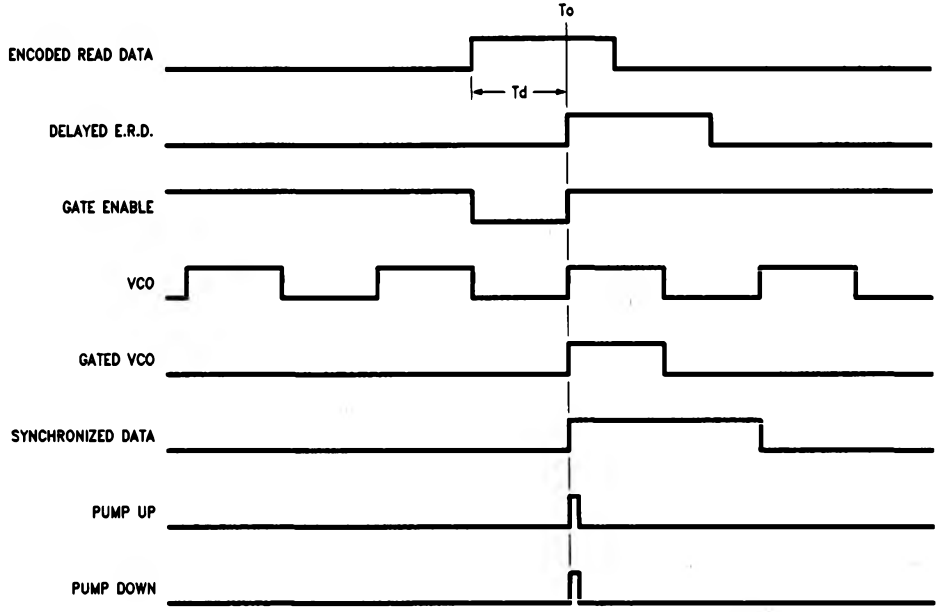

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FIGURE 7. Capture of Nominally Positioned ENCODED READ DATA Pulse

2.1 Functional Block Description (Continued)

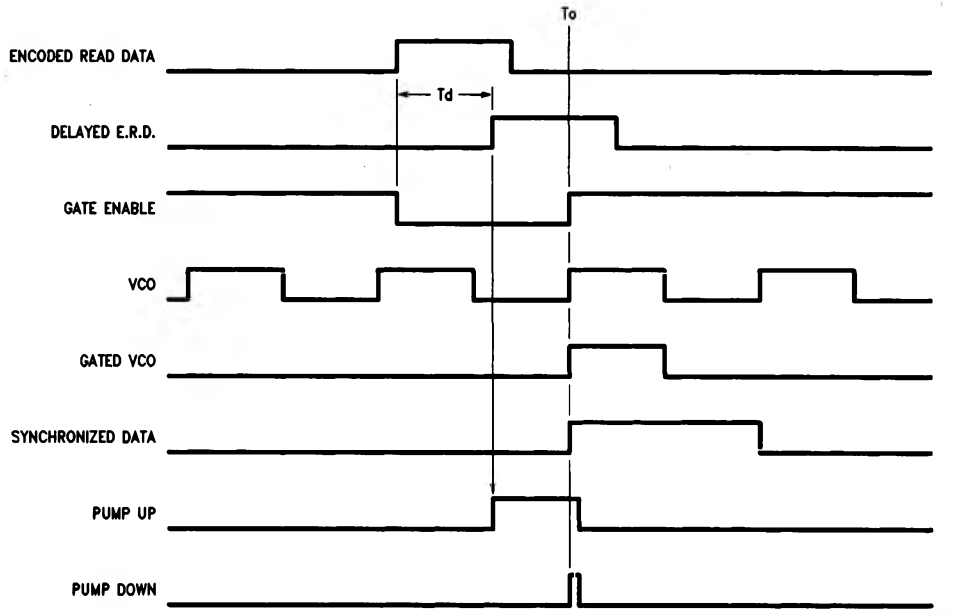

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FIGURE 8. Capture of Early-Shifted ENCODED READ DATA Pulse

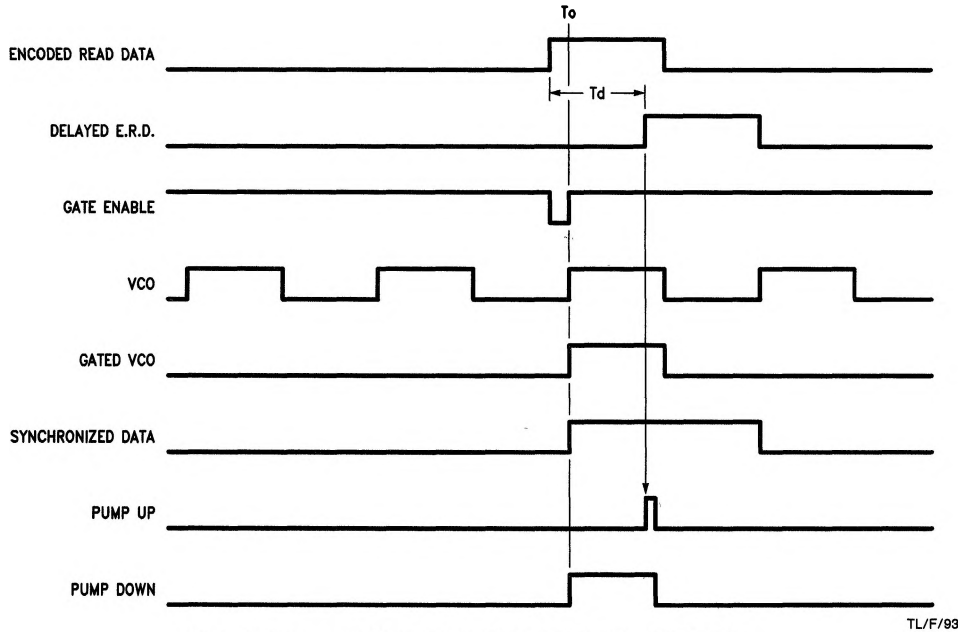

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FIGURE 9. Capture of Late-Shifted ENCODED READ DATA Pulse

2.1 Functional Block Description (Continued)

DELAY LINE

The DP8459 employs an internal silicon delay line to establish synchronization window alignment. The delay is nominally equivalent to one half of the period of the REFERENCE CLOCK waveform, and is variable in fine increments via the Control Register in order to achieve the window strobe function. The Timing Extractor circuitry derives realtive timing information soley from the REFERENCE CLOCK signal and regulates the magnitude of the delay within the Delay Line. The Delay Line thus remains insensitive to the external components associated with the extractor as well as to supply voltage, temperature, and IC process variations.

TIMING EXTRACTOR

This block extracts timing information from the REFERENCE CLOCK input for use by the variable silicon delay line. External passive components (tied to the Timing Extractor Filter pin) are associated with this block, although the accuracy of the circuit's function remains independent of the general value and tolerance of the components. The resistor-capacitor net is employed by the Timing Extractor for stabilization purposes—no monostable multivibrator (one-shot) circuitry is employed by the DP8459. Note that the performance of the delay line is directly dependent upon the accuracy of the REFERENCE CLOCK input waveform. Either a crystal reference generator or a stable servo clock source must be applied to this input. Multiplexing of the REFERENCE CLOCK waveform between read operations (within multiple data rate systems) is acceptable, although sufficient Timing Extractor stabilization time must be allowed following any perturbation at this pin before a read operation may be performed (see *Figure 10* for timing table).

PHASE COMPARATOR

The DP8459 employs a digital Phase Comparator (non-harmonic discriminator circuit) which has the capability of forcing the frequency of the PLL VCO toward the frequency of the reference input regardless of the magnitude of the frequency difference. The function of the Phase Comparator circuit can be represented in a diagrammatically simplified form as in *Figure 11*.

The Phase Comparator's action can be disabled at any time (cleared) via the $\overline{\text{COAST}}$ input pin, allowing the VCO to free-run.

CHARGE PUMP

The Charge pump is a high speed, switching, dual-gain, bi-directional current source whose current flow is controlled by the digital Phase Comparator circuit. The current pulses at the CHARGE PUMP OUTPUT (CPO) pin thus reflect the magnitude and sign of the phase error seen at the input of the Phase Comparator. The CPO pin is connected externally to a passive component network whose impedance translates the aggregate current into a voltage for the VCO INPUT while providing a low-pass filter function for the PLL. The matched source and sink current generators' operating currents are set via the $R_{NOMINAL}$ and R_{BOOST} pins, which are supplied current from V_{CC} through external resistors. The bias voltages at the $R_{NOMINAL}$ and R_{BOOST} pins are set to $0.75 \times V_{CC}$; the current into each of these pins is internally multiplied by 2 for Charge Pump use. The CPO current is defined as follows:

$$I_{CPO} = (V_{CC}/2)/R_{NOM}$$

HIGH GAIN DISABLE high (logical-one)

$$I_{CPO} = (V_{CC}/2)/(R_{NOM} \| R_{BOOST})$$

HIGH GAIN DISABLE low (logical-zero)

RFC Frequency	1	4	10	20	40	MHz
CT1	0.82	0.2	0.082	0.056	0.027	μF
RT1	68	68	68	68	68	Ω
Settling Time	192	96	19.2	9.6	4.6	μs

Values may be interpolated for intermediate data rates. Timing Extractor settling times are given which indicate time required for the DP8459 to accommodate a change of Strobe setting from nominal selection to either extreme (early/late), or vice versa, to within approximately 1% of final value.

FIGURE 10. TIMING EXTRACTOR FILTER Component Values for Various Data Rates

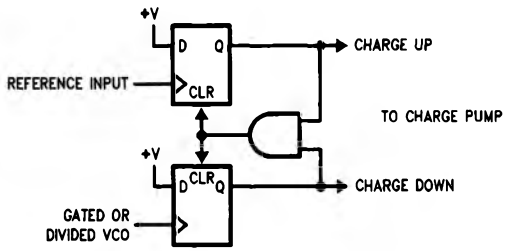

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FIGURE 11. Simplified Digital Phase-Frequency Comparator

2.1 Functional Block Description (Continued)

VOLTAGE CONTROL OSCILLATOR (VCO)

The DP8459 VCO is comprised of two portions—a self contained, high frequency oscillator (no external components) whose frequency is regulated by the voltage at the VCO INPUT pin, and a programmable modulus digital divider. The oscillator is only required to operate over approximately a 2:1 frequency range; the divider modulus is programmable in factors of 2. The two blocks work in conjunction to achieve a continuous range of equivalent VCO operating frequencies from 500 kHz to 50 MHz. (See *Figure 12*.)

CONTROL REGISTER

Within the DP8459, the Control Register is a MICROWIRE compatible, 6-bit shift register block with bits 0 through 4 employed to control the window strobe function and bit 5 employed to regulate the device test mode (see *Figures 13* and *14*). Information is serially shifted into the Control Register via the CRD and CRC (negative edge clock) pins whenever the $\overline{CRE}$ pin is active (logical-zero). When the $\overline{CRE}$ pin is inactive (logical-one), CRD and CRC are ignored. *Figure 3* shows the truth table for the VCO range select function; *Figure 4* shows the truth table for the window strobe function.

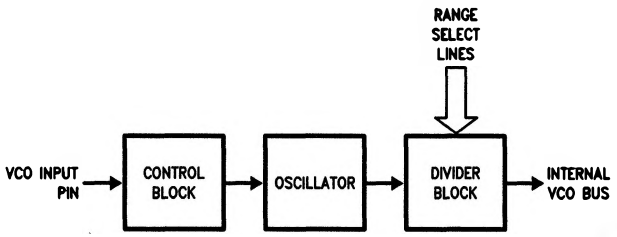

FIGURE 12

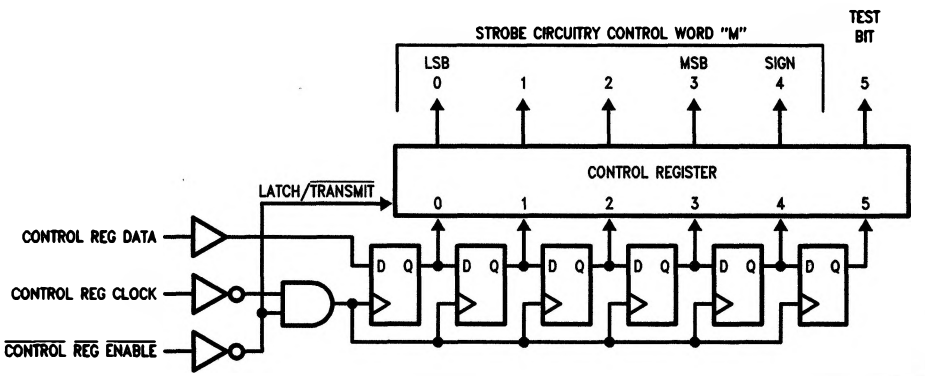

FIGURE 13. Control Register

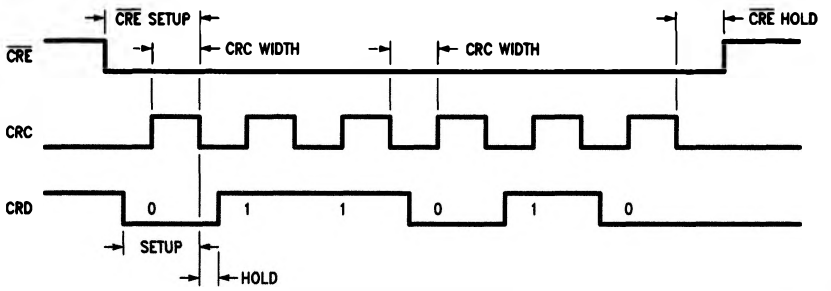

FIGURE 14. Microwire Compatible Control Register Serial Load Timing Diagram

2.1 Functional Block Description (Continued)

SYNCHRONIZATION FIELD MATCHING DIVIDER

The Synchronization field Matching Divider is a programmable modulus counter employed for implementation of the preamble frequency lock function. It is placed in the VCO feedback path to match the relative frequency of the VCO seen at the Phase Comparator to the frequency of the ENCODED READ DATA (preamble) during the read operation whenever the $\overline{\text{FREQUENCY LOCK CONTROL}}$ input is active (logic-zero). The modulus of the divider, M, is determined by the states of the SYNC PATTERN SELECT 0 and 1 inputs, as defined by the table in *Figure 15*.

Sync Pattern Select		Sync Matching Divider Modulus M	Expected Code Preamble
1	0		
0	0	1	GCR
0	1	2	MFM; 1,N
1	0	3	2,7
1	1	4	2,7

FIGURE 15. SYNC PATTERN SELECT Input Truth Table

Prior to the assertion of READ GATE, the divider is held in a known count state and is enabled at the end of the zero phase start sequence in correct phase relationship with the ENCODED READ DATA. Re-assertion (logical zero) of the $\overline{\text{FREQUENCY LOCK CONTROL}}$ pin within a read operation (following the normal $\overline{\text{FLC}}$ deassertion after lock is achieved) is permissible; however, it should be noted that the initial phase error of the Synchronization Field Matching Divider with respect to the ENCODED READ DATA at $\overline{\text{FREQUENCY LOCK CONTROL}}$ re-assertion may be as large as $M \times \tau_{VCO}$ in magnitude, possibly resulting in an extended PLL settling time.

ZERO PHASE START

The function of the zero phase start (ZPS) block is to clear the Phase Comparator and freeze the VCO in a known phase when a transition occurs at the READ GATE input (either high or low), and restart the VCO in a precise, controlled phase with respect to the newly selected input (ENCODED READ DATA or REFERENCE CLOCK ÷ 2, respectively). The ZPS circuit also resets the count state of the Synchronization field Matching Divider in anticipation of locking to specific preamble information (when frequency lock is being employed), and controls the operation of the REFERENCE CLOCK multiplexer. ZPS operation at READ GATE assertion is aimed at optimizing initial window alignment and thus minimizing initial phase step and the resulting phase lock acquisition time. ZPS is also employed at deassertion of READ GATE; however, the ZPS phase alignment for the REFERENCE CLOCK signal at READ GATE deassertion has been made less stringent than for ENCODED READ DATA at READ GATE assertion.

PREAMBLE PATTERN DETECTOR

The Preamble Pattern Detector block has a pattern-specific recognition circuit keyed to search the ENCODED READ DATA for the pattern selected at the SYNC PATTERN SELECT inputs. The pattern search begins following the assertion of READ GATE and the completion of the zero phase start sequence, and continues until approximately 32 uninterrupted ENCODED READ DATA pulses of the 1T, 2T or 3T pattern have been detected, or until 16 uninterrupted ENCODED READ DATA pulses of the 4T pattern have been detected (see specification tables). When this event occurs, the PREAMBLE DETECTED output becomes active high (logical-one). The output will then remain latched in the high state until READ GATE is deasserted. The PREAMBLE DETECTED output may be tied to the HIGH GAIN DISABLE input to regulate the gain of the PLL during the preamble lock sequence, and/or tied to the $\overline{\text{FREQUENCY LOCK CONTROL}}$ input for self-regulation of frequency acquisition in hard or pseudo-hard sectored systems.

±50% VCO FREQUENCY OFFSET DETECTOR

The Frequency Offset Detector is employed to constrain the VCO frequency swing, preventing VCO runaway associated with standard, wide-range voltage controlled oscillators. The circuitry will sense the relative difference between the REFERENCE CLOCK frequency and the VCO frequency, sending a "charge-up" signal to the Charge Pump to correct the VCO should a limit of approximately −50% in frequency differential (VCO w.r.t. REF CLOCK) be exceeded, and sending a "charge-down" signal to the Charge Pump to correct the VCO should a limit of approximately +50% in frequency differential be exceeded. The resulting voltage-clamping action at the filter node(s) also prevents out-of-range control voltage straying and thus speeds lock recovery.

SYNCHRONIZATION CLOCK OUTPUT MULTIPLEXER

This block issues the VCO signal following READ GATE assertion and completion of the zero phase start sequence, and issues the REFERENCE CLOCK input signal when the READ GATE is deasserted. Multiplexer switching is achieved without glitches. The output is intended to be used both for read and write clock purposes. (Please note output loading recommendations for this pin in Section 6.)

2.2 SPECIFICATION TABLES

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
TTL Inputs	7V
Output Voltages	7V
Input Current (R_{NOM}, R_{BOOST}, CPO, VCOI, TEF)	2 mA
Storage Temperature	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
ESD Susceptibility (Note 3)	1500V

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.00	5.25	V
T_A	Ambient Temperature		0	25	70	°C
I_{OH}	High Logic Level Output Current	SYNC CLOCK Others			−2000 −400	μA
I_{OL}	Low Logic Level Output Current (Note 1)	SYNC CLOCK Others			20 8	mA
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level Input Voltage				0.8	V
f_{NRZ}	Operating Data Rate Range		0.25		25	Mb/s
$t_{PW\text{-}RFC}$	Width of REFERENCE CLOCK, High or Low		8			ns
$t_{PW\text{-}ERD}$	Width of ENCODED READ DATA		12 High 18 Low			ns
$t_{PW\text{-}CRE}$	Width of CONTROL REGISTER ENABLE, High or Low (Note 2)		40			ns
$t_{SU\text{-}CRD}$	CONTROL REGISTER DATA Set-Up Time with Respect to CRC (Note 2)		20			ns
$t_{H\text{-}CRD}$	CONTROL REGISTER DATA Hold Time with Respect to CRC (Note 2)		10			ns
$t_{SU\text{-}\overline{CRE}}$	CONTROL REGISTER ENABLE Set-Up Time with Respect to CRC (Note 2)		20			ns
$t_{H\text{-}\overline{CRE}}$	CONTROL REGISTER ENABLE Hold Time with Respect to CRC (Note 2)		20			ns
$t_{PW\text{-}CRC}$	CONTROL REGISTER CLOCK Pulse Width Positive or Negative (Note 2)		40			ns
I_{CPIN}	Combined R_{NOM} & R_{BOOST} Input Current				1000	μA

Note 1: PUMP UP and PUMP DOWN outputs have no current sinking capability and thus are excluded from this specification.

Note 2: Parameter guaranteed by correlation to characterization data. No outgoing test performed.

Note 3: Human body model; 120 picofarads through 1.5 kΩ.

AC Electrical Characteristics Over recommended V_{CC} and operating temperature range.

Symbol	Parameter	Min	Typ	Max	Units
t_{STOP}	SYNC CLOCK Negative Transitions following READ GATE until Data Lock ZPS Sequence Begins (VCO Freezes)		2	3	—
$t_{RESTART}$	Positive ENCODED READ DATA Transitions following VCO Freeze until VCO Restarts		2		—
$t_{READ\ ABORT}$	Number of REF CLOCK Cycles following READ GATE Deactivation until REF CLOCK Lock ZPS Sequence Begins			4	—
t_T	Window Truncation (Half Window Loss); **DP8459V-10** 10 Mbit/sec (Note 1) **DP8459V-25** 20 Mbit/sec (Note 2)		 3% × τ_{VCO} 4% × τ_{VCO}	 3.0 2.5	 ns ns
ϕ Linearity	Phase Range for Charge Pump Linearity (wrt VCO)		$\pm\pi$		Radians
K_{VCO}	VCO Gain Constant	1.0 ω_O	1.2 ω_O	1.6 ω_O	Rad/Sec V
$f_{MAX\ VCO}$	VCO Maximum Frequency; RS0 = RS1 = RS2 = Logical ZERO	70			MHz
t_{SD0}	Time Skew between SYNC CLOCK Negative Edge and SYNC DATA Negative Edge	0		10	ns
t_{SD1}	Time Skew between SYNC CLOCK Negative Edge and SYNC DATA Positive Edge	0		10	ns
t_{ZPSR}	Zero Phase Start Trigger Bit Targeting Accuracy, READ GATE Activation (READ) (Note 4)		2		ns
t_{PWPC}	Width of PCT, PU or PD Outputs in Fully Stabilized Lock (ERD Free of Jitter); R-Pull-Down = 510Ω		10		ns
$\Delta f_{VCO}/f_{RFC}$	Automatic f_{VCO} Range Limiting		50		%
t_{HOLD}	SYNC CLOCK Rest Period (Logical One) at Assertion or De-Assertion of READ GATE	½		3	T_{VCO}
t_{PDT}	SCK Negative Edge to PREAMBLE DETECTED Positive Edge at End of Detection Sequence			25	ns
L_{PDT1}	Length of Valid 1T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	33	34	35	ERD Pulses
L_{PDT2}	Length of Valid 2T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	32	33	34	ERD Pulses
L_{PDT3}	Length of Valid 3T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	31	32	33	ERD Pulses
L_{PDT4}	Length of Valid 4T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	15	16	17	ERD Pulses
t_S	Window Strobe Time Step (M = Hex Value of Bits 0–3 in CONTROL REGISTER; Bit 4 = Sign Bit)		M × (1.8%) × t_{RFC}		ns
$t_{RFC-SCK1}$	Positive Transition Propagation Delay from REF CLOCK INPUT to SYNC CLOCK OUTPUT, READ GATE Low			15	ns
$t_{RFC-SCK0}$	Negative Transition Propagation Delay from REF CLOCK INPUT to SYNC CLOCK OUTPUT, READ GATE Low			15	ns

Note 1: The DP8459V-10 static window specification, t_T, applies only to the factory-tested 2,7-code data rate of 10 Mb/s (with RS0,1,2 = 010) and with the component values as listed in *Figures 5* and *10*, test configuration as shown in *Figure 23*, test procedure as shown in *Figure 24*, and strobe word M = −2. Significant variation in t_T as a percentage of the VCO period due to the use of other filters and data rates is not expected.

Note 2: The DP8459V-25 static window specification, t_T, incorporates the DP8459V-10 window specification and, in addition, the factory-tested 2,7-code data rate of 20 Mb/s (with RS0, 1, 2, = 000), with the component values as listed in *Figures 5* and *10*, test configuration as shown in *Figure 23*, test procedure as shown in *Figure 24*, and strobe word M = −3. Significant variation in t_T as a percentage of the VCO period due to the use of other filters and data rates is not expected.

Note 3: $I_{IN} = V_{CC}/(4 \times R_{IN})$. $R_{IN} = R_{NOM}$ (HGD High) or $R_{NOM}||R_{BOOST}$ (HGD Low).

Note 4: t_{ZPSR} (ZPS Read) gauges the accuracy with which the ZPS circuitry aligns the VCO to the triggering ERD bit internally (i.e., initial phase step) at the completion of a ZPS operation following READ GATE assertion.

DC Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	V_{CC}−2V	V_{CC}−1.6V		V
V_{OL}	Low Level Output Voltage (Note 4)	V_{CC} = Min, I_{OL} = Max			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−200	μA
I_O	Output Drive Current (Note 1)	V_{CC} = Max, V_O = 2.125V	−12		−110	mA
I_{CPO}	Charge Pump Output Current (K1)	100 ≤ I_{Rp} ≤ 1000 (Note 2)	1.7 I_{Rp}	2.0 I_{Rp}	2.5 I_{Rp}	μA
$I_{CPO-OFF}$	Charge Pump Output Inactive Current	100 ≤ I_{Rp} ≤ 1000 (Note 2)	−0.85		+0.85	μA
I_{VCOI}	VCOI Offset Current	VCOI Voltage 1.5V	−0.25		+0.25	μA
V_{RNOM}	Voltage across R-NOM Resistor	1.2 kΩ ≤ R-NOM ≤ 12 kΩ	Typ. −18%	0.26 V_{CC}	Typ. +18%	V
V_{RBST}	Voltage across R-BOOST Resistor	1.2 kΩ ≤ R-BOOST ≤ 12 kΩ	Typ. −18%	0.26 V_{CC}	Typ. +18%	V
I_{CC1}	Supply Current, Nominal Strobe	V_{CC} = Max (Note 3)			190	mA

Note 1: This value has been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

Note 2: $I_{Rp} = I_{NOM} + I_{BOOST}$.

Note 3: I_{CC1} is measured with the window strobe set at nominal timing (Strobe Bits 0 through 5 = 0,0,0,0,0,0); VCO operating at maximum allowed frequency within any given range selection. I_{CC} typically increases by 30 mA when the strobe is set at the maximum early position (M = −15). This is not a linear increase per step. Most of the increase occurs as the −15 step is approached. I_{CC} decreases as the window is moved late.

Note 4: PUMP UP and PUMP DOWN outputs have no current sinking capability and thus are excluded from this specification.

External Component Selection

Symbol	Parameter	Min	Typ	Max	Units
R_{NOM}	Charge Pump Nominal Operating Current Setting Resistor (Note 1)	1.2		12	kΩ
R_{BOOST}	Charge Pump Boost Current Setting Resistor (Note 1)	1.2		∞	kΩ
C_{NOM}	R_{NOM} Bypass Capacitor (Note 2)	0.01			μF
C_{BOOST}	R_{BOOST} Bypass Capacitor (Note 2)	0.01			μF
R_{PU}	PUMP UP Open Emitter Output Pull-Down Resistor	510			Ω
R_{PD}	PUMP DOWN Open Emitter Output Pull-Down Resistor	510			Ω

Note 1: The minimum allowed value for the parallel combination of R_{NOM} and R_{BOOST} is 1.2 kΩ.

Note 2: C_{NOM} and C_{BOOST} should be high quality, high frequency type.

3.0 PLL Applications: Loop Filter Design

In order to maintain greatest design flexibility for the Customer, all PLL filter components and Charge Pump gain setting elements reside external to the DP8459. All PLL dynamics are thus under the control of the system designer. The following is a brief analysis of the DP8459 PLL; Section 3.1 contains a derivation of component values based on projected requirements within an example hard disk drive system.

Figure 16 represents the DP8459 PLL in simplified form.

Mathematical gain representations for each block are:

$K_{PG} = 1/N$ Pulse Gate equivalent gain

$K_{PC} = 1/(2\pi)$ Phase Comparator gain

$K_{CP} = V_{CC}/2R_p$ Charge Pump gain where

$R_p = R_{NOM}$, HGD high;

$R_p = R_{NOM} || R_{BOOST}$, HGD low

$K_{VCO} = 1.2\ \omega_O$ VCO gain (ω_O = operating center frequency)

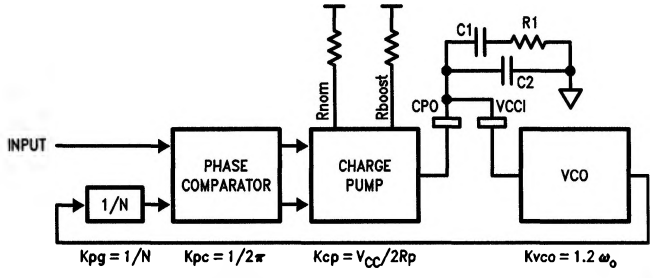

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FIGURE 16. Basic DP8459 Phase Locked Loop Block Diagram

3.0 PLL Applications: Loop Filter Design (Continued)

N is defined as the number VCO cycles per recorded ENCODED READ DATA pulse, or conversely, the ratio of the VCO frequency to the ENCODED READ DATA frequency. The aggregate block gain equation (excluding the loop filter) can be written as:

$$K_B = 1.2\, V_{CC}\, f_O/(2R_pN)$$

The impedance of the loop filter is

$$Z(s) = \frac{1}{sC_2} \| \left(\frac{1}{sC_1} + R_1\right) = \frac{1 + sR_1C_1}{sC_1(1 + C_2/C_1 + sR_1C_2)}$$

The open loop system response G(s) is given by

$$G(s) = \frac{K_B}{s} \times \frac{1 + sR_1C_1}{sC_1\,(1 + C_2/C_1 + sR_1C_2)}$$

This last equation reveals the PLL with this filter configuration is a third order system, which is typically difficult to analyze. However, if $C_2 << C_1$, it can be argued that the behavior of the third order loop closely resembles that of a second order system, allowing for a greatly simplified analysis.

If $C_2 << C_1$, the impedance Z(s) approximates to

$$\frac{1 + sR_1C_1}{sC_1}$$

The overall open loop gain (including the filter) is then

$$G(s) = \frac{K_B}{s} \times \frac{1 + sR_1C_1}{sC_1}$$

Substituting K_B into the equation,

$$G(s) = \frac{1.2\, f_o\, V_{CC}}{s2N} \times \frac{1 + sR_1C_1}{sR_pC_1}$$

$\tau_1 = R_pC_1$ and $\tau_2 = R_1C_1$ are the pole and zero, respectively, which govern the system response. The closed loop gain H(s) is

$$H(s) = \frac{\phi_{OUT}}{\phi_{IN}} = \frac{G(s)}{1 + G(s)}$$

Substituting,

$$H(s) = \frac{K_B\,(sR_1C_1 + 1)}{s^2C_1 + K_B\,(sR_1C_1 + 1)}$$

$$= \frac{(K_B/C_1)(sR_1C_1 + 1)}{s^2 + sK_BR_1 + K_B/C_1}$$

The second order characteristic equation can be written as follows:

$$s^2 + sK_BR_1 + K_B/C_1 = s^2 + s2\zeta\omega_n + \omega_n{}^2$$

Extracting the component values from these results,

$$C_1 = \frac{K_B}{\omega_n{}^2} = \frac{1.2\, V_{CC}\, f_o/(2R_pN)}{\omega_n{}^2}$$

$$R_1 = \frac{2\zeta\omega_n}{K_B} = \frac{2\zeta\omega_n}{1.2\, V_{CC}\, f_o/(2R_pN)}$$

$$C_2 \leq (1/10)\, C_1$$

Thus, one is able to select component values in accordance with specific system requirements, i.e., with given VCO center frequency (equivalent to REFERENCE CLOCK frequency), R_p (in either high or low gain mode), N (the ratio of the VCO frequency to the ENCODED READ DATA frequency), the desired natural frequency of the loop, and the desired damping ratio.

The natural frequency and the damping ratio may be extracted from the component values to determine system behavior under various conditions (differing data patterns, i.e., varying N value; high gain or low gain; read or non-read mode):

$$\omega_n = [1.2\, V_{CC}\, f_o/2R_pNC_1)]^{0.5} \quad \text{Natural frequency}$$

$$\zeta = \omega_n\, R_1C_1/2 \quad \text{Damping ratio}$$

3.1 2,7 CODE, 10 MBIT/SEC LOOP FILTER DESIGN EXAMPLE

Initial Requirements and Definitions

This example illustrates a 10 MBit/sec 2,7 hard disk system employing a 4T preamble field (recorded at 1/4 the VCO frequency, i.e., N = 4). The component derivations are not meant to produce values which will be optimum for all systems employing this data rate, code, and preamble type; this exercise is for exemplary purposes only. (See National Semiconductor Advanced Peripheral Processing Solutions Mass Storage Handbook #1, 1986, AN-413, section 3.4, pages 1-43 through 1-48 for additional information regarding disk system PLL filter design.)

Although the DP8459 provides a frequency acquisition feature intended for use within the preamble, this design example will be approached so as to achieve PLL dynamics which will avoid the cycle-slipping phenomenon frequency-lock action is normally employed to accommodate. Thus, the design will be valid both for systems which do employ frequency lock as well as for those which do not. Advantages gained by the use of frequency-lock beyond that of extended lock-in range, however, such as harmonic false lock avoidance and quadrature lock avoidance, make the use of this feature strongly advisable even with the intrinsic lock-in range achieved by design in this example.

The DP8459 is configured here with the $\overline{\text{FREQ LOCK CONTROL}}$ input tied to the PREAMBLE DETECTED output, the HIGH GAIN DISABLE input tied to the READ GATE input, and the CHARGE PUMP OUTPUT tied to the VCO INPUT pin as well as to the external loop filter components (see *Figure 17*). This establishes self-regulated frequency lock control, READ GATE regulated Charge Pump gain, and single node loop filtering.

3.0 PLL Applications: Loop Filter Design (Continued)

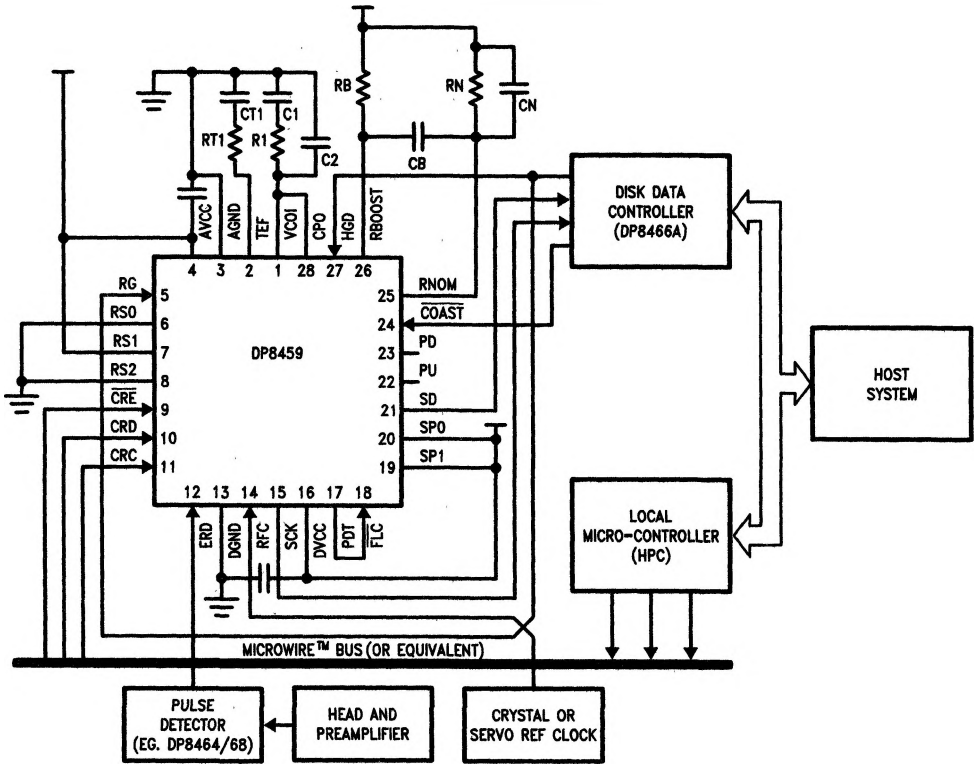

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FIGURE 17. DP8459 in a Typical System Configuration

3.0 PLL Applications: Loop Filter Design (Continued)

System constraints:

$f_{NRZ\ DATA}$ = 10 Mbit/sec

f_{VCO} = 20 MHz

$f_{REFERENCE\ CLOCK}$ = 20 MHz

Code type = ½ (2, 7)

N_{min} = 3 (highest recorded frequency)

N_{max} = 8 (lowest recorded frequency)

$N_{preamble}$ = 4 ($f_{preamble}$ = 5 MHz)

Preamble Length = 11 NRZ bytes (ESDI min.) = 8.8 μs (44 recorded pulses)

Disk formatting = pseudo hard sectored

The DP8459 provides a zero phase start function which minimizes the initial phase step encountered at the start of preamble lock acquisition and thus the phase stabilization time within the preamble is significantly reduced with respect to a fully random-phase lock sequence. However, the PLL will encounter a finite frequency step at the start of preamble acquisition due to variations in disk rotational velocity which may be as large as ±1% (more pronounced in exchangable media systems). The lock-in range of the PLL at the time of preamble acquisition must then be at least ±0.01 x $f_{preamble}$. Given that the PLL lock sequence involves only an adjustment to a frequency step, the following requirements will be set for final PLL dynamics within the filter design procedure:

1. Residual phase error θ_e at the end of the preamble (a full 11 NRZ bytes allowed for PLL stabilization) will be 2 ns or less (4% of the total synchronization window).
2. The lock-in range $\Delta\omega_L$ must be at least 1.5 times the expected frequency step range.
3. The minimum 3 dB bandwidth $\omega_{-3\ dB}$ in the data field must be twice the expected maximum mechanical vibration frequency (10 kHz).
4. The natural frequency of the loop ω_n and damping ratio ζ will be minimized in the data field in order to achieve a high level of jitter rejection. (Minimum damping ratio ζ will be 0.5 (phase margin of 52°) for adequate stability).
5. Re-lock time to the REFERENCE CLOCK will be minimized.

First, some definitions will be established. Regarding requirement #1, the equations for phase error due to a frequency step are[1]:

$$\theta_e(t) = [\Delta\omega/\omega_n]\,[1/(1-\zeta^2)^{0.5}\sin(1-\zeta^2)^{0.5}\omega_n t]\exp(-\zeta\omega_n t)$$

for $\zeta < 1$;

$$\theta_e(t) = [\Delta\omega/\omega_n]\,[\omega_n t]\exp(-\omega_n t) \text{ for } \zeta = 1;$$

$$\theta_e(t) = [\Delta\omega/\omega_n]\,[1/(\zeta^2-1)^{0.5}\sinh(\zeta^2-1)^{0.5}\omega_n t]\times \exp(-\zeta\omega_n t) \text{ for } \zeta > 1.$$

These equations are plotted in *Figure 18*. The equations for phase error due to a phase step are[1]:

$$\theta_e(t) = \Delta\theta\{\cos(1-\zeta^2)^{0.5}\omega_n t - [\zeta/(1-\zeta^2)^{0.5}]\sin(1-\zeta^2)^{0.5}\omega_n t\}\exp(-\zeta\omega_n t) \text{ for } \zeta < 1;$$

$$\theta_e(t) = \Delta\theta[1-\omega_n t]\exp(-\omega_n t) \text{ for } \zeta = 1;$$

$$\theta_e(t) = \Delta\theta\{\cosh(\zeta^2-1)^{0.5}\omega_n t - [\zeta/(\zeta^2-1)^{0.5}]\sinh(\zeta^2-1)^{0.5}\omega_n t\}\exp(-\zeta\omega_n t) \text{ for } \zeta > 1.$$

(These equations are plotted in *Figure 19* and are supplied for informational purposes only; an ideal zero phase start function would not produce a phase step at lock initiation.)

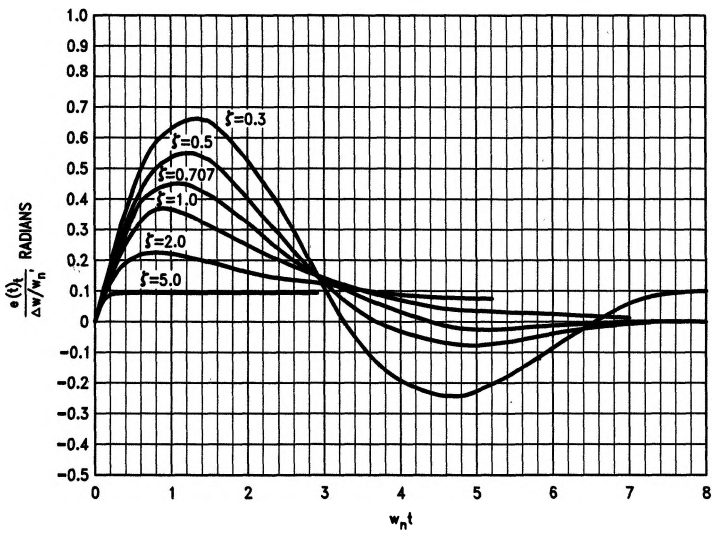

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FIGURE 18. Transient Phase-Error Versus the Dimensionless Parameter $\omega_n t$ Due to a Step in Frequency for Various Loop Damping Factors, ζ (from Ref. 4 by Permission of L. A. Hoffman)

3.0 PLL Applications: Loop Filter Design (Continued)

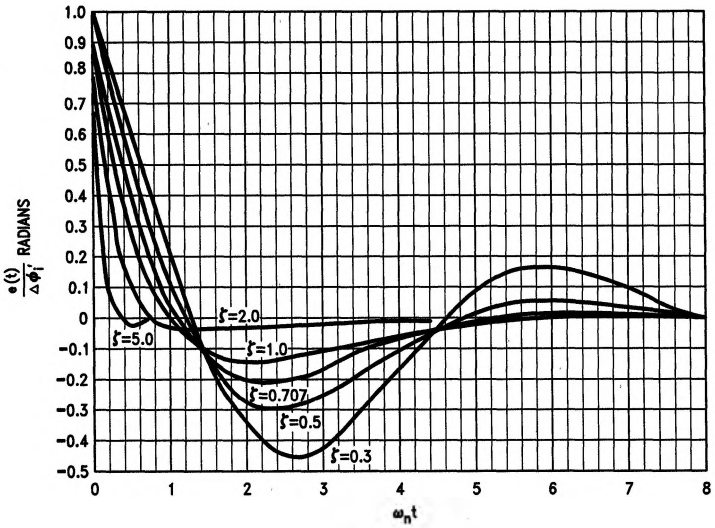

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FIGURE 19. Phase-Error Versus the Dimensionless Parameter $\omega_n t$ Due to a Step in Phase for Various Loop Damping Factors, ζ (from Ref. 4 by Permission of L. A. Hoffman)

Note that the phase error θ_e is measured with respect to the divided (or gated) VCO phase, i.e., 2π radians = N/(20 MHz) = 200 ns in this example.

Regarding requirement #2, the lock-in range (with no cycle-slipping) can be shown to be equal to the open loop transfer function multiplied by the loop filter impedance evaluated at infinite frequency[2]:

$$\Delta\omega_L \approx \pm K_B Z_f(s)|_{s \to \infty}$$

The 3 dB bandwidth for requirement #3 is defined by the equation[3]:

$$\omega_{-3\,dB} = \omega_n [2\zeta^2 + 1 + \{(2\zeta^2 + 1)^2 + 1\}^{0.5}]^{0.5}$$

Requirement #4 has been established in order to maximize the available window margin via PLL dynamics. Conceptually, window margin is preserved if the loop phase response to individually displaced bits (jitter) is not allowed to cause subsequent windows to be readily shifted from the "average" position. Any window movement from nominal position can readily degrade the window margin. It can be seen from *Figure 19* that systems employing low values of damping ratio exhibit a reduced instantaneous response to phase step and thus display improved jitter rejection with respect to higher damping ratio systems. Damping ratio, fortunately, is easily regulated by loop filter design. It also follows that a low natural frequency and its associated "slower" instantaneous phase response will assist in achieving the goal of jitter rejection. However, the minimum natural frequency limit for the PLL may actually be imposed on the system by the $\theta_e(t)$ settling time requirement, the $\Delta\omega_L$ requirement, or the $\omega_{-3\,dB}$ requirement. Whichever of these produces the highest minimum ω_n value must, by necessity, dominate in the design. The goal of minimizing the natural frequency in order to maximize jitter rejection, therefore, may have to defer to one of these other three criteria.

Requirement #5 is addressed in three ways: 1) the DP8459 itself engages the frequency discriminating action of the Phase Comparator whenever the READ GATE is deasserted and the PLL locks to the REFERENCE CLOCK signal, thus guaranteeing re-lock regardless of the initial frequency step; 2) tying the HIGH GAIN DISABLE pin to the READ GATE input places the Charge Pump in the high gain mode whenever the PLL is locked to the REFERENCE CLOCK, producing an elevated natural frequency and a more rapid locking action; 3) N = 2 whenever the READ GATE is deasserted, which, in this example, effectively increases the loop gain by another factor of 2 with respect to the gain within the preamble, where N = 4.

Determining PLL Response Characteristics

It is expected that the minimum value of ω_n will be determined by the residual phase error requirement of #1 rather

3.0 PLL Applications: Loop Filter Design (Continued)

than the lock-in range requirement of #2 or the $\omega_{-3\ dB}$ requirement of #3. This assumption will be checked at the end of the analysis. System requirements then are as follows:

1. $\theta_e(t) \leq (2\ ns) \times (2\pi\ rad/\ 200\ ns) = 0.063$ radians, where t = preamble length 8.8 μs
2. $\Delta\omega_L \approx \pm K_B Z_f(s)|_{s \to \infty} \geq 0.015 \times 5\ MHz \times 2\pi = 471$ Krad/sec
3. $\omega_{-3\ dB} = \omega_n[2\zeta^2 + 1 + \{(2\zeta^2 + 1)^2 + 1\}^{0.5}]^{0.5}$ $\geq 2 \times 10\ kHz \times 2\pi = 126$ Kr/s

Requirement #1 calls for $\theta_e(8.8\ \mu s) \leq 0.063$ radians. Damping ratio ζ varies as the inverse square root of N (see the equation for Damping Ratio in Section 3.0) such that $\zeta_{PREAMBLE} = \sqrt{(N_{MAX}/N_{PREAMBLE})} \times \zeta_{MIN} = \sqrt{2} \times 0.5 = 0.707$. Solving the appropriate equation for $\theta_e(t)$ for various values of ω_n with $\zeta = 0.707$, t = 8.8 μs and an expected frequency step of $0.01 \times 5\ MHz \times 2\pi = 314$ Kr/s:

ω_n	θ_e (8.8 μs)	$\lvert t_e \rvert$
200 Kr/s	0.606 rad	19.29 ns
300 Kr/s	0.219 rad	6.97 ns
400 Kr/s	0.056 rad	1.78 ns
500 Kr/s	0.0012 rad	0.038 ns
600 Kr/s	−0.0098 rad	0.312 ns
700 Kr/s	−0.008 rad	0.026 ns

$\theta_e(8.8\mu s)|_{400\ Kr/s} = 0.056$ radian < 0.063 radian

$t_e = 0.056$ radian $\times 200\ ns/2\pi$ radian $= 1.78\ ns < 2\ ns$

Thus 400 Kr/s is chosen as the desired natural frequency within the preamble to satisfy requirement #1.

If the assumption that $\theta_e(t)$ dominates the minimum natural frequency requirement is correct, then the $\Delta\omega_L$ requirement of #2 and the $\omega_{-3\ dB}$ requirement of #3 should be met by the ω_n obtained above. First, examining requirement #2,

$$Z_f(s)|_{s \to \infty} = R_1 \text{ } (C_2 \text{ neglected}).$$

Thus,

$$\Delta\omega_L = K_B R_1$$

Rearranging for R_1:

$$R_1 = \Delta\omega_L / K_B$$

The equation for R_1 previously derived shows

$$R_1 = 2\zeta\ \omega_n / K_B$$

Thus,

$$\Delta\omega_L / K_B = 2\zeta\omega_n / K_B$$

$$\Delta\omega_L = 2\ \zeta\omega n$$

In this case, $\omega_n = 400$ Kr/s and $\zeta = 0.707$ (preamble), thus

$\Delta\omega_L = 400\ Kr/s \times 2 \times 0.707 = 566\ Kr/s > 471\ Kr/s$

Thus, requirement #2 is met.

Examining requirement #3, where $\omega_{-3\ dB} \geq 2 \times 10\ kHz \times 2\pi$ when N equals its maximum value of 8 (minimum frequency data pattern; $\zeta = 0.5$):

$$\omega_n(min) = \omega_n(preamble) \times 1/\sqrt{(N_{MAX}/N_{PREAMBLE})}$$
$$= 400\ Kr/s \times 1/\sqrt{2} = 283\ Kr/s$$
$$\omega_{-3\ dB} = \omega_{n(min)}\ [2\zeta^2 + 1 + \{(2\zeta^2 + 1)^2 + 1\}^{0.5}]^{0.5}$$
$$= 283\ Kr/s \times 1.817 = 514\ Kr/s$$
$$514\ Kr/s \div 2\pi = 82\ kHz > 2 \times 10\ kHz$$

Thus requirements #1 through #3 are met, and #4 defers to the minimum ω_n established by #1.

Regarding requirement #5, the DP8459 has been configured externally in this example such that when the READ GATE is deasserted, the loop gain will be increased by a factor of 2 due to the Charge Pump gain switching ($R_{NOM} = R_{BOOST}$; HGD tied to RG) and by an additional factor of 2 due to the decrease in N from 4 (preamble) to a fixed internal value of 2. The resulting factor of 4 effective gain elevation results in an increase in both the natural frequency, ω_n, and the damping ratio, ζ, by $\sqrt{4} = 2$. Thus, when READ GATE is deasserted,

$$\omega_n = 2 \times 400\ Kr/s = 800\ Krad/s$$
$$\zeta = 2 \times 0.707 = 1.414$$
$$\Delta\omega_L = 2\zeta\omega_n = 2 \times 1.414 \times 800\ Krad/s = 2.3\ Mr/s$$

COMPONENT CALCULATIONS

The formulae for the filter components, derived previously, are

$$C_1 = \frac{K_B}{\omega_n^2} = \frac{1.2\ V_{CC}\ f_o/(2R_pN)}{\omega_n^2}$$

$$R_1 = \frac{2\zeta\omega_n}{K_B} = \frac{2\zeta\omega_n}{1.2\ V_{CC}\ f_o/(2R_pN)}$$

$$C_2 \leq (1/10)\ C_1$$

A 2:1 ratio of high-to-low Charge Pump gain was chosen for the derivation of R_{NOM} and R_{BOOST}. To achieve the 2:1 gain ratio, R_{NOM} must be equal to R_{BOOST} while the parallel combination $R_{NOM} \| R_{BOOST}$ must be equal to or greater than 1.2 kΩ as per specification. Note that in the equation for C_1 above, the capacitor value is inversely proportional to R_p. Thus, external field interference immunity can be achieved if C_1 is maximized through the minimizing of R_p. The selection of $R_{NOM} = R_{BOOST} = 2.4$ kΩ satisfies the requirements for the Charge Pump resistors and the gain ratio. R_p will be equal to R_{NOM} with READ GATE high, and thus

$C_1 = [1.2 \times 5 \times 20\ MHz/(2 \times 2.4k \times 4)]/(400\ Kr/s)^2$
$= 0.039\ \mu F$

R_1 can now be calculated:

$$\frac{2 \times 0.707 \times 400\ Kr/s}{1.2 \times 5 \times 20\ MHz/(2 \times 2.4k \times 4)} = 90\Omega$$

A standard value of 100Ω is chosen. Since $C_2 \leq 0.1 \times C_1$, C_2 will be chosen to be 510 pF. A table listing the dynamics of the PLL under standard operation conditions and with component values adjusted to industry standards is shown in *Figure 20.*

3.0 PLL Applications: Loop Filter Design (Continued)

Field	Preamble	Min Freq Data	Max Freq Data	Ref Clock
N	4	8	3	2
CP Gain	Low	Low	Low	High
Natural Freq. ω_n	400 Krad/s	283 Krad/s	462 Krad/s	800 Krad/s
Damping Ratio ζ	0.7	0.5	0.8	1.4

FIGURE 20. 2,7 Code, 10 Mbits/Sec Design Example PLL Dynamics

4.0 Window Margin and Bit Jitter Tolerance

A key performance specification for the DP8459 involves the integrity of the synchronization window. The **synchronization window** is defined as a continuously repeating time cell, nominally equal in span to the period of the VCO, within which an ENCODED READ DATA pulse will be recognized (captured) regardless of its position within the window (see *Figure 21*). The captured ERD bit is then transmitted to the SYNCHRONIZED DATA output on the next occurring SYNC CLOCK negative edge. The SYNCHRONIZED DATA and the SYNC CLOCK are held in a fixed, specified timing relationship for use by the data controller in deserialization and decoding. The synchronization window (with strobe setting at nominal position) is centered about the mean location of the ERD pulses via the delay line and the time-averaging action of the PLL. National Semiconductor specifies the **static window truncation** (t_T) of the DP8459 data synchronizer as the maximum expected loss of the synchronization window seen adjacent to the ideal window boundary following complete PLL stabilization with the strobe control setting at the M = −2 position (see *Figure 22*). Static lock conditions are defined as having been achieved when the PLL has been allowed to establish fully stabilized lock to a consistent preamble-type pattern of nominally positioned, non-shifted ERD pulses.

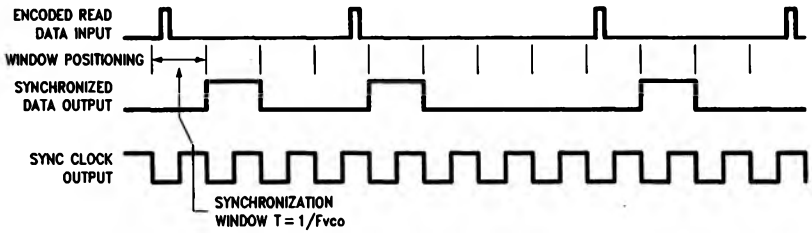

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FIGURE 21. Synchronization Window

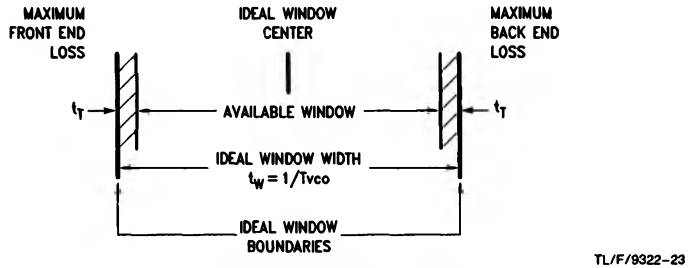

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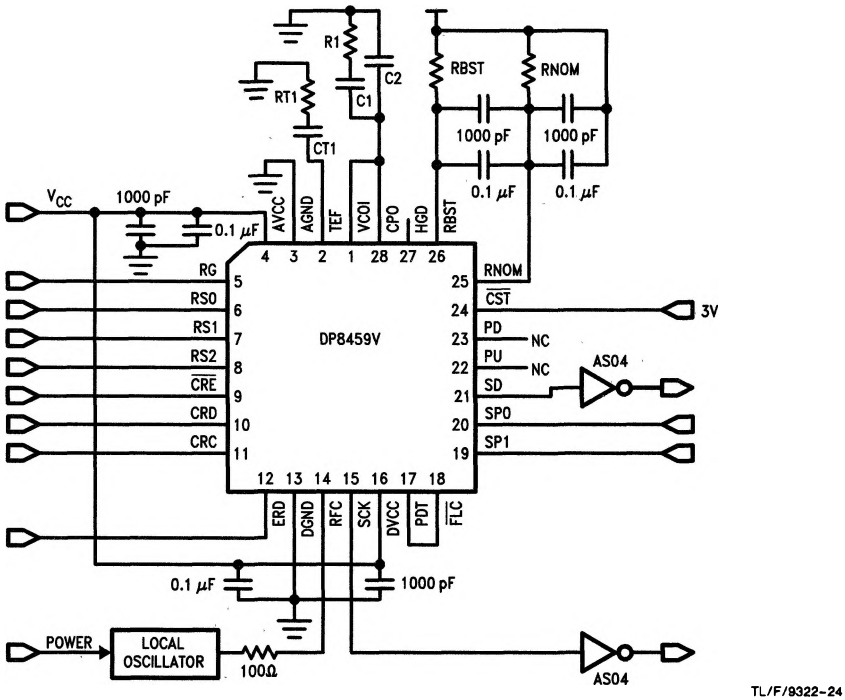
Figure 22. Window Specification Diagram

4.0 Window Margin and Bit Jitter Tolerance (Continued)

4.1 SYNCHRONIZATION WINDOW GENERATION

The DP8459 employs a pulse gate-delay line scheme in the generation of the synchronization window. *Figure 6* shows a simplified block diagram of the pulse gate and delay line circuitry coupled with the phase locked loop. All elements except the delay line are assumed to be delayless for simplicity of analysis. The pulse gate allows a single VCO edge to be transmitted to the pump down input of the phase comparator for each arriving ENCODED READ DATA pulse, while the delay line allows the ENCODED READ DATA pulse to open (enable) the pulse gate at a predetermined time (t_d) prior to the arrival of the ERD pulse at the pump up input of the phase comparator. *Figures 7, 8* and *9* show waveform diagrams of the capture of nominal, early and late ERD pulses, respectively. In normal operation where stable lock has been achieved, the time-integrating action of the PLL has established time alignment between the waveforms at the phase comparator inputs, i.e., both events occur at t_o, on average. If t_d is set equal to $0.5 \times \tau_{VCO}$, the nominal or average ERD pulse will open the pulse gate at $t_o - 0.5 \times \tau_{VCO}$, precisely the midpoint between VCO edges. ERD pulses are then free to shift to any position (ideally) between VCO edges, that is, they have an allowed displacement of $\pm 0.5\ \tau_{VCO}$ from the mean, while yet opening the pulse gate for the passing of the appropriate VCO edge to the phase comparator and at the same time being properly captured by the data synchronization latch (flip-flop D, *Figure 6*). The $\pm 0.5\ \tau_{VCO}$ region is referred to as the synchronization (capture) window.

Any variation in the value of the time delay t_d causes the time at which the pulse gate is enabled ($t_o - t_d$) to shift away from the VCO waveform midpoint, and thus produces a corresponding shift in the position of the synchronization (capture) window. This action, when done in a controlled fashion, is known as window strobing and is useful for purposes of window skew compensation, determination of system window margin, and recovery routines for non-readable data (see Section 4.3).



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Notes: SD and SCK outputs are buffered by Advanced Schottky gates to provide standardized, typical loading conditions.

CRC, CRD, CRE, RG, and ERD are driven by a pattern generator providing the appropriate sequences both to load the control register with the appropriate strobe position information and to cycle the RG and ERD test routine as per *Figure 24*.

FIGURE 23. DP8459 Window Measurement Configuration

4.0 Window Margin and Bit Jitter Tolerance (Continued)

4.2 WINDOW TRUNCATION TESTING

The DP8459 static window truncation specification is an aggregate figure within which the window margin loss contributions from all relevant blocks in the data synchronization chain are combined into the single parameter, t_T.

The preliminary DP8459 static window specification, t_T, applies only to the factory-tested data rates of 10 Mb/s (with RS0,1,2 = 010) and 20 Mb/s (with RS0,1,2 = 000), with the component values as listed for each corresponding data rate in *Figures 5,* and *10,* test configuration as shown in *Figure 23,* test procedure as shown in *Figure 24,* and strobe word M = −2 for 10 Mbits/sec and M = −3 for 20 Mbits/sec. Significant variation in t_T due to the use of other filters and data rates is not expected.

The test algorithm employed in the outgoing factory measurement (screening) of t_T emulates an ENCODED READ DATA stream consisting of a long synchronization field with a single, movable test bit at its end. This method is referred to as *static* window testing, since the window in which the test bit is inserted is fully stabilized and unable to react instantaneously to the phase step introduced by the displaced bit. The standard screening procedure employed for determining DP8459 static window truncation is divided into two portions, one which determines the location of the leading (front) window boundary and one which determines the trailing (back) window boundary. The DP8459 is made to cycle through the read operation many times as a variable bit is moved, once per read cycle, from outside the target window across the ideal leading boundary and into the window. The bit is advanced toward the center of the target window until it resides in a position where it is able to be detected a large number of times consecutively, guaranteeing VCO jitter immunity. The time displacement between the bit's valid detection position and the ideal leading window boundary is recorded as t_{Tf} (front). (This value may be negative if the actual window boundary resides outside the ideal window.) The variable bit is then placed outside the trailing window boundary and the variable bit is again moved, once per read cycle, from outside the target window across the ideal boundary and into the window. The bit continues to advanced toward the center of the recognition region until it is in a position where it is able to be read a large number of times consecutively. The time displacement between the bit's valid detection position and the ideal trailing window boundary is recorded as t_{Tb} (back). (Again, the value may be negative if the actual window boundary resides outside the ideal window due to window encroachment.) The larger (more positive) of the two (t_{Tf}, t_{Tb}) values is taken as t_T. A flow chart of the test sequence is shown in *Figure 24.* Tables of external component values used for production screening of the DP8459 at various data rates are shown in *Figures 5* and *10.*

Window truncation evaluated within data patterns containing shifted bits is a direct function of PLL dynamics which are under Customer control, and thus is neither tested nor specified.

4.3 WINDOW STROBE

The DP8459 incorporates a window strobe function capable of shifting the synchronization window either early or late with respect to its nominal position in small, specified steps. The strobe step t_S is defined as the controlled time displacement of the DP8459 synchronization window from its nominal (strobe centered) position and is typically

$$t_S = M \times [1.8\% \times \tau_{VCO}]$$

where M is the value of the strobe control word (−15 through +15; see *Figure 4*) set by the first 5 bits within the Control Register. (Note that M is equivalent to the hexidecimal value of the five strobe control bits where bits 0 through 3 are the LSB through MSB and bit 4 is the sign bit.)

The changing of the strobe value t_S is not an instantaneous event following the changing of the control word in the Control Register. The response time of the strobe control circuitry to any change in strobe setting is a function of the timing elements connected to the TIMING EXTRACTOR FILTER pin and the data rate at which the device is being operated. A finite settling time must be allowed for the delay circuitry to respond following the loading and latching of the new control word (latching occurs and strobe changes begin at de-assertion of CONTROL REGISTER ENABLE, i.e., at transition to logical ONE). It is recommended that any changes to the strobe setting be done with READ GATE deasserted and with a sufficient allowance for settling time prior to the initiation of a subsequent read operation. Approximate settling times are given in *Figure 10* for various TEF component values at specific data rates. (Please refer to AN-578 Window Strobe Function.)

4.3.1 MARGIN TESTING

The read channel window margin of a disk/tape memory system is the portion of the synchronization window remaining after the subtraction of all possible sources of degradation such as media bit shift, head-amplifier anomalies, pulse detector anomalies, cable-induced skew, synchronizer losses, and extraneous noise. The remaining margin must be sufficient to allow the system to perform with an acceptable media error rate under all operating conditions. Acceptable media error rates will vary between systems depending on ECC codes, data redundancy, and other factors. The measured value of the synchronization window margin is often used as a performance criteria for HDA (head-disk assembly) and read channel qualification, and for gauging the probability of encountering data errors on the media.

The DP8459 strobe function can be readily used to measure the window margin within a drive system. Margin tests have been most frequently employed only during outgoing factory tests of storage media systems with specialized and costly test apparatus employed for the purpose; however, the DP8459 allows media/system qualification at any time in the factory or the field during the system's operational life, given the incorporation of an appropriate margin test algorithm within the disk system controller. The algorithm may be configured first to record the most bit-interactive (shift-producing) pattern possible with the recording code being employed (eg., a repeating hex **6D B6** pattern in MFM) in an area of the media where recording density is its highest (inner-most track in constant-angular velocity or constant data rate disk systems), and secondly to read the track repeatedly while incrementally advancing the degree of window "strobe" (controlled shift) first in the early direction until the data error rate crosses a pre-determined threshold and then in the late direction until the same threshold is again crossed. The smaller of the two DP8459 window strobe measurements (either the early or the late value) determined at the error rate threshold crossing points is then equal to the read channel window margin.

4.0 Window Margin and Bit Jitter Tolerance (Continued)

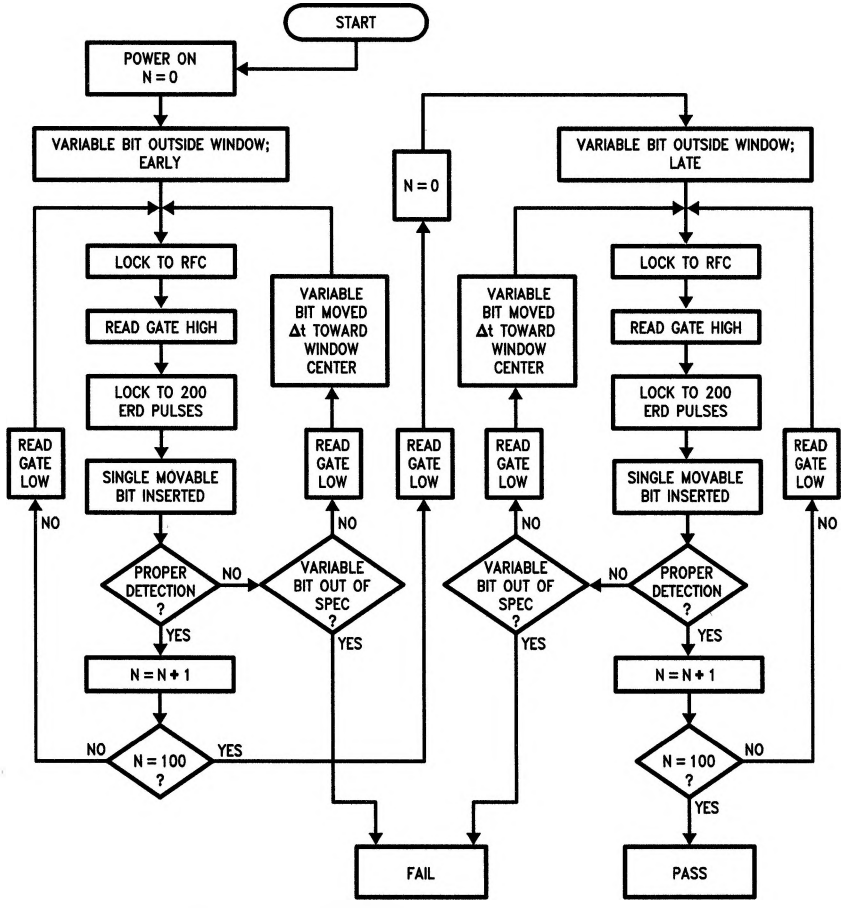

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FIGURE 24. DP8459 Static Window Truncation Test Flow Chart

4.0 Window Margin and Bit Jitter Tolerance (Continued)

4.3.2 ERROR-BOUND SECTOR/TRACK DATA RECOVERY

A standard technique exists for attempting to recover illegible data from a sector or track within a disk system which involves the re-reading of the bad data while shifting the data synchronizer window a small amount early/late with respect to the nominal position. A typical early/late strobe value for data retrieval is in the range from approximately 2% to 3% of the total window width. The strobe step size produced by the DP8459 window control circuitry easily allows for this type of data recovery procedure, and is in fact small enough to feasibly permit more than one degree of window movement within the data recovery algorithm.

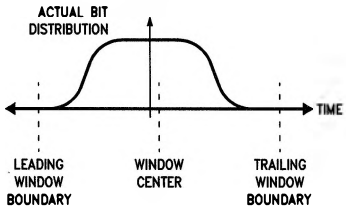
4.3.3 AUTO WINDOW ALIGNMENT (DE-SKEW ROUTINE)

It is possible to configure an intelligent drive system to employ the DP8459 strobe feature in a window auto-calibration (de-skew) routine implemented to center the detection window about the mean position of the bit distribution curve. The de-skew routine would maximize the read channel window margin and correspondingly minimize the bit error rate (BER). The auto-calibration routine would be configured as an extension of the window margin routine (Section 4.3.1), where the early and late strobe values determined at the error rate threshold crossing points would be numerically combined to determine the window center skew. For example, if at 10 Mb/s the strobe-until-error value in the "early" direction were found to be M = −8 and the "late" value M = 4, window skew would be determined as follows:

$$t_{skew} = 1.8 \times \tau_{VCO} \times [M_{early} + M_{late}]/2$$
$$= 0.9\ ns \times [-8 + 4]/2$$
$$= -1.8\ ns$$

The window has an apparent shift of 1.8 ns in the late direction. The strobe setting in the DP8459 would then be set to compensate for the skew, centering the synchronization window and maximizing the available read channel window margin. In this case, the strobe setting would be M = −2. This routine could be executed at system power-up and perhaps on a regular, specified time schedule during system operation to maintain a fine-tuning of the read channel timing characteristics under varying operating conditions (conceivably eliminating the need for an error-strobe routine).

Original Window Position



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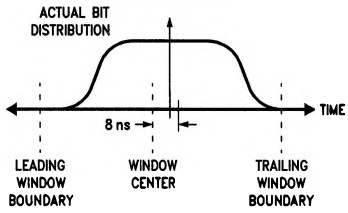
Early Strobe Window Position



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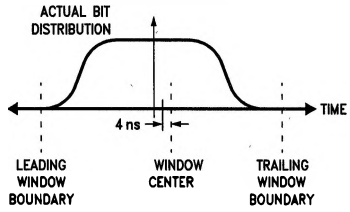
Late Strobe Window Position



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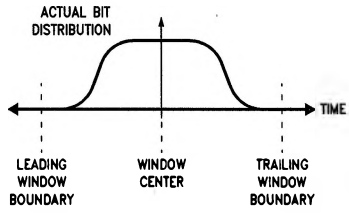
De-Skewed Window Position



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5.0 Multiple Data Rate Applications

The DP8459 may be rapidly and easily switched from one data rate to another, conceivably from its highest to its lowest specified data rate and vice versa, with a minimum of adaptation effort. This capacity facilitates the employment of the DP8459 for stepped data rate disk applications (constant density recording, or CDR), or for the employment of a single data synchronizer for multiple-media controllers as a cost and space conserving measure, e.g., allowing a controller to address tape, floppy disk and hard disk read channels on a multiplexed basis while employing a single data separator. DP8459 data rate changes require only the appropriate new REFERENCE CLOCK frequency be applied and the necessary new RANGE SELECT information be presented to the chip in cases where the Customer chooses to employ compromise loop and Timing Extractor filters. The Customer may alternatively choose to employ a transmission gate technique to multiplex between appropriate filter elements for various operating data rates should the frequencies be sufficiently different (e.g., streaming tape drive versus hard disk drive).

6.0 PC Board Layout Recommendations

The DP8459 data synchronizer circuit has been designed to minimize the sensitivities normally associated with phase locked loops which operate within digital environments, and in particular those within disk and tape memory systems. A list of recommendations and precautions is made available here for the Customer, however, such that the DP8459 environment can be optimized and the best possible performance achieved with the device.

1. A localized V_{CC} supply net or island should be established for the device and all its associated passive components, supplied by but separated from the main V_{CC} plane. The local V_{CC} net should be tied to the main V_{CC} plane at only one point and bypassed to the ground plane at that point.
2. The DP8459 V_{CC} pins should be bypassed to ground through the shortest electrical path possible between the supply pins the ground pins themselves. Bypassing should be achieved with a 0.1 μF ceramic capacitor in parallel with a 1000 pF silver mica capacitor.
3. The main digital ground plane should be used for all grounding associated with the device. Both Analog and Digital ground pins should be tied to this plane.
4. All passive components associated with the DP8459 should be located as close to their respective device pins as possible. Lead length should be minimized.
5. External passive components should be oriented so as to minimize the length of the ground-return path between the component's ground plane tie point and the DP8459 Analog ground pin.
6. In order to minimize pin parasitic capacitances, planing (supply or ground) should not be placed between device pin eyelets.
7. Digital signal lines should not be run adjacent to external passive analog components associated with the device. Digital signal lines should not be run between analog signal pins or traces associated with the device.
8. Digital input noise experience by the device should be minimized, i.e., it may be advisable to condition input waveforms in order to reduce transient noise. This may be done with a series damping resistor at the REFERENCE CLOCK input (and perhaps at the ENCODED READ DATA input) in high frequency systems. This would terminate board traces and thus prevent underdamped, noise-producing switching transients at the device inputs.
9. Digital output loading should be minimized, i.e., if outputs must drive large loads or long traces, employ buffering. Pre-termination of PC traces driven by the SYNCHRONIZED CLOCK and SYNC DATA outputs may be advisable in high frequency systems (i.e., include series resistance equivalent to the characteristic impedance of the PC board trace).
10. All unused digital output pins should be allowed to float, unconnected to any trace.
11. The device should not be located in a region of the PC board where large V_{CC} or ground plane currents are expected, or where strong electric or magnetic fields may be present. The lowest ambient noise region of the board should be chosen for device location.
12. If device socketing is desired, a low-profile, low mutual capacitance, low resistance, forced-insertion socket type should be employed.
13. Wire-wrapping should not be employed, even in an evaluation set-up.
14. Capacitors used for the loop filter, the Timing Extractor filter, and all bypassing purposes should be ultra-stable monolithic ceramic capacitors or equivalent timing quality capacitors. Silver-mica capacitors should be employed for values 1000 pF and below.
15. In order to achieve very close proximity of passive components to the DP8459 device, it is acceptable to have axial-lead resistors standing upright; however, the shorter component lead should be connected to the device pins to obviate noise induction into sensitive nodes.

7.0 Application Support

It is National Semiconductor's policy to offer and maintain a high level of direct Customer support on all of its mass storage products. National's experience in supporting the disk data memory industry has allowed the DP8459 to be designed to directly address the unique challenges of serial data synchronization within the areas of magnetic and optical media data storage and local area networks, facilitating straightforward use of the device in a diverse range of applications. In the event that questions arise regarding the use of the DP8459 or any other associated NSC mass storage device, the Customer is encouraged to contact the Logic Applications Group or Logic Marketing Group at

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Telephone (408) 721-5000

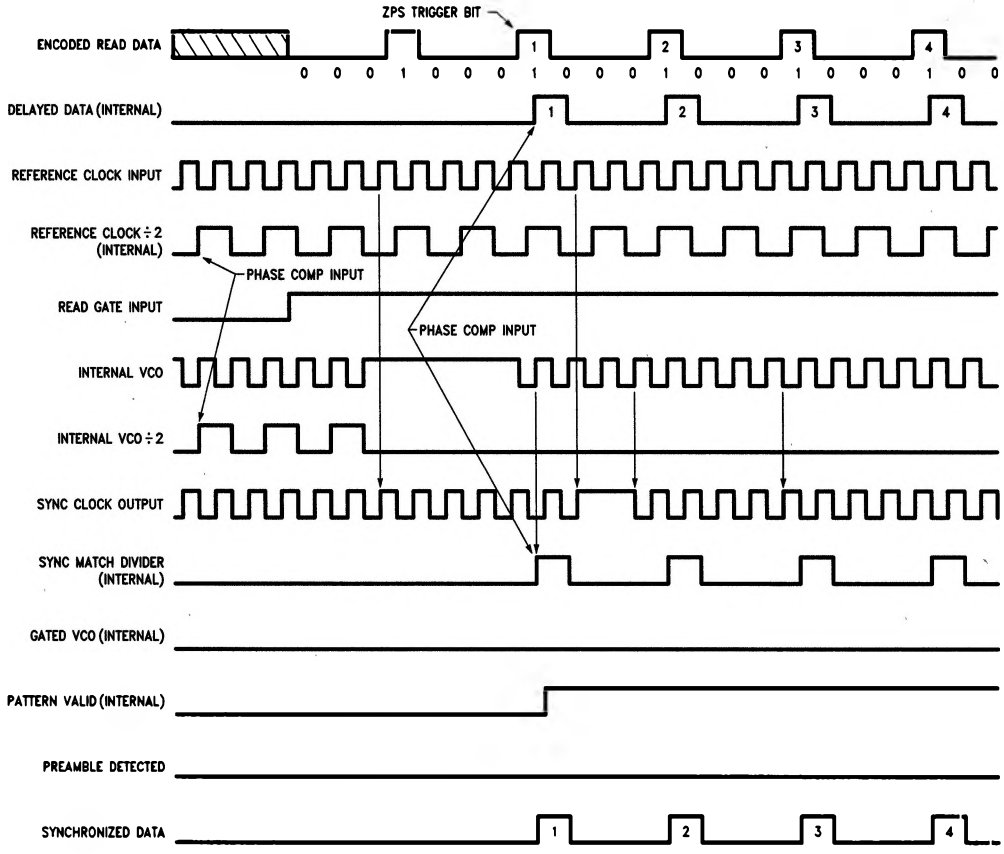

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FIGURE 25. Zero Phase Start Lock Acquistion Sequence and Start of Preamble Detection; Frequency Lock Employed, 4T Pattern

7.0 Application Support (Continued)

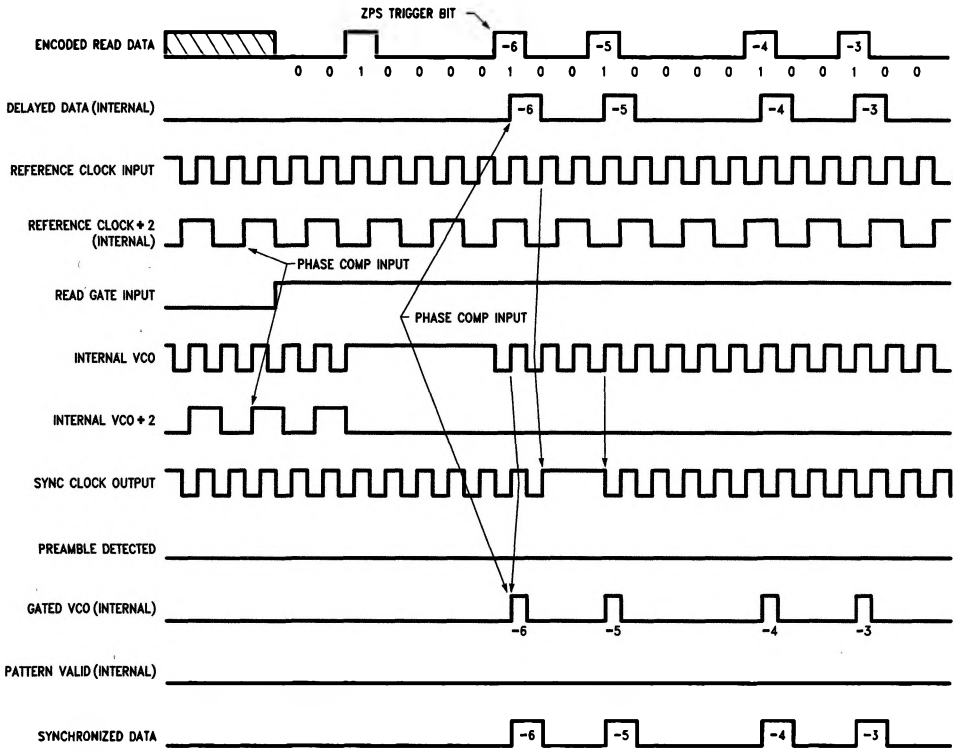

FIGURE 26. Zero Phase Start Lock Acquisition Sequence, Frequency Lock not Employed (Soft Sectoring)

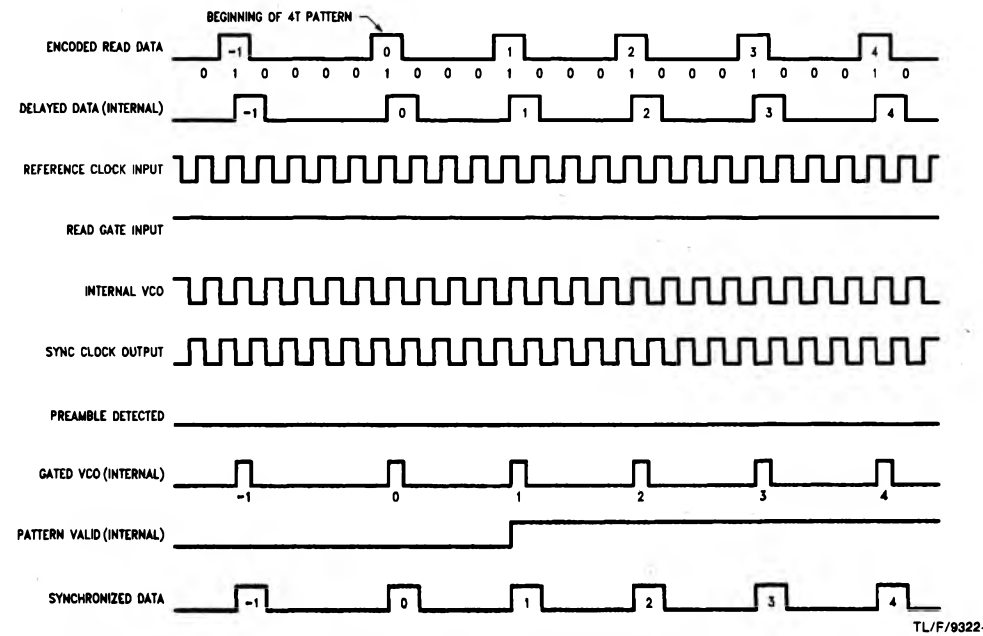

FIGURE 27. Start of Preamble Detection; 4T Pattern, Frequency Lock not Employed (Soft Sectoring)

7.0 Application Support (Continued)

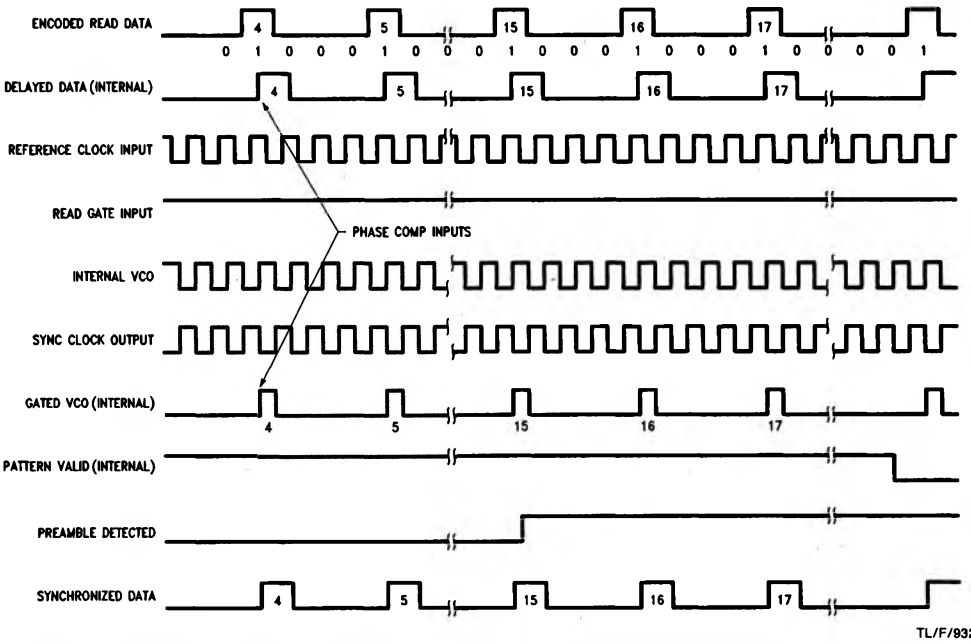

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FIGURE 28. Occurrance of Preamble Detection; 4T Pattern, Frequency Lock not Employed (Soft Sectored)

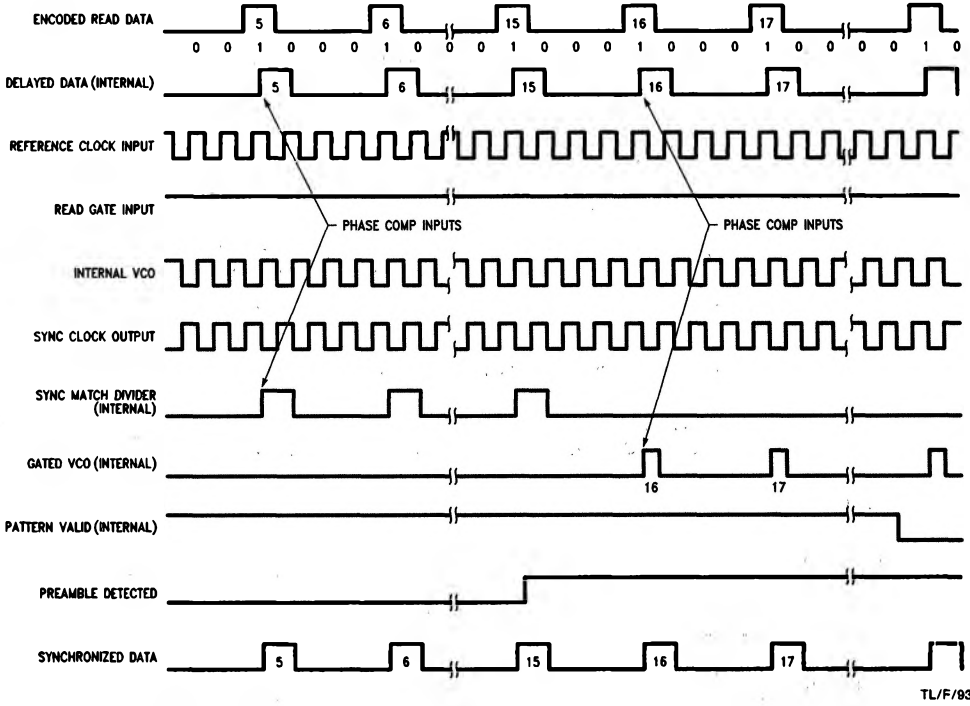

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FIGURE 29. Occurrance of Preamble Detection, Frequency Lock Employed

7.0 Application Support (Continued)

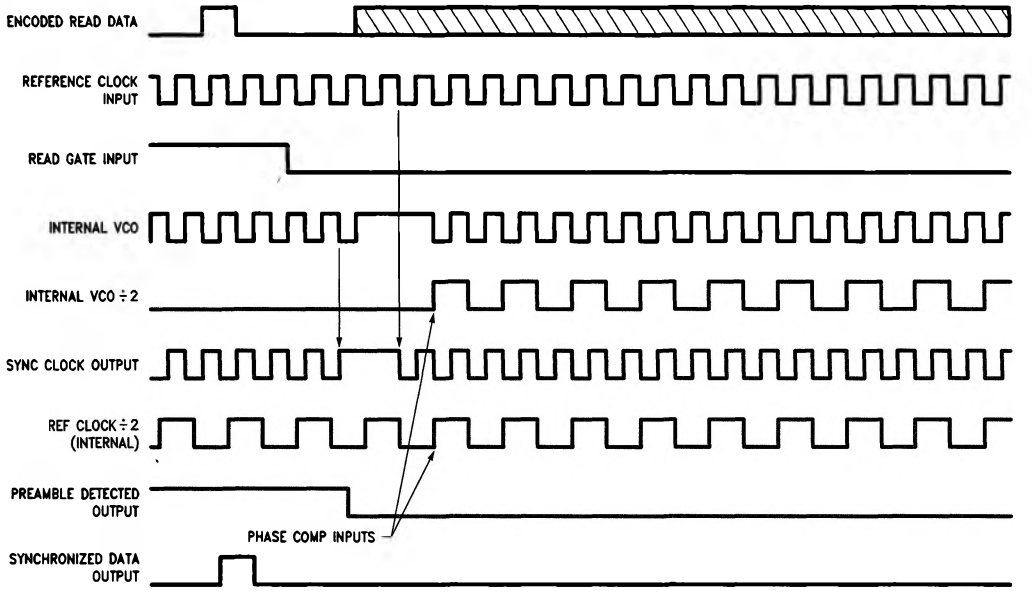

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FIGURE 30. End of Read Cycle; REFERENCE CLOCK Lock Sequence

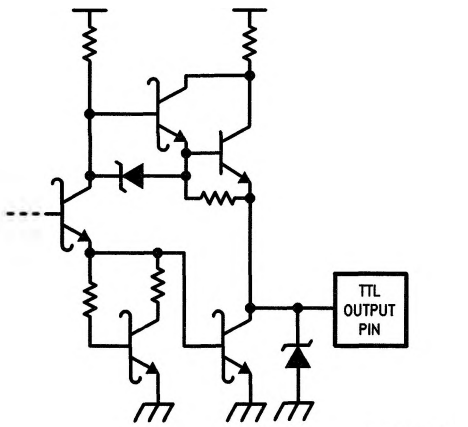

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FIGURE 31. Typical TTL Digital Output

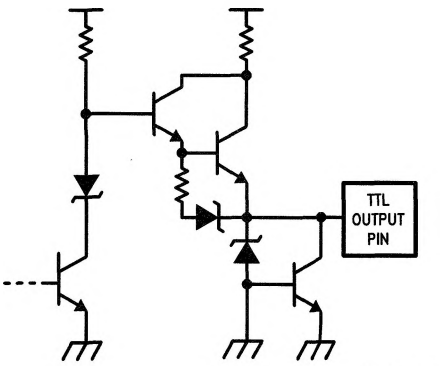

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FIGURE 32. Open Emitter TTL Output (PU and PD Outputs)

7.0 Application Support (Continued)

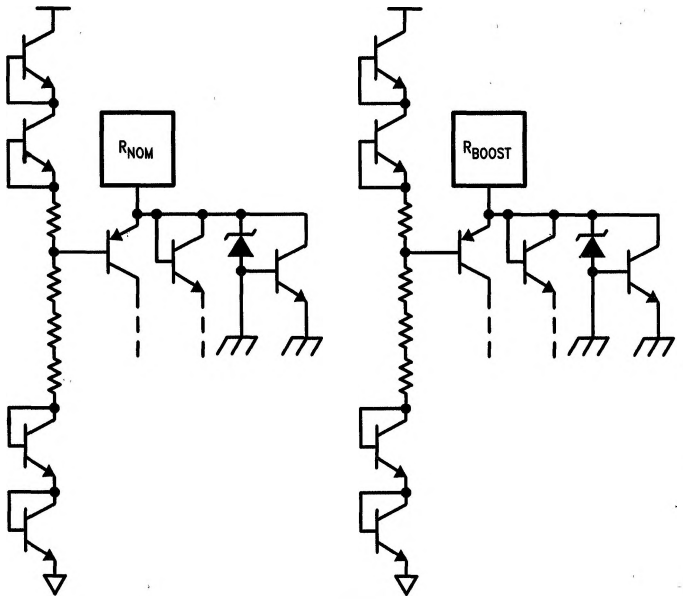

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FIGURE 33. $R_{NOMINAL}$ and R_{BOOST} Pin Configurations

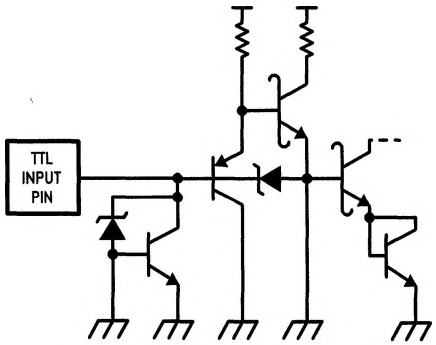

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FIGURE 34. Typical TTL Digital Input

7.0 Application Support (Continued)

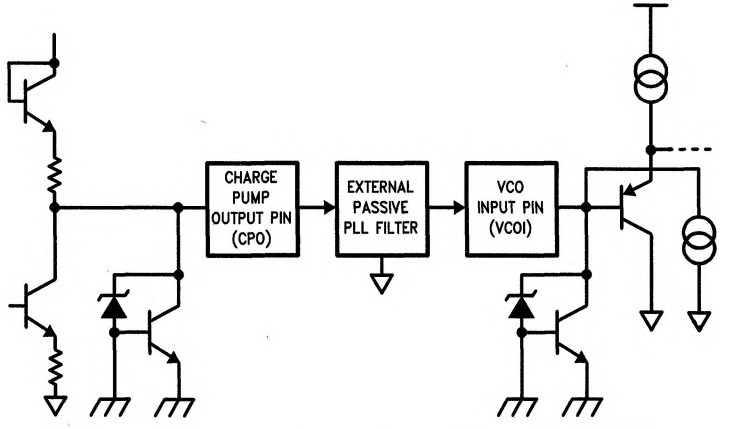

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FIGURE 35. Charge Pump Output and VCO Input Circuit Configurations

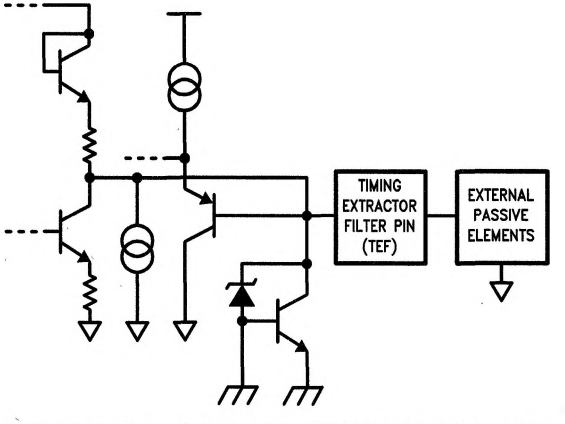

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FIGURE 36. Timing Extractor Filter Pin Circuit Configurations

References

1. *Phaselock Techniques*, Floyd M. Gardner, Second Edition, John Wiley & Sons, 1979, pp. 48.

2. ibid, pp. 70.

3. ibid, pp. 14.

4. *Receiver Design and the Phase Locked Loop*, L.A. Hoffman, Aerospace Corporation, El Segundo, Ca., May 1963.