

±3-A HIGH-EFFICIENCY PWM POWER DRIVER

FEATURES

- **±3-A Maximum Output Current**
- **Low Supply Voltage Operation: 2.8 V to 5.5 V**
- **High Efficiency Generates Less Heat**
- **Over-Current and Thermal Protection**
- **Fault Indicators for Over-Current, Thermal and Under-Voltage Conditions**
- **Two Selectable Switching Frequencies**
- **Internal or External Clock Sync**
- **PWM Scheme Optimized for EMI**
- **9×9 mm PowerPAD™ Quad Flatpack**

APPLICATIONS

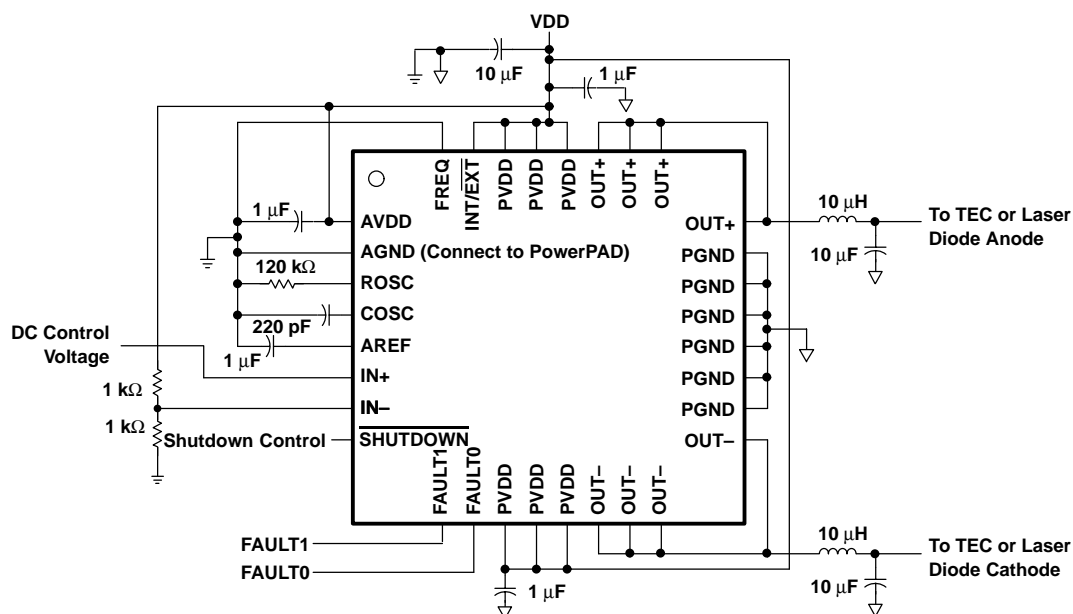
- **Thermoelectric Cooler (TEC) Driver**
- **Laser Diode Biasing**

DESCRIPTION

The DRV591 is a high-efficiency, high-current power amplifier ideal for driving a wide variety of thermoelectric cooler elements in systems powered from 2.8 V to 5.5 V. PWM operation and low output stage on-resistance significantly decrease power dissipation in the amplifier.

The DRV591 is internally protected against thermal and current overloads. Logic-level fault indicators signal when the junction temperature has reached approximately 130°C to allow for system-level shutdown before the amplifier's internal thermal shutdown circuitry activates. The fault indicators also signal when an over-current event has occurred. If the over-current circuitry is tripped, the DRV591 automatically resets (see application information section for more details).

The PWM switching frequency may be set to 500 kHz or 100 kHz depending on system requirements. To eliminate external components, the gain is fixed at approximately 2.3 V/V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

DRV591

SLOS389A – NOVEMBER 2001– REVISED MAY 2002



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

	DRV591	UNIT
Supply voltage, AVDD, PVDD	–0.3 to 5.5	V
Input voltage, V _I	–0.3 to V _{DD} + 0.3	V
Output current, I _O (FAULT0, FAULT1)	1	mA
Continuous total power dissipation	See Dissipation Rating Table	
Operating free-air temperature range, T _A	–40 to 85	°C
Operating junction temperature range, T _J	–40 to 150	°C
Storage temperature range, T _{stg}	–65 to 165	°C

⁽¹⁾ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, AVDD, PVDD		2.8	5.5	V
High-level input voltage, V _{IH}	FREQ, INT/EXT, SHUTDOWN, COSC	2		V
Low-level input voltage, V _{IL}	FREQ, INT/EXT, SHUTDOWN, COSC		0.8	V
Operating free-air temperature, T _A		–40	85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ _{JA} ⁽¹⁾ (°C/W)	Θ _{JC} (°C/W)	T _A = 25°C POWER RATING
VFP	29.4	1.2	4.1 W

⁽¹⁾ This data was taken using 2 oz trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in × 3 in PCB.

ORDERING INFORMATION

T _A	PowerPAD QUAD FLATPACK (VFP)
–40°C to 85°C	DRV591VFP ⁽¹⁾

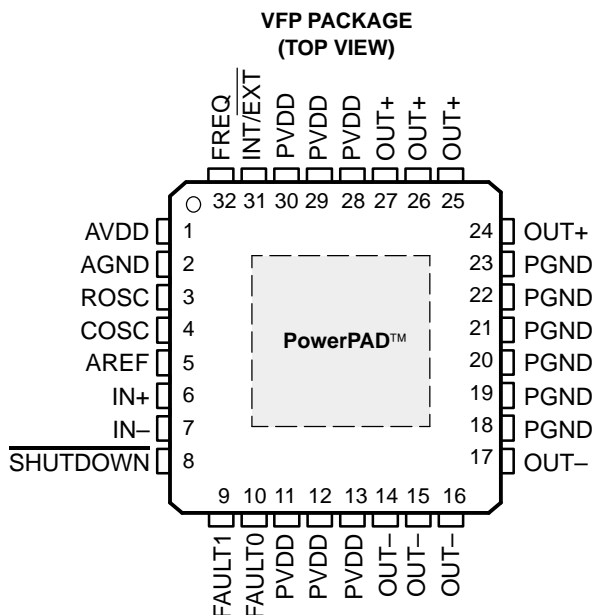
⁽¹⁾ This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., DRV591VFP_R).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OO}	Output offset voltage (measured differentially)	V _I = V _{DD} /2,	I _O = 0 A		14	100	mV
I _{IH}	High-level input current	V _{DD} = 5.5V,	V _I = V _{DD}			1	μA
I _{IL}	Low-level input current	V _{DD} = 5.5V,	V _I = 0 V			1	μA
V _n	Integrated output noise voltage	f = <1 Hz to 10 kHz			40		μV
V _{ICM}	Common-mode voltage range	V _{DD} = 5 V		1.2		3.8	V
		V _{DD} = 3.3 V		1.2		2.1	
A _V	Closed-loop voltage gain			2.1	2.34	2.6	V/V
Full power bandwidth				60			kHz
V _O	Voltage output (measured differentially)	I _O = ±1 A, r _{ds(on)} = 65 mΩ, V _{DD} = 5 V		4.87			V
		I _O = ±3 A, r _{ds(on)} = 65 mΩ, V _{DD} = 5 V		4.61			
r _{DS(on)}	Drain-source on-state resistance	V _{DD} = 5 V, I _O = 4 A, T _A = 25°C	High side	25	60	95	mΩ
			Low side	25	65	95	
		V _{DD} = 3.3 V, I _O = 4 A, T _A = 25°C	High side	25	80	140	mΩ
			Low side	25	90	140	
Maximum continuous current output				3			A
Status flag output pins (FAULT0, FAULT1) Fault active (open drain output)		Sinking 200 μA		0.1			V
External clock frequency range		For 500 kHz operation		225	250	275	kHz
		For 100 kHz operation		45	50	55	
I _q	Quiescent current	V _{DD} = 5 V, No load or filter		2	6.2	12	mA
		V _{DD} = 3.3 V, No load or filter		2	4.6	8	
I _q (SD)	Quiescent current in shutdown mode	V _{DD} = 5 V, SHUTDOWN = 0.8 V		0	0.1	50	μA
Output resistance in shutdown		SHUTDOWN = 0.8 V		2			kΩ
Power-on threshold				1.7	2.8		V
Power-off threshold				1.6	2.6		V
Thermal trip point		FAULT0 active		130			°C
Z _I	Input impedance (IN+, IN–)			100			kΩ

PIN ASSIGNMENTS



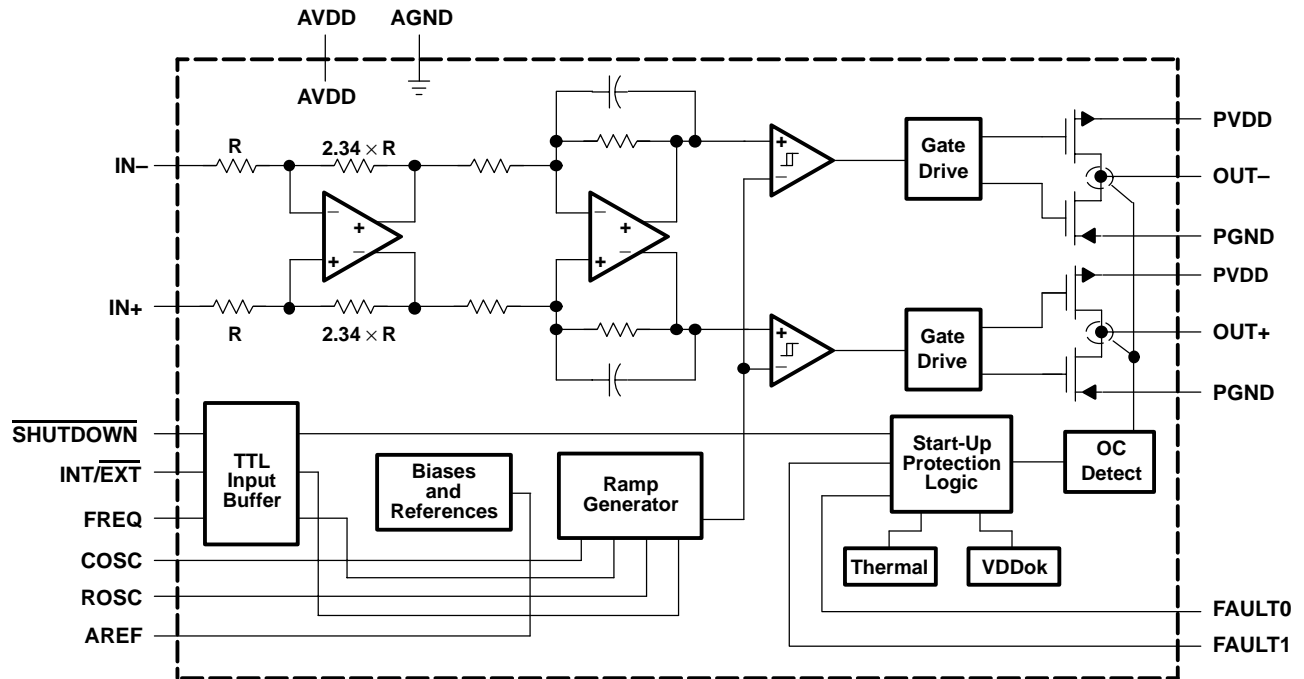
DRV591

SLOS389A – NOVEMBER 2001– REVISED MAY 2002

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	2		Analog ground
AREF	5	O	Connect 1 μ F capacitor to ground for AREF voltage filtering
AVDD	1	I	Analog power supply
COSC	4	I	Connect capacitor to ground to set oscillation frequency (220 pF for 500 kHz, 1 nF for 100 kHz) when the internal oscillator is selected; connect clock signal when an external oscillator is used
FAULT0	10	O	Fault flag 0, low when active open drain output (see application information)
FAULT1	9	O	Fault flag 1, high when active open drain output (see application information)
FREQ	32	I	Selects 500 kHz switching frequency when a TTL logic low is applied to this terminal; selects 100 kHz switching frequency when a TTL logic high is applied
IN $\bar{}$	7	I	Negative differential input
IN+	6	I	Positive differential input
INT/EXT $\bar{}$	31	I	Selects the internal oscillator when a TTL logic high is applied to this terminal; selects the use of an external oscillator when a TTL logic low is applied to this terminal
OUT $\bar{}$	14, 15, 16, 17	O	Negative bridge-tied load (BTL) output (4 pins)
OUT+	24, 25, 26, 27	O	Positive bridge-tied load (BTL) output (4 pins)
PGND	18, 19, 20, 21, 22, 23		High-current ground (6 pins)
PVDD	11, 12, 13, 28, 29, 30	I	High-current power supply (6 pins)
ROSC	3	I	Connect 120-k Ω resistor to AGND to set oscillation frequency (either 500 kHz or 100 kHz). Not needed if an external clock is used.
SHUTDOWN $\bar{}$	8	I	Places the amplifier in shutdown mode when a TTL logic low is applied to this terminal; places the amplifier in normal operation when a TTL logic high is applied

FUNCTIONAL BLOCK DIAGRAM



DRV591

SLOS389A – NOVEMBER 2001– REVISED MAY 2002

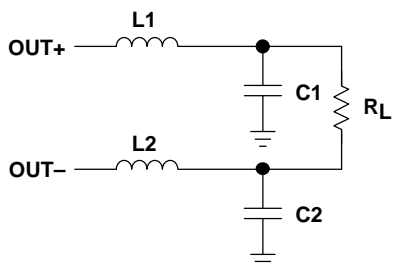
TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficiency	vs Load resistance	2, 3
$r_{DS(on)}$ Drain-source on-state resistance	vs Supply voltage	4
	vs Free-air temperature	5
	vs Free-air temperature	6
	vs Supply voltage	7
I_q Supply current	vs Supply voltage	7
PSRR Power supply rejection ratio	vs Frequency	8, 9
Closed loop response		10, 11
I_O Maximum output current	vs Output voltage	12
	vs Ambient temperature	13
V_{IO} Input offset voltage	Common-mode input voltage	14, 15

TEST SET-UP FOR GRAPHS

The LC output filter used in Figures 2, 3, 8, and 9 is shown below.



L1, L2 = 10 μ H (part number: CDRH104R, manufacturer: Sumida)
C1, C2 = 10 μ F (part number: ECJ-4YB1C106K, manufacturer: Panasonic)

Figure 1. LC Output Filter

TYPICAL CHARACTERISTICS

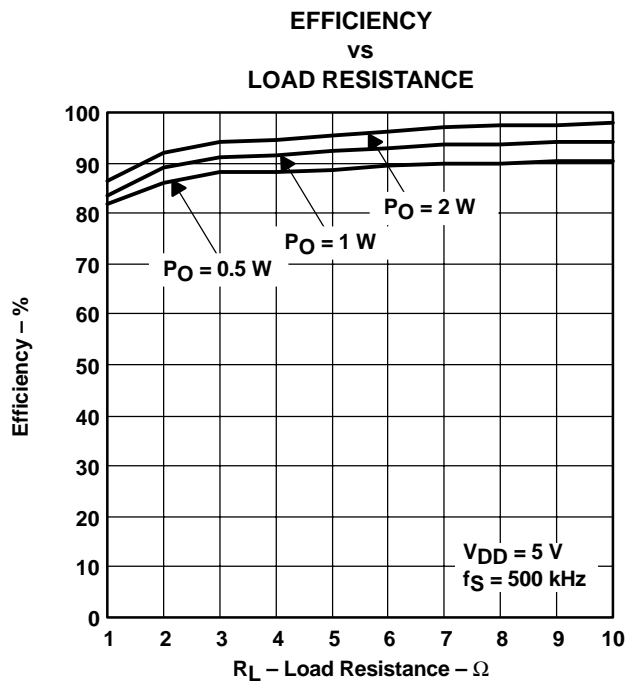


Figure 2

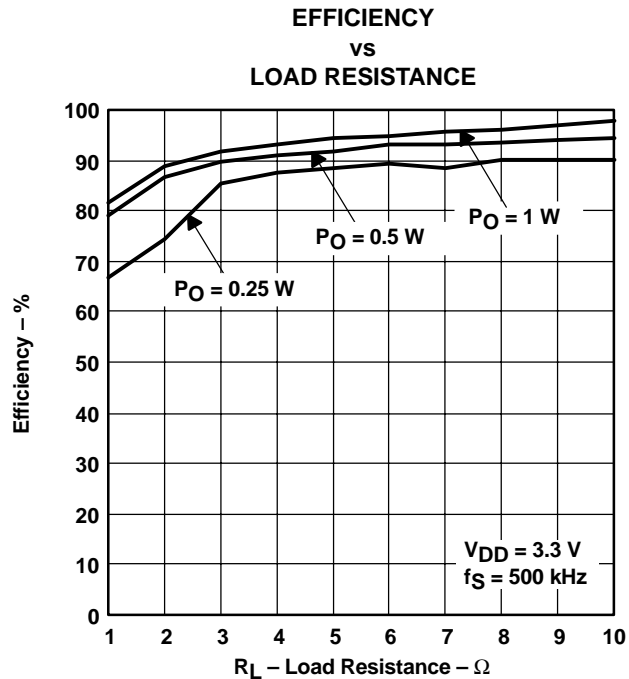


Figure 3

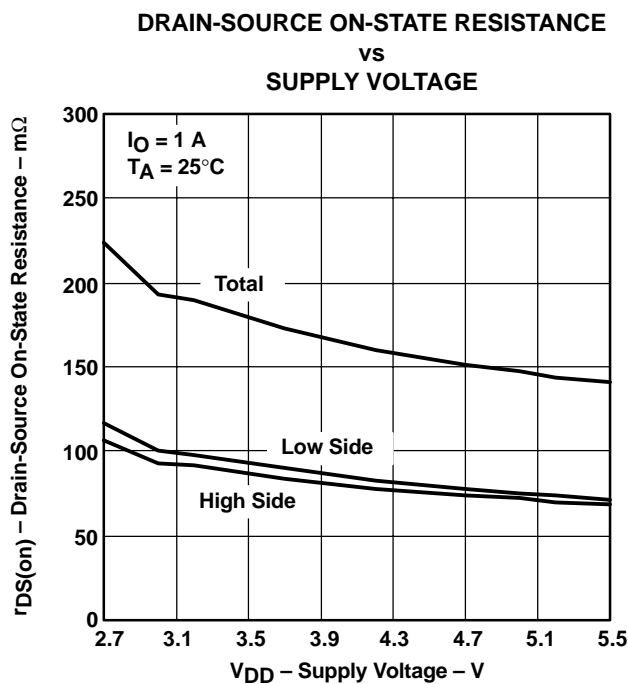


Figure 4

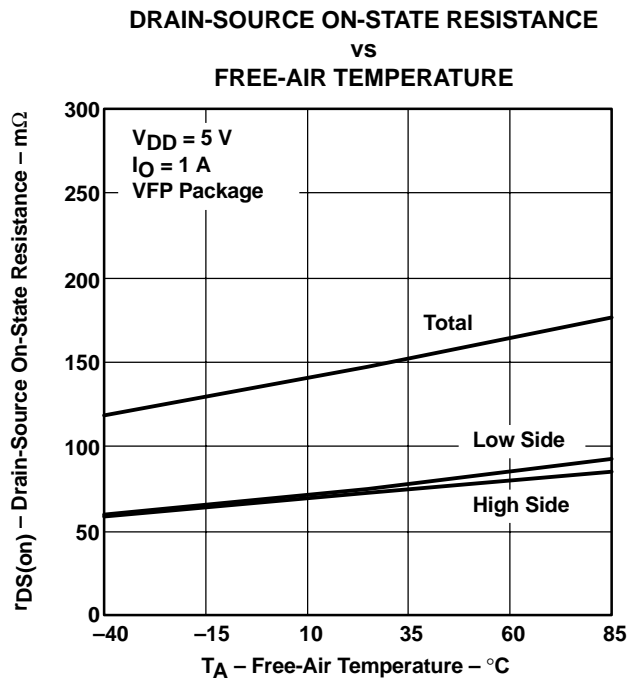


Figure 5

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

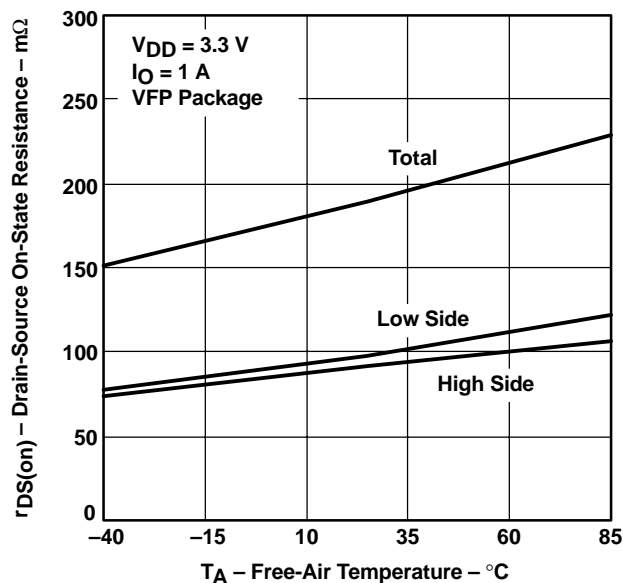


Figure 6

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

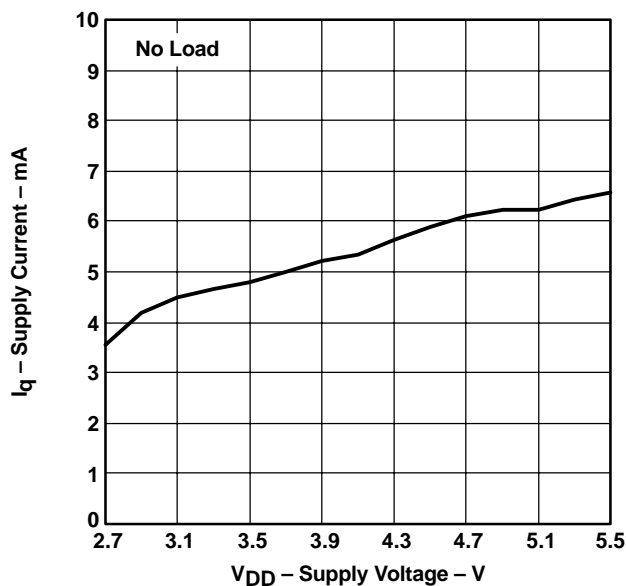


Figure 7

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

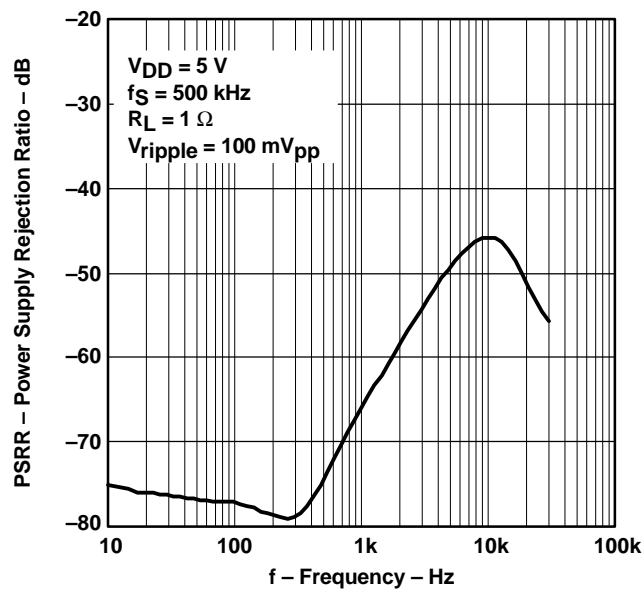


Figure 8

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

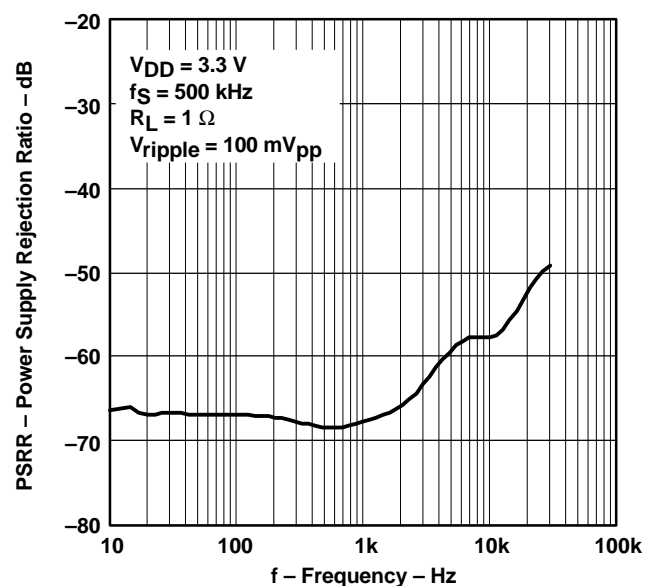


Figure 9

TYPICAL CHARACTERISTICS

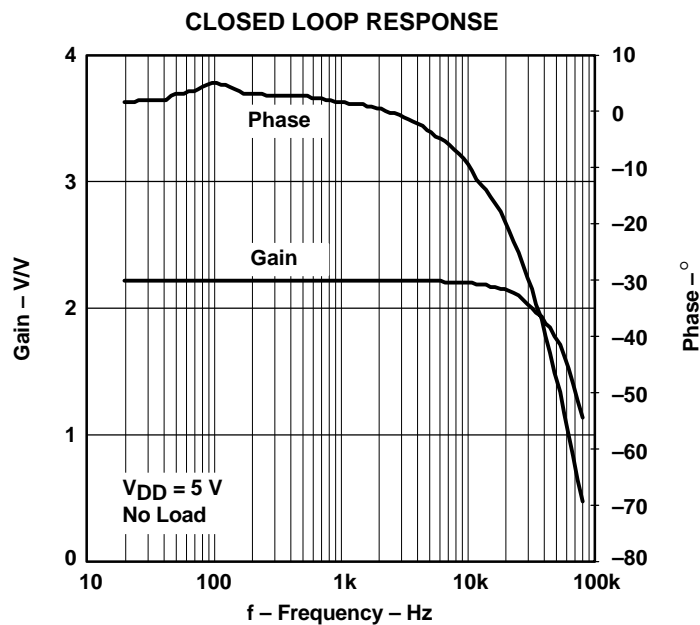


Figure 10

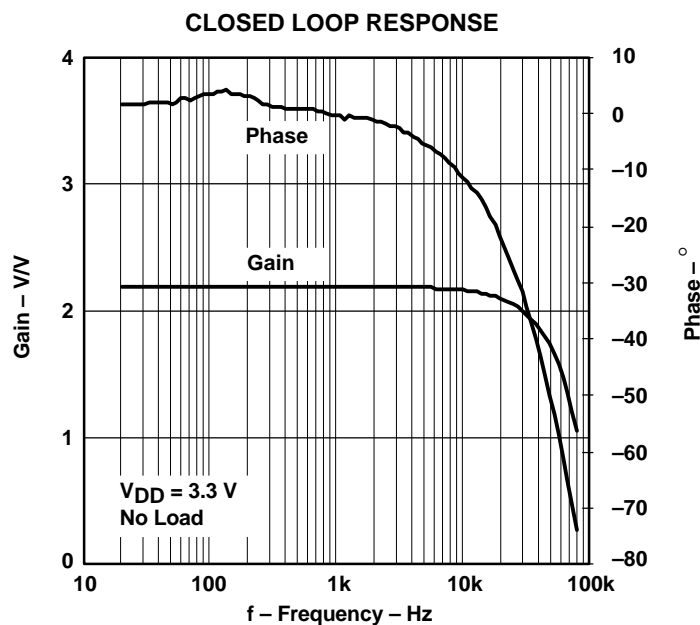
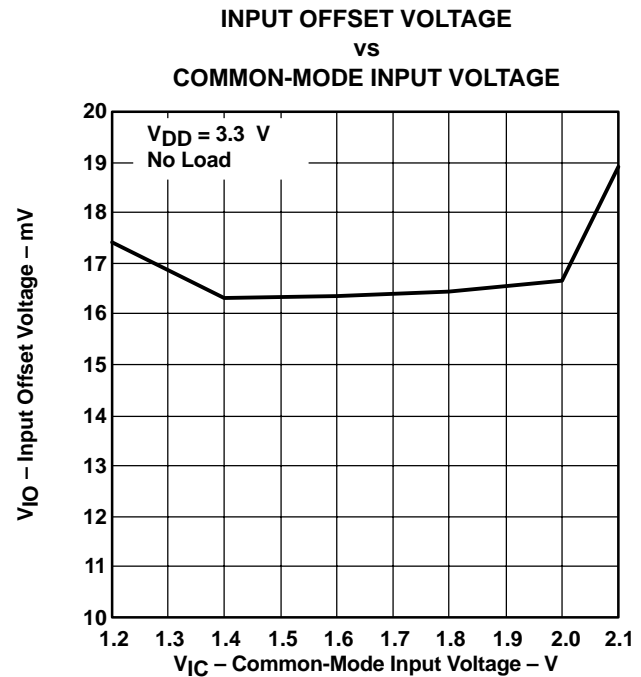
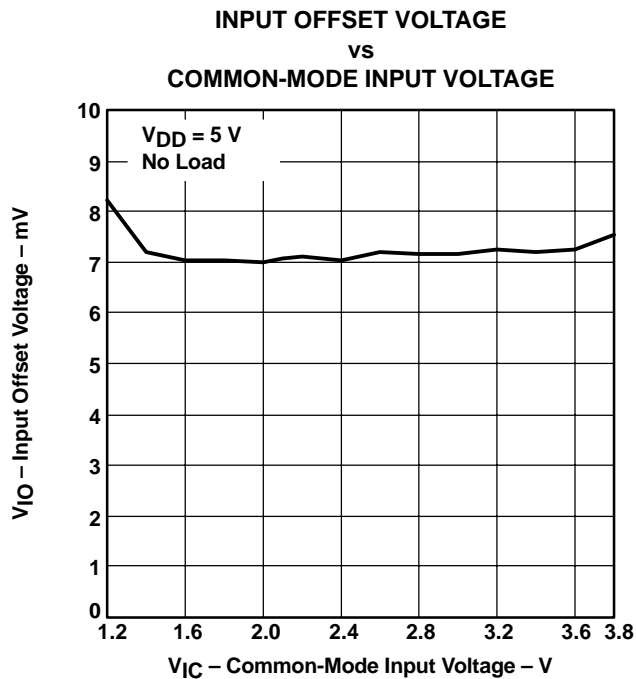
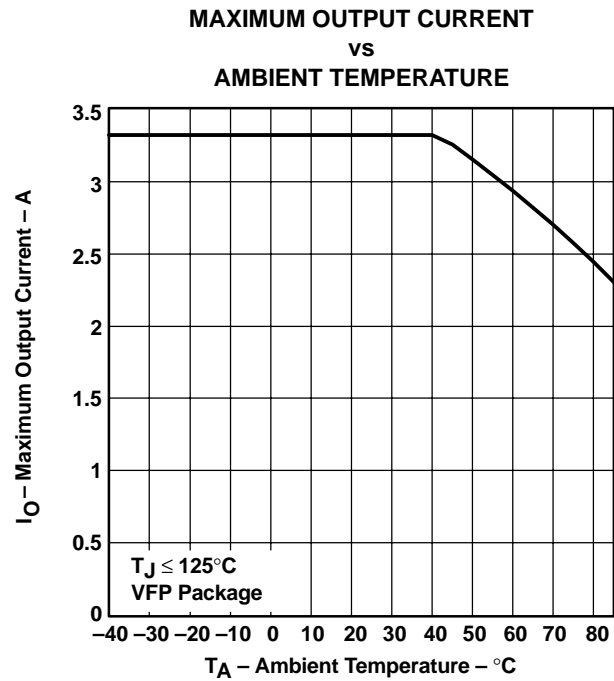
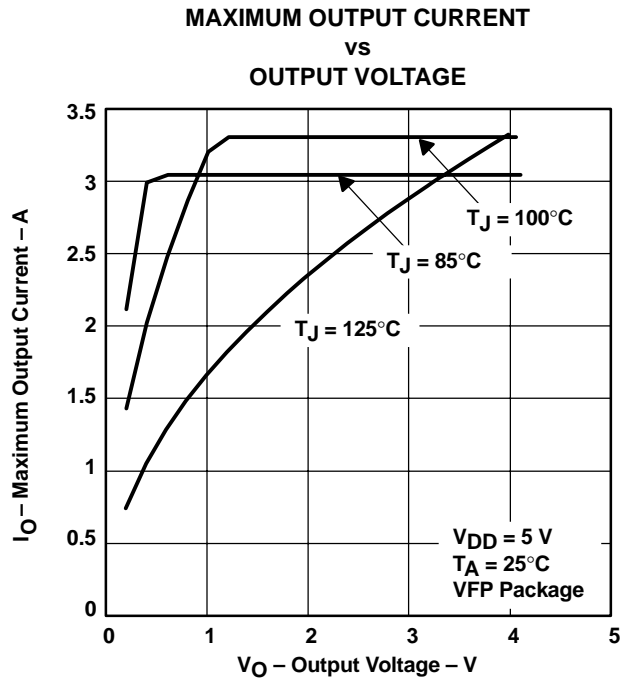


Figure 11

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

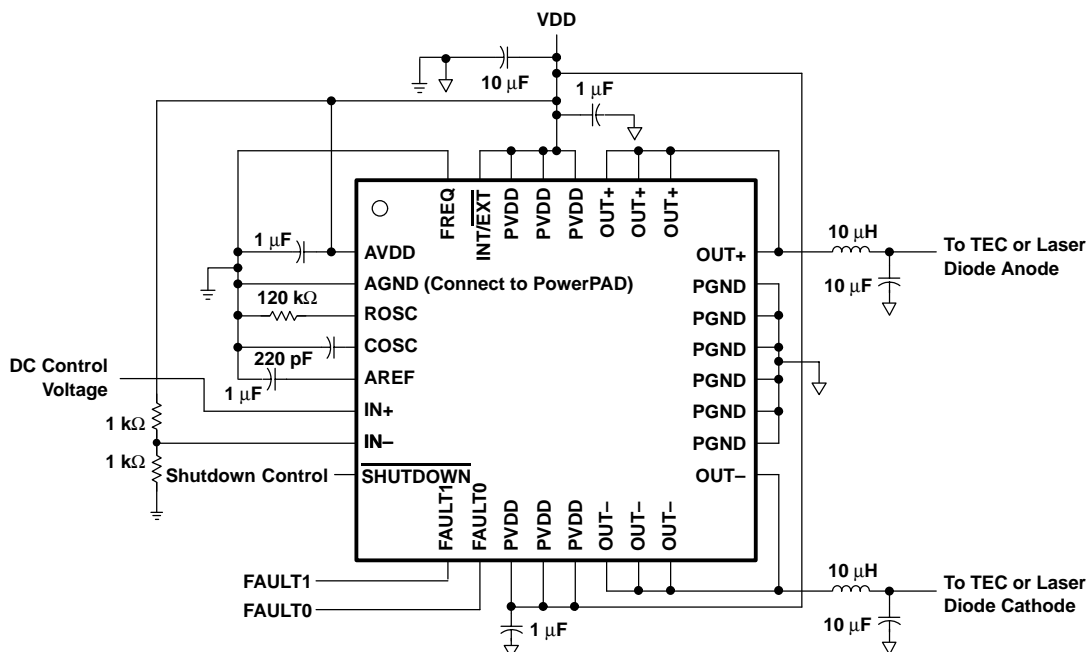


Figure 16. Typical Application Circuit

OUTPUT FILTER CONSIDERATIONS

TEC element manufacturers provide electrical specifications for maximum dc current and maximum output voltage for each particular element. The maximum ripple current, however, is typically only recommended to be less than 10% with no reference to the frequency components of the current. The maximum temperature differential across the element, which decreases as ripple current increases, may be calculated with the following equation:

$$\Delta T = \frac{1}{(1 + N^2)} \times \Delta T_{\max} \quad (1)$$

Where:

ΔT = actual temperature differential

ΔT_{\max} = maximum temperature differential
(specified by manufacturer)

N = ratio of ripple current to dc current

According to this relationship, a 10% ripple current reduces the maximum temperature differential by 1%. An LC network may be used to filter the current flowing to the TEC to reduce the amount of ripple and, more importantly, protect the rest of the system from any electromagnetic interference (EMI).

FILTER COMPONENT SELECTION

The LC filter, which may be designed from two different perspectives, both described below, helps estimate the overall performance of the system. The filter should be

designed for the worst-case conditions during operation, which is typically when the differential output is at 50% duty cycle. The following section serves as a starting point for the design, and any calculations should be confirmed with a prototype circuit in the lab.

Any filter should always be placed as close as possible to the DRV591 to reduce EMI.

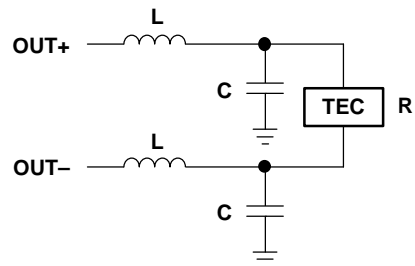


Figure 17. LC Output Filter

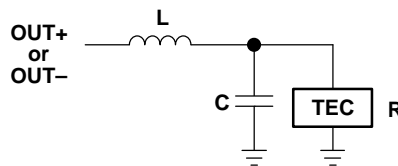


Figure 18. LC Half-Circuit Equivalent
(for DRV591 Only)

DRV591

SLOS389A – NOVEMBER 2001– REVISED MAY 2002

LC FILTER IN THE FREQUENCY DOMAIN

The transfer function for a 2nd order low-pass filter (Figures 17 and 18) is shown in equation (2):

$$H_{LP}(j\omega) = \frac{1}{-\left(\frac{\omega}{\omega_0}\right)^2 + \frac{1}{Q} \frac{j\omega}{\omega_0} + 1} \quad (2)$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Q = quality factor

ω = DRV591 switching frequency

For the DRV591, the differential output switching frequency is typically selected to be 500 kHz. The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the switching frequency. Equation (2) may then be simplified to give the following magnitude equation (3). These equations assume the use of the filter in Figure 17.

$$|H_{LP}|_{dB} = -40 \log \left(\frac{f_s}{f_o} \right) \quad (3)$$

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

f_s = 500 kHz (DRV591 switching frequency)

If $L=10\ \mu\text{H}$ and $C=10\ \mu\text{F}$, the cutoff frequency is 15.9 kHz, which corresponds to -60 dB of attenuation at the 500 kHz switching frequency. For $V_{DD} = 5\ \text{V}$, the amount of ripple voltage at the TEC element is approximately 5 mV.

The average TEC element has a resistance of 1.5 Ω , so the ripple current through the TEC is approximately 3.4 mA. At the 3-A maximum output current of the DRV591, this 5.4 mA corresponds to 0.11% ripple current, causing less than 0.0001% reduction of the maximum temperature differential of the TEC element (see equation 1).

LC FILTER IN THE TIME DOMAIN

The ripple current of an inductor may be calculated using equation (4):

$$\Delta I_L = \frac{(V_O - V_{TEC})DT_s}{L} \quad (4)$$

D = duty cycle (0.5 worst case)

$$T_s = 1/f_s = 1/500\ \text{kHz}$$

For $V_O = 5\ \text{V}$, $V_{TEC} = 2.5\ \text{V}$, and $L = 10\ \mu\text{H}$, the inductor ripple current is 250 mA. To calculate how much of that ripple current flows through the TEC element, however, the properties of the filter capacitor must be considered.

For relatively small capacitors (less than 22 μF) with very low equivalent series resistance (ESR, less than 10 m Ω), such as ceramic capacitors, the following equation (5) may be used to estimate the ripple voltage on the capacitor due to the change in charge:

$$\Delta V_C = \frac{\pi^2}{2} (1-D) \left(\frac{f_o}{f_s} \right)^2 V_{TEC} \quad (5)$$

D = duty cycle

f_s = 500 kHz

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

For $L = 10\ \mu\text{H}$ and $C = 10\ \mu\text{F}$, the cutoff frequency, f_o , is 15.9 kHz. For worst case duty cycle of 0.5 and $V_{TEC}=2.5\ \text{V}$, the ripple voltage on the capacitors is 6.2 mV. The ripple current may be calculated by dividing the ripple voltage by the TEC resistance of 1.5 Ω , resulting in a ripple current through the TEC element of 4.1 mA. Note that this is similar to the value calculated using the frequency domain approach.

For larger capacitors (greater than 22 μF) with relatively high ESR (greater than 100 m Ω), such as electrolytic capacitors, the ESR dominates over the charging-discharging of the capacitor. The following simple equation (6) may be used to estimate the ripple voltage:

$$\Delta V_C = \Delta I_L \times R_{ESR} \quad (6)$$

ΔI_L = inductor ripple current

R_{ESR} = filter capacitor ESR

For a 100 μF electrolytic capacitor, an ESR of 0.1 Ω is common. If the 10 μH inductor is used, delivering 250 mA of ripple current to the capacitor (as calculated above), then the ripple voltage is 25 mV. This is over ten times that of the 10 μF ceramic capacitor, as ceramic capacitors typically have negligible ESR.

SWITCHING FREQUENCY CONFIGURATION: OSCILLATOR COMPONENTS R_{OSC} AND C_{OSC} AND FREQ OPERATION

The onboard ramp generator requires an external resistor and capacitor to set the oscillation frequency. The frequency may be either 500 kHz or 100 kHz by selecting the proper capacitor value and by holding the FREQ pin either low (500 kHz) or high (100 kHz). Table 1 shows the values required and FREQ pin configuration for each switching frequency.

Table 1. Frequency Configuration Options

SWITCHING FREQUENCY	R_{OSC}	C_{OSC}	FREQ
500 kHz	120 k Ω	220 pF	LOW (GND)
100 kHz	120 k Ω	1 nF	HIGH (VDD)

For proper operation, the resistor R_{OSC} should have 1% tolerance while capacitor C_{OSC} should be a ceramic type with 10% tolerance. Both components should be grounded to AGND, which should be connected to PGND at a single point, typically where power and ground are physically connected to the printed-circuit board.

EXTERNAL CLOCKING OPERATION

To synchronize the switching to an external clock signal, pull the INT/EXT terminal low, and drive the clock signal into the COSC terminal. This clock signal must be from 10% to 90% duty cycle and meet the voltage requirements specified in the electrical specifications table. Since the DRV591 includes an internal frequency doubler, the external clock signal must be approximately 250 kHz. Deviations from the 250 kHz clock frequency are allowed and are specified in the electrical characteristic table. The resistor connected from ROSC to ground may be omitted from the circuit in this mode of operation—the source is disconnected internally.

INPUT CONFIGURATION: DIFFERENTIAL AND SINGLE-ENDED

If a differential input is used, it should be biased around the midrail of the DRV591 and must not exceed the common-mode input range of the input stage (see the operating characteristics at the beginning of the data sheet).

The most common configuration employs a single-ended input. The unused input should be tied to $V_{DD}/2$, which may be simply accomplished with a resistive voltage divider. For the best performance, the resistor values chosen should be at least 100 times lower than the input resistance of the DRV591. This prevents the bias voltage at the unused input from shifting when the signal input is applied. A small ceramic capacitor should also be placed from the input to ground to filter noise and keep the voltage stable. An op amp configured as a buffer may also be used to set the voltage at the unused input.

FIXED INTERNAL GAIN

The differential output voltage may be calculated using equation (7):

$$V_O = V_{OUT+} - V_{OUT-} = A_V (V_{IN+} - V_{IN-}) \quad (7)$$

A_V is the voltage gain, which is fixed internally at 2.34 V/V. The maximum and minimum ratings are provided in the electrical specification table at the beginning of the data sheet.

POWER SUPPLY DECOUPLING

To reduce the effects of high-frequency transients or spikes, a small ceramic capacitor, typically 0.1 μ F to 1 μ F, should be placed as close to each set of PVDD pins of the

DRV591 as possible. For bulk decoupling, a 10 μ F to 100 μ F tantalum or aluminum electrolytic capacitor should be placed relatively close to the DRV591.

AREF CAPACITOR

The AREF terminal is the output of an internal mid-rail voltage regulator used for the onboard oscillator and ramp generator. The regulator may not be used to provide power to any additional circuitry. A 1 μ F ceramic capacitor must be connected from AREF to AGND for stability (see oscillator components above for AGND connection information).

SHUTDOWN OPERATION

The DRV591 includes a shutdown mode that disables the outputs and places the device in a low supply current state. The SHUTDOWN pin may be controlled with a TTL logic signal. When SHUTDOWN is held high, the device operates normally. When SHUTDOWN is held low, the device is placed in shutdown. The SHUTDOWN pin must not be left floating. If the shutdown feature is unused, the pin may be connected to VDD.

FAULT REPORTING

The DRV591 includes circuitry to sense three faults:

- Overcurrent
- Undervoltage
- Overtemperature

These three fault conditions are decoded via the FAULT1 and FAULT0 terminals. Internally, these are open-drain outputs, so an external pull-up resistor of 5 k Ω or greater is required.

Table 2. Fault Indicators

FAULT1	FAULT0	
0	0	Overcurrent
0	1	Undervoltage
1	0	Overtemperature
1	1	Normal operation

The over-current fault is reported when the output current exceeds four amps. As soon as the condition is sensed, the over-current fault is set and the outputs go into a high-impedance state for approximately 3 μ s to 5 μ s (500 kHz operation). After 3 μ s to 5 μ s, the outputs are re-enabled. If the over-current condition has ended, the fault is cleared and the device resumes normal operation. If the over-current condition still exists, the above sequence repeats.

The under-voltage fault is reported when the operating voltage is reduced below 2.8 V. This fault is not latched, so as soon as the power-supply recovers, the fault is cleared and normal operation resumes. During the under-voltage condition, the outputs go into a high-impedance state to prevent over-dissipation due to increased $r_{DS(on)}$.

DRV591

SLOS389A – NOVEMBER 2001 – REVISED MAY 2002

The over-temperature fault is reported when the junction temperature exceeds 130°C. The device continues operating normally until the junction temperature reaches 190°C, at which point the IC is disabled to prevent permanent damage from occurring. The system's controller must reduce the power demanded from the DRV591 once the over-temperature flag is set, or else the device switches off when it reaches 190°C. This fault is not latched; once the junction temperature drops below 130°C, the fault is cleared, and normal operation resumes.

POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURE

Though the DRV591 is much more efficient than traditional linear solutions, the power drop across the on-resistance of the output transistors does generate some heat in the package, which may be calculated as shown in equation (8):

$$P_{DISS} = (I_{OUT})^2 \times r_{DS(on), total} \quad (8)$$

For example, at the maximum output current of 3 A through a total on-resistance of 130 mΩ (at $T_J = 25^\circ\text{C}$), the power dissipated in the package is 1.17 W.

Calculate the maximum ambient temperature using equation (9):

$$T_A = T_J - (\theta_{JA} \times P_{DISS}) \quad (9)$$

PRINTED-CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

Since the DRV591 is a high-current switching device, a few guidelines for the layout of the printed-circuit board (PCB) must be considered:

1. **Grounding.** Analog ground (AGND) and power ground (PGND) must be kept separated, ideally back to where the power supply physically connects to the PCB, minimally back to the bulk decoupling capacitor (10 μF ceramic minimum). Furthermore, the PowerPAD ground connection should be made to AGND, not PGND. Ground planes are not recommended for AGND or PGND, traces should be used to route the currents. Wide traces (100 mils) should be used for PGND while narrow traces (15 mils) should be used for AGND.
2. **Power supply decoupling.** A small 0.1 μF to 1 μF ceramic capacitor should be placed as close to each set of PVDD pins as possible, connecting from PVDD to PGND. A 0.1 μF to 1 μF ceramic capacitor should also be placed close to the AVDD pin, connecting from AVDD to AGND. A bulk decoupling capacitor of at least 10 μF , preferably ceramic, should be placed close to the DRV591, from PVDD to PGND. If power supply lines are long, additional decoupling may be required.
3. **Power and output traces.** The power and output traces should be sized to handle the desired maximum output current. The output traces should be kept as short as possible to reduce EMI, i.e., the output filter should be placed as close to the DRV591 outputs as possible.
4. **PowerPAD.** The DRV591 in the Quad Flatpack package uses TI's PowerPAD technology to enhance the thermal performance. The PowerPAD is physically connected to the substrate of the DRV591 silicon, which is connected to AGND. The PowerPAD ground connection should therefore be kept separate from PGND as described above. The pad underneath the AGND pin may be connected underneath the device to the PowerPAD ground connection for ease of routing. For additional information on PowerPAD PCB layout, refer to the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002.
5. **Thermal performance.** For proper thermal performance, the PowerPAD must be soldered down to a thermal land, as described in the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002. In addition, at high current levels (greater than 2 A) or high ambient temperatures (greater than 25°C), an internal plane may be used for heat sinking. The vias under the PowerPAD should make a solid connection, and the plane should not be tied to ground except through the PowerPAD connection, as described above.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
DRV591VFP	ACTIVE	HLQFP	VFP	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DRV591VFPG4	ACTIVE	HLQFP	VFP	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DRV591VFPR	ACTIVE	HLQFP	VFP	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DRV591VFPRG4	ACTIVE	HLQFP	VFP	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

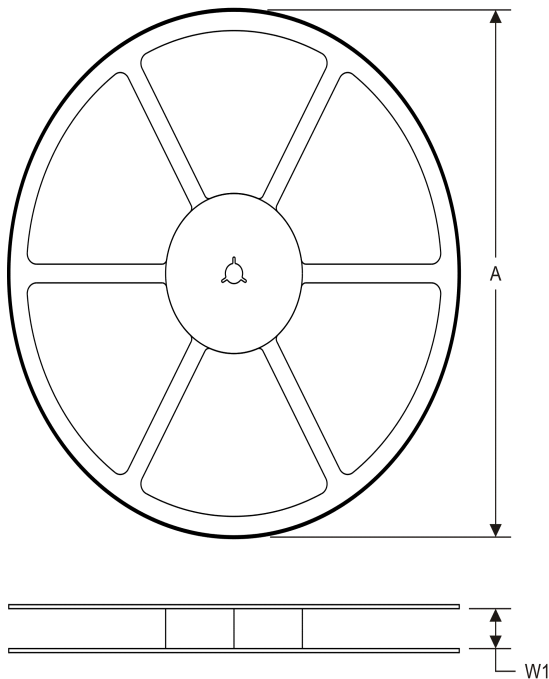
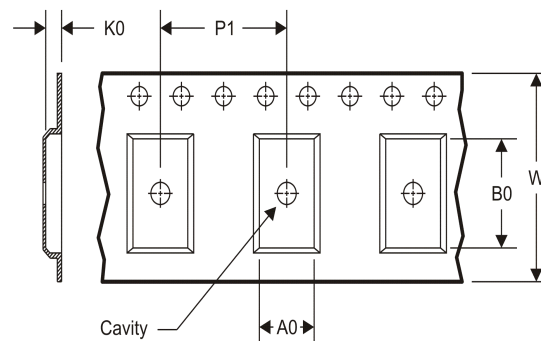
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


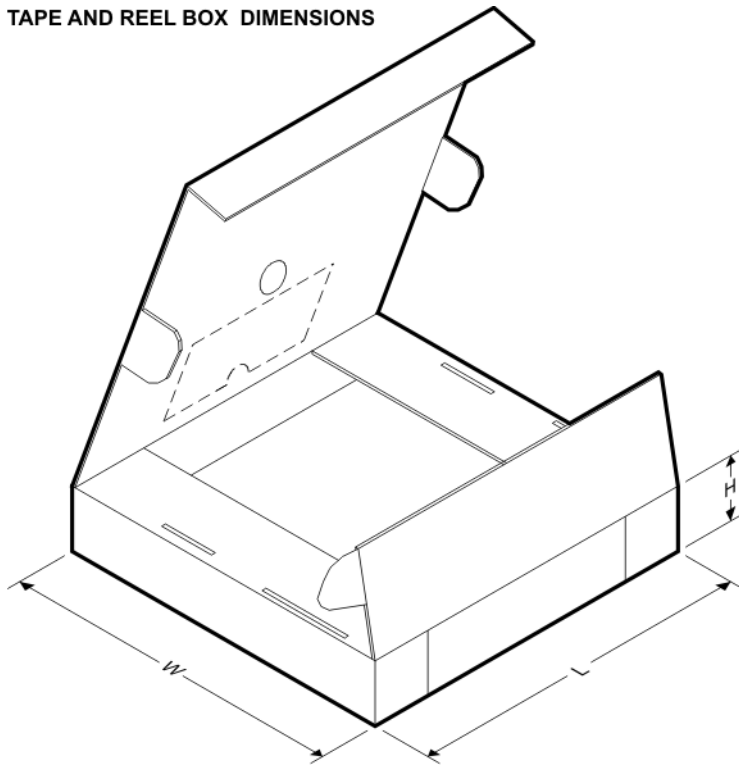
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV591VFPR	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

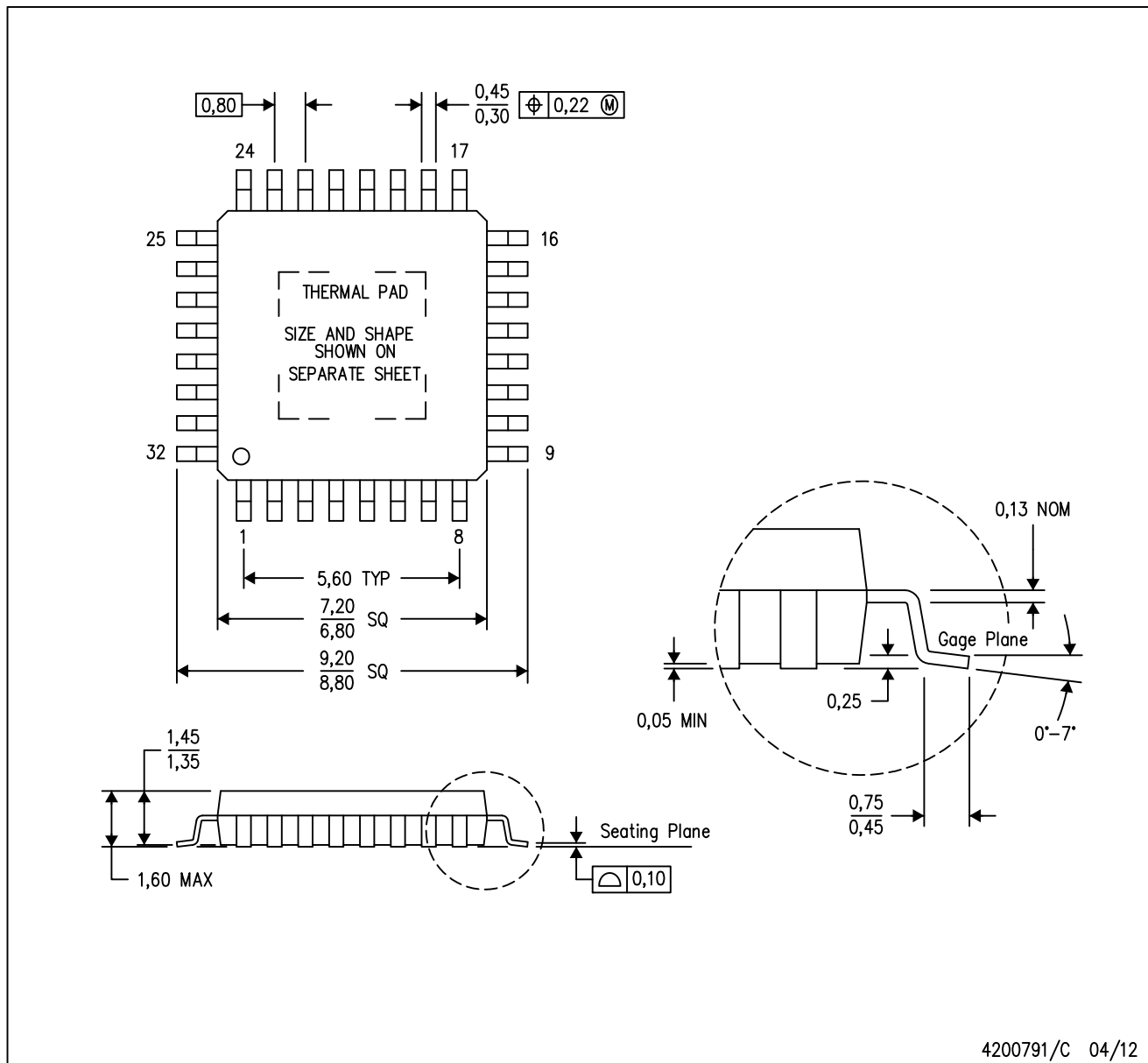


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV591VFPR	HLQFP	VFP	32	1000	367.0	367.0	38.0

VFP (S-PQFP-G32)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments Incorporated.

VFP (S-PQFP-G32)

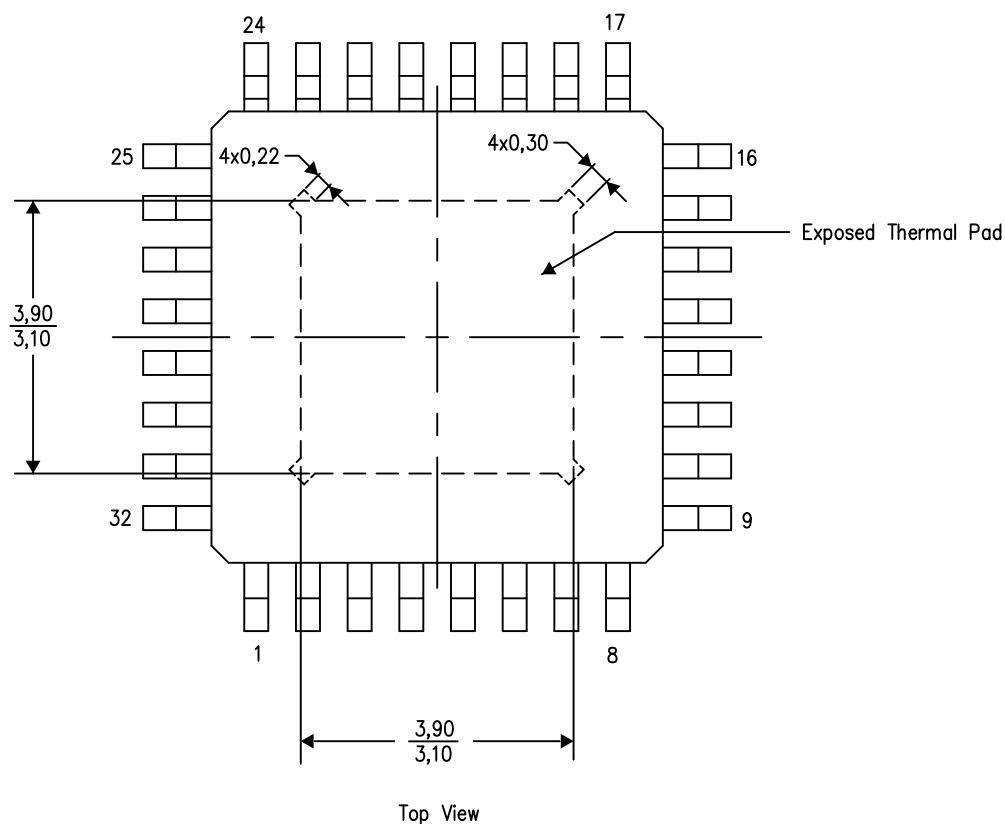
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

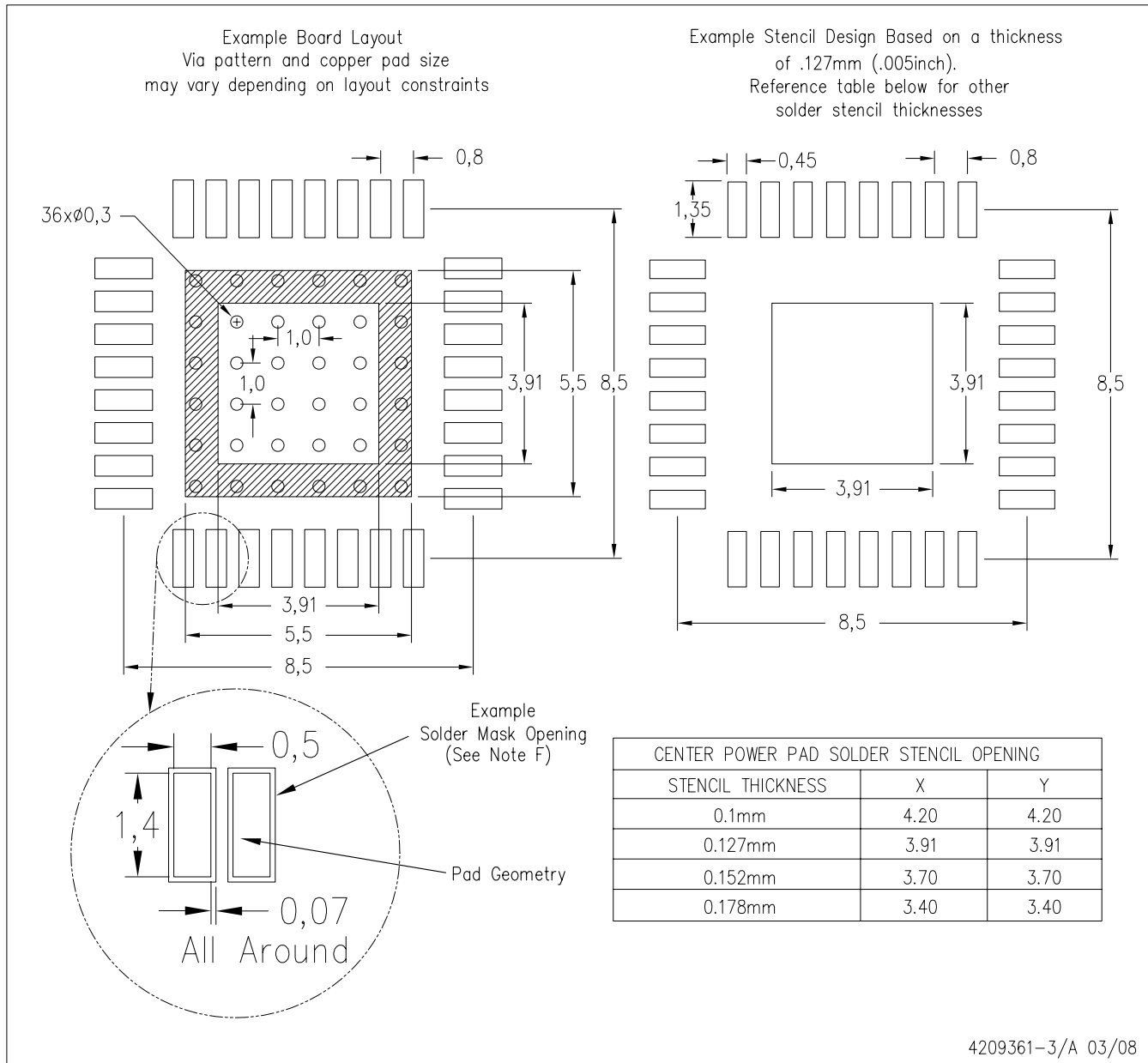


Exposed Thermal Pad Dimensions

4206318-2/D 04/12

NOTE: All linear dimensions are in millimeters

VFP (S-PQFP-G32) PowerPAD™



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community e2e.ti.com