QUAD 1/2-H-BRIDGE DRIVER IC

Check for Samples: DRV8844

FEATURES

- **Quad 1/2-H-Bridge DC Motor Driver**
  - **Can Drive Four Solenoids, Two DC Motors, One Stepper Motor, or Other Loads**
  - **Full Individual Half Bridge Control**
  - **Low MOSFET On-Resistance**
- **2.5-A Maximum Drive Current at 24 V, 25°C**
- **Floating Input Buffers Allow Dual (Bipolar) Supplies (up to ±30 V)**
- **Built-In 3.3-V, 10-mA LDO Regulator**
- **Industry Standard IN/IN Digital Control Interface**
- **8-V to 60-V Operating Supply Voltage Range**
- **Thermally Enhanced Surface Mount Package**

APPLICATIONS

- **Textile Machines**
- **Office Automation Machines**
- **Gaming Machines**
- **Factory Automation**
- **Robotics**

DESCRIPTION

The DRV8844 provides four individually controllable 1/2-H-bridge drivers. It can be used to drive two DC motors, one stepper motor, four solenoids, or other loads. The output driver channel for each channel consists of N-channel power MOSFET's configured in a 1/2-H-bridge configuration.

The DRV8844 can supply up to 2.5-A peak or 1.75-A RMS output current per channel (with proper PCB heatsinking at 24 V and 25°C) per H-bridge.

Separate inputs to independently control each 1/2-H-bridge are provided. To allow operation with split supplies, the logic inputs and nFAULT output are referenced to a separate floating ground pin.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

The DRV8844 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PowerPAD™ (HTSSOP) - PWP	Reel of 2000	DRV8844PWPR	DRV8844
		Tube of 50	DRV8844PWP	

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE INFORMATION

Functional Block Diagram

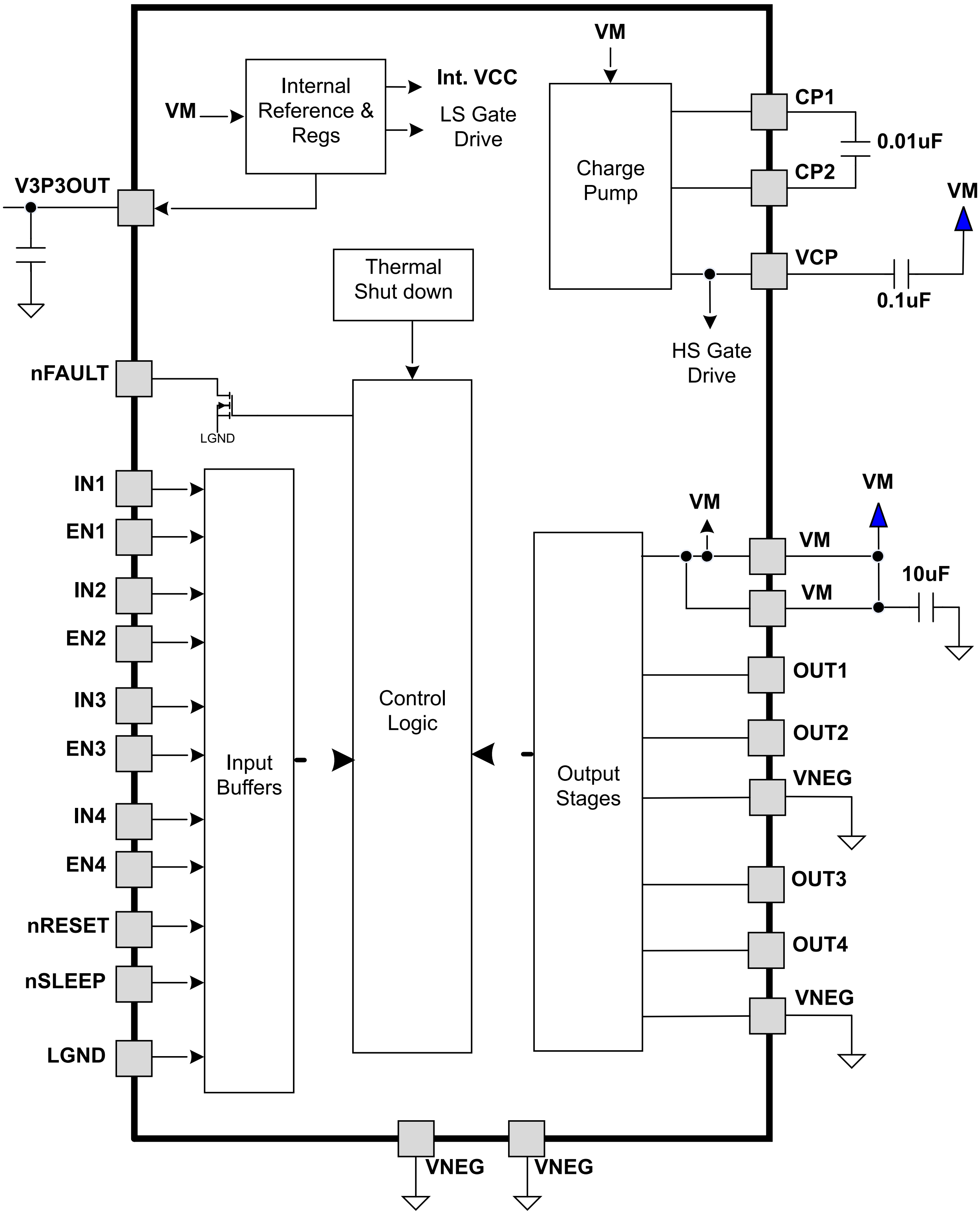
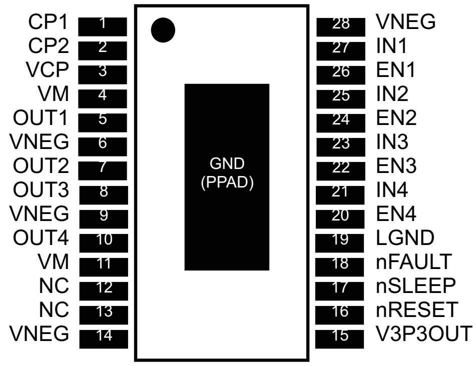


Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O [(1)]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
VNEG	6, 9, 14, 28, PPAD	-	Negative power supply (dual supplies) or ground (single supply)	
LGND	19	I	Logic input reference ground	Connect to logic ground. This may be any voltage between VNEG and VM - 8 V.
VM	4, 11	-	Main power supply	Connect to motor supply (8 V - 60 V). Both pins must be connected to same supply. Bypass to VNEG with a 10-µF (minimum) capacitor.
V3P3OUT	15	O	3.3-V regulator output	Bypass to VNEG with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-µF 100-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor to VM.
CONTROL				
IN1	27	I	Channel 1 input	Logic input controls state of OUT1. Internal pulldown.
EN1	26	I	Channel 1 enable	Logic high enables OUT1. Internal pulldown.
IN2	25	I	Channel 2 input	Logic input controls state of OUT2. Internal pulldown.
EN2	24	I	Channel 2 enable	Logic high enables OUT2. Internal pulldown.
IN3	23	I	Channel 3 input	Logic input controls state of OUT3. Internal pulldown.
EN3	22	I	Channel 3 enable	Logic high enables OUT3. Internal pulldown.
IN4	21	I	Channel 4 input	Logic input controls state of OUT4. Internal pulldown.
EN4	20	I	Channel 4 enable	Logic high enables OUT4. Internal pulldown.
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs. Internal pulldown.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemp, overcurrent, UVLO). Open-drain output.
OUTPUT				
OUT1	5	O	Output 1	Connect to loads.
OUT2	7	O	Output 2	
OUT3	8	O	Output 3	
OUT4	10	O	Output 4	
NO CONNECT				
NC	12, 13	-	No connect	No connection to these pins

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted) (1) (2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 65	V
	Logic ground voltage range (LGND)	–0.5 to VM - 8	V
	Digital pin voltage range	LGND - 0.5 to LGND + 7	V
	Peak motor drive output current, t < 1 μS	Internally limited	A
	Continuous motor drive output current (3)	2.5	A
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VNEG terminal, unless otherwise specified.
(3) Power dissipation and thermal limits must be observed.

THERMAL INFORMATION

THERMAL METRIC (1)		DRV8844 PWP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance (2)	31.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	15.9	
θ_{JB}	Junction-to-board thermal resistance (4)	5.6	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter (6)	5.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (7)	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	8		60	V
I_{V3P3}	V3P3OUT load current	0		10	mA

(1) All V_M pins must be connected to the same supply voltage.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		1	5	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		500	800	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		6.3	8	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.18	3.3	3.52	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			LGND + 0.6	LGND + 0.7	V
V_{IH}	Input high voltage		LGND + 2.2		LGND + 5.25	V
V_{HYS}	Input hysteresis		50		600	mV
I_{IL}	Input low current	VIN = LGND	–5		5	µA
I_{IH}	Input high current	VIN = LGND + 3.3 V			100	µA
R_{PD}	Internal pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			LGND + 0.5	V
I_{OH}	Output high leakage current	V_O = LGND + 3.3 V			1	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
I_{OFF}	Off-state leakage current		–2		2	µA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		3			A
t_{DEAD}	Output dead time			90		ns
t_{OCP}	Overcurrent protection deglitch time			5		µs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

SWITCHING CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

NUMBER	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
1	t_1	Delay time, ENx high to OUTx high, INx = 1	130	330	ns
2	t_2	Delay time, ENx low to OUTx low, INx = 1	275	475	ns
3	t_3	Delay time, ENx high to OUTx low, INx = 0	100	300	ns
4	t_4	Delay time, ENx low to OUTx high, INx = 0	200	400	ns
5	t_5	Delay time, INx high to OUTx high	300	500	ns
6	t_6	Delay time, INx low to OUTx low	275	475	ns
7	t_R	Output rise time, resistive load to VNEG	30	150	ns
8	t_F	Output fall time, resistive load to VNEG	30	150	ns

(1) Not production tested – specified by design

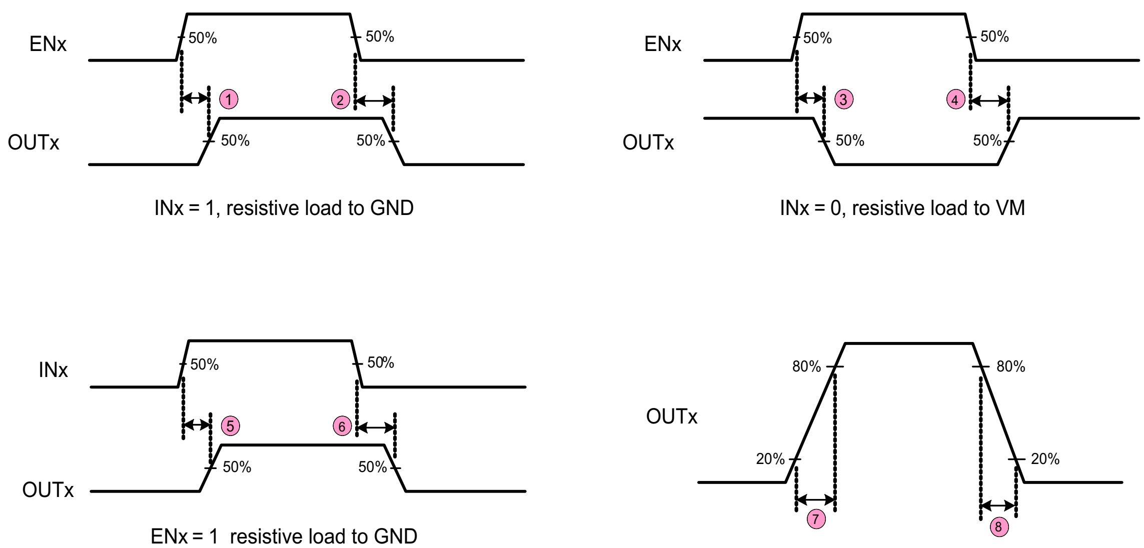


Figure 1. DRV8844 Switching Characteristics

FUNCTIONAL DESCRIPTION

Output Stage

The DRV8844 contains four 1/2-H-bridge drivers using N-channel MOSFETs. A block diagram of the output circuitry is shown in Figure 2.

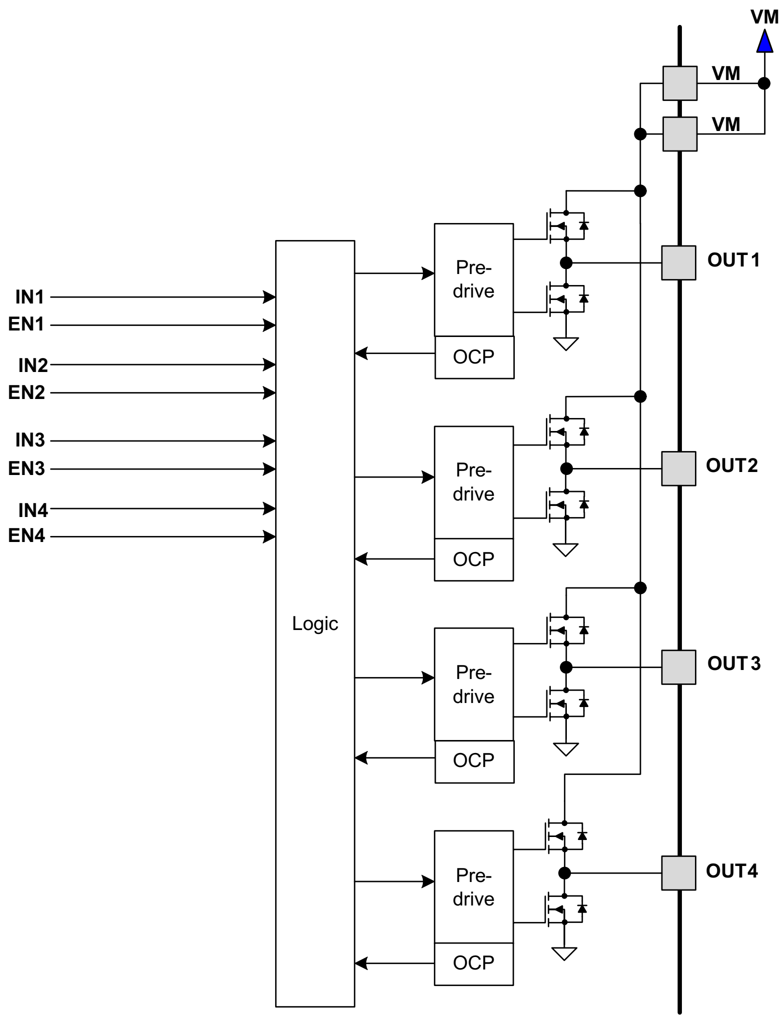


Figure 2. Motor Control Circuitry

The output pins are driven between VM and VNEG. VNEG is normaly ground for single supply applications, and a negative voltage for dual supply applications.

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

Logic Inputs

The logic inputs and nFAULT output are referenced to the LGND pin. This pin would be connected to the logic ground of the source of the logic signals (e.g., microcontroller). This allows LGND to be at a different voltage than VNEG; for example, you could drive a load by with bipolar power supplies by driving VM with +24 V and VNEG with -24 V, and connect LGND to 0 V (ground).

Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. Table 2 shows the logic.

Table 2. H-Bridge Logic

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

The inputs can also be used for PWM control of, for example, the speed of a DC motor. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to the ENx pin; to use slow decay, the PWM signal is applied to the INx pin. Table 3 is an example of driving a DC motor using OUT1 and OUT2 as an H-bridge:

Table 3. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
PWM	1	0	1	Forward PWM, slow decay
0	1	PWM	1	Reverse PWM, slow decay
1	PWM	0	PWM	Forward PWM, fast decay
0	PWM	1	PWM	Reverse PWM, fast decay

The drawings below show the current paths in different drive and decay modes:

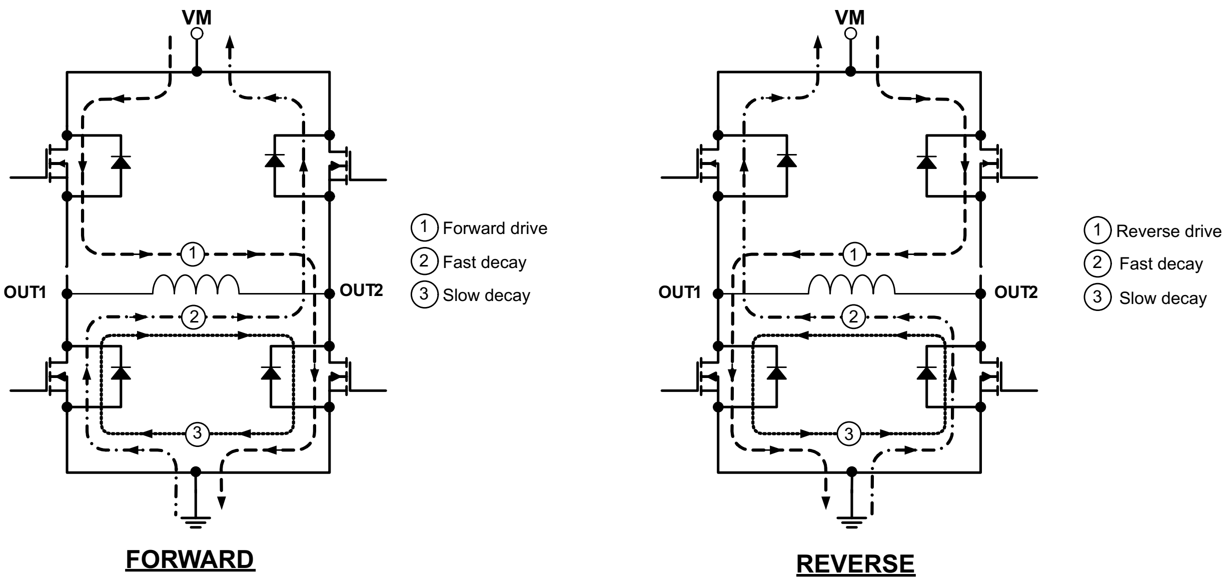


Figure 3. Current Paths

Charge Pump

Since the output stages use N-channel FETs, a gate drive voltage higher than the VM power supply is needed to fully enhance the high-side FETs. The DRV8844 integrates a charge pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. Refer to the block diagram and pin descriptions for details on these capacitors (value, connection, etc.).

The charge pump is shut down when SLEEPn is active low.

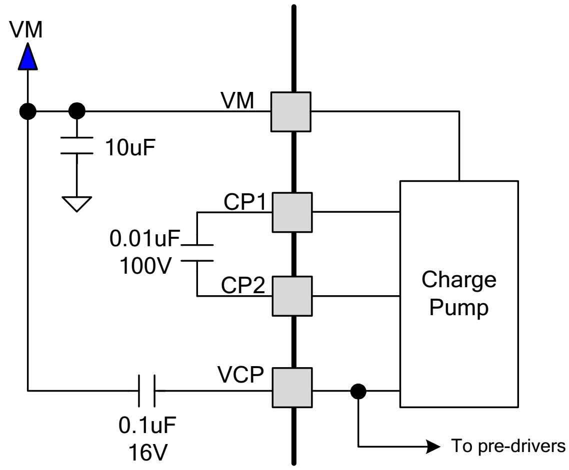


Figure 4. Charge Pump

nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. Note that nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals need to be driven to logic high for device operation.

The V3P3OUT LDO regulator remains operational in sleep mode.

Protection Circuits

The DRV8844 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP deglitch time, the channel experiencing the overcurrent will be disabled and the nFAULT pin will be driven low. The driver will remain off until either RESET is asserted or VM power is cycled.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all outputs will be disabled, internal logic will be reset, and the nFAULT pin will be driven low. Operation will resume when VM rises above the UVLO threshold.

THERMAL INFORMATION

Thermal Protection

The SDRV8844 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the SDRV8844 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each H-bridge when running a DC motor can be roughly estimated by Equation 1.

$$P = 2 \bullet R_{DS(ON)} \bullet (I_{OUT})^2 \quad (1)$$

where P is the power dissipation of one H-bridge, $R_{DS(ON)}$ is the resistance of each FET, and I_{OUT} is the RMS output current being applied to each winding. I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The total device dissipation will be the power dissipated in each of the two H-bridges added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV8844PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8844	Samples
DRV8844PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8844	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

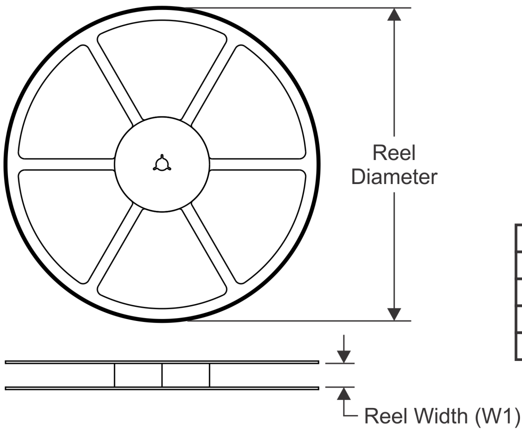
(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

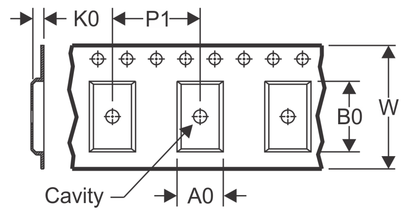
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

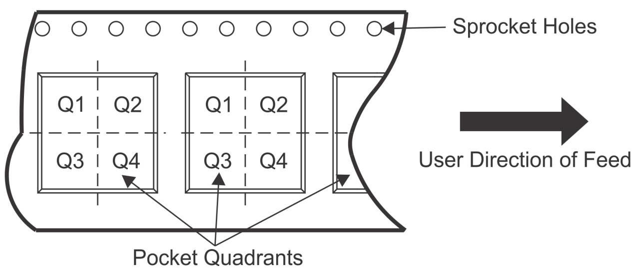


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

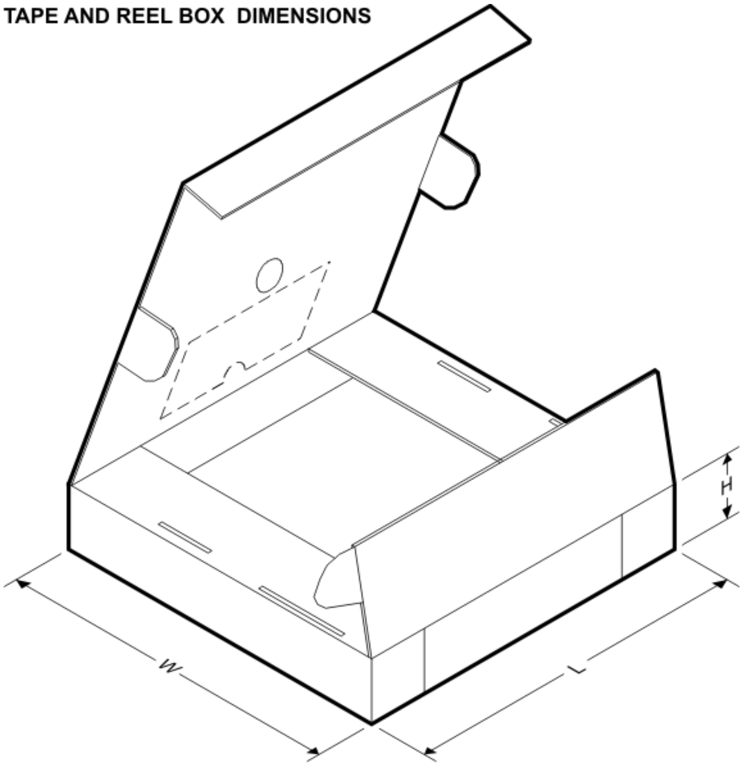


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8844PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

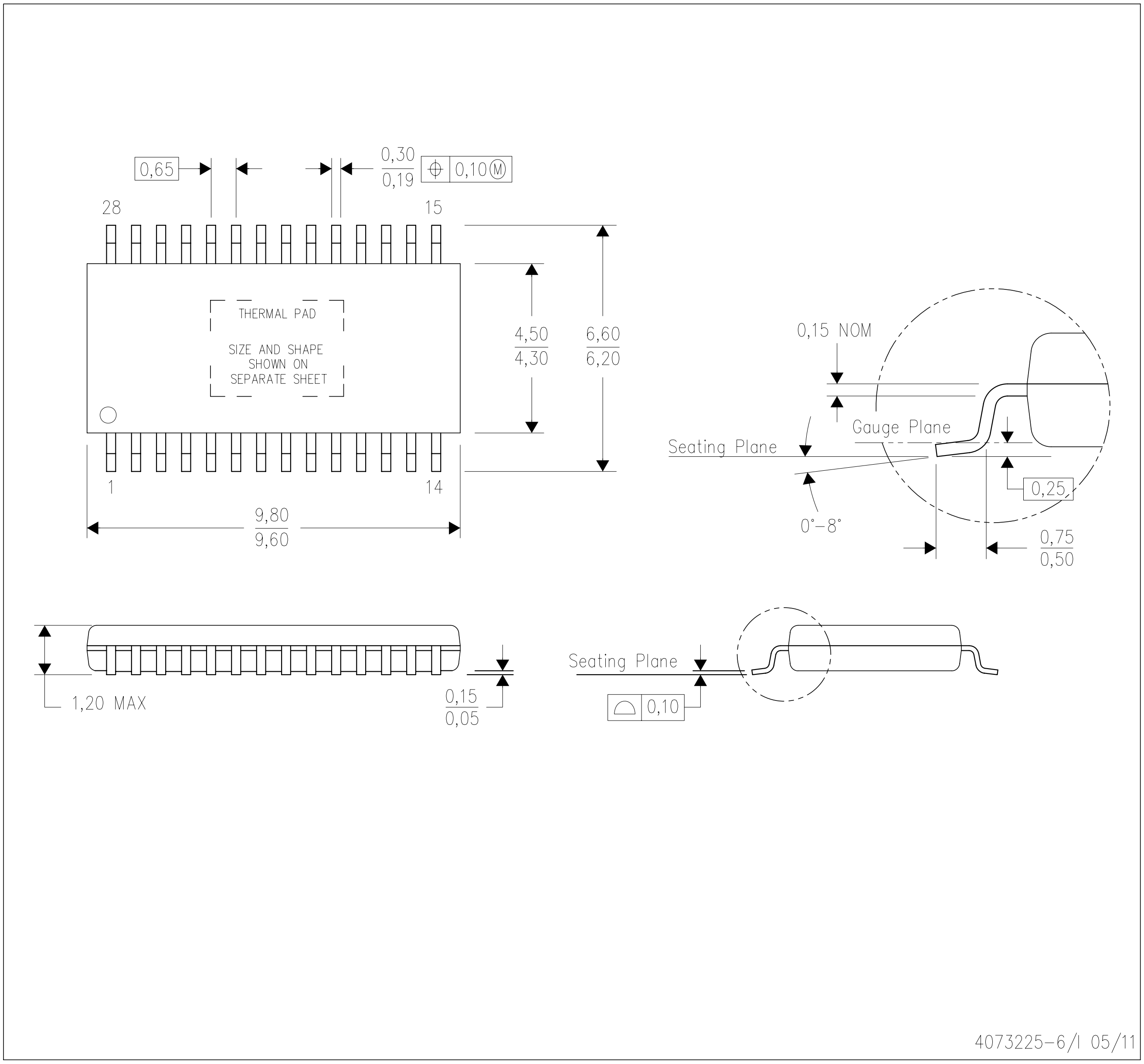
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8844PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

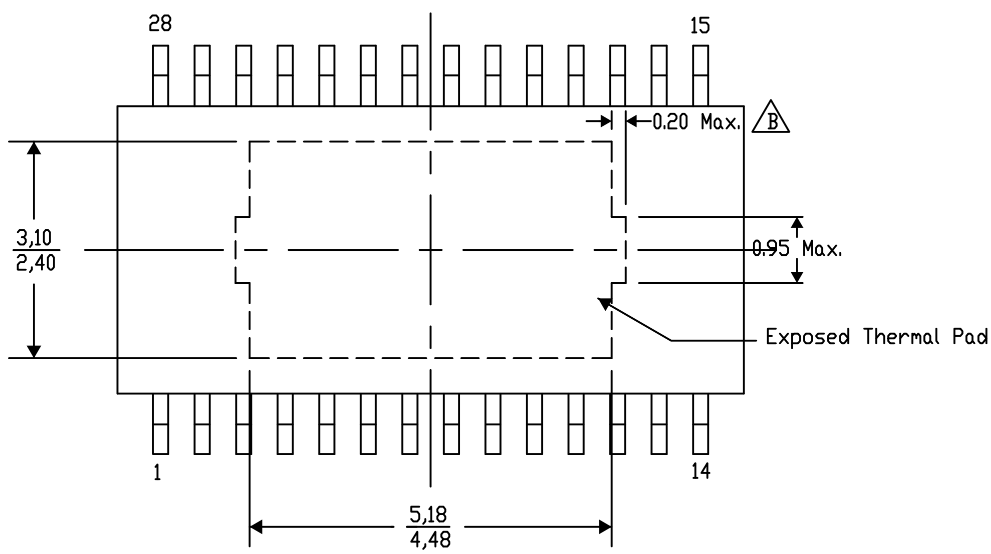
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

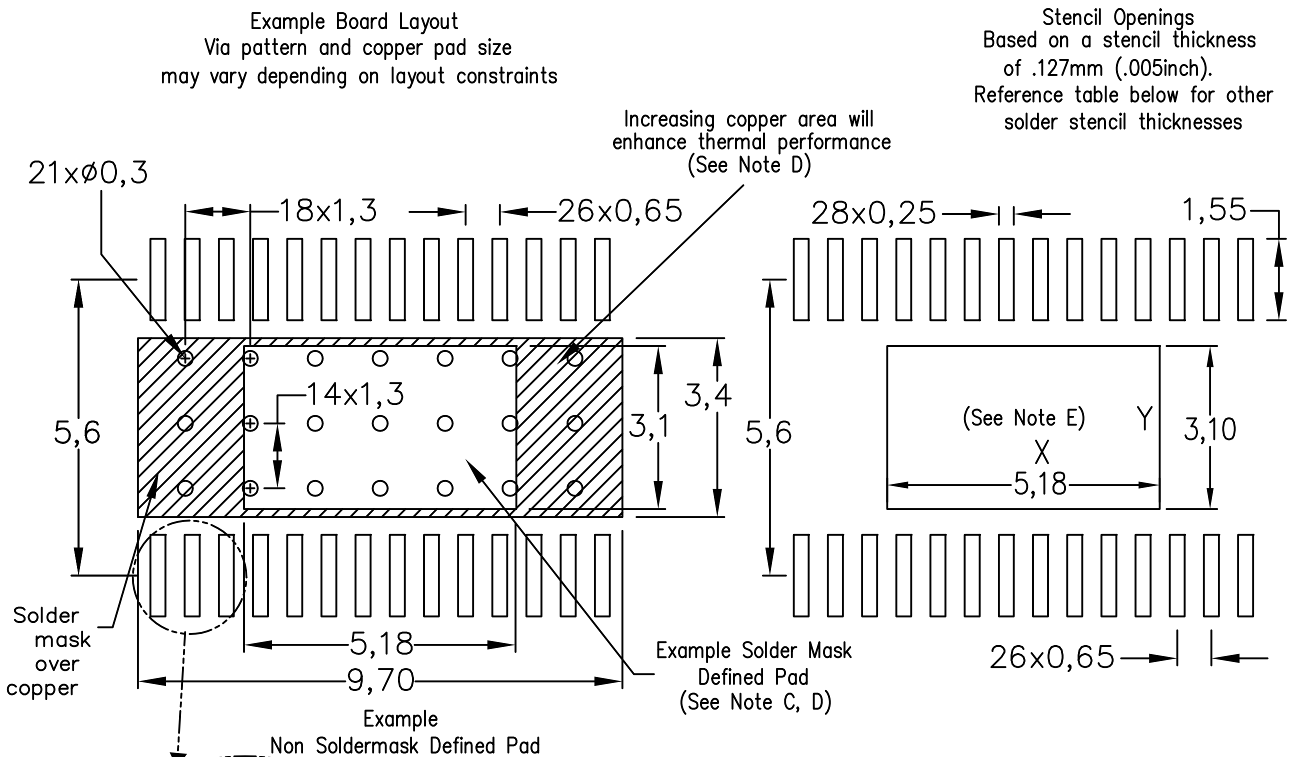
Exposed Thermal Pad Dimensions

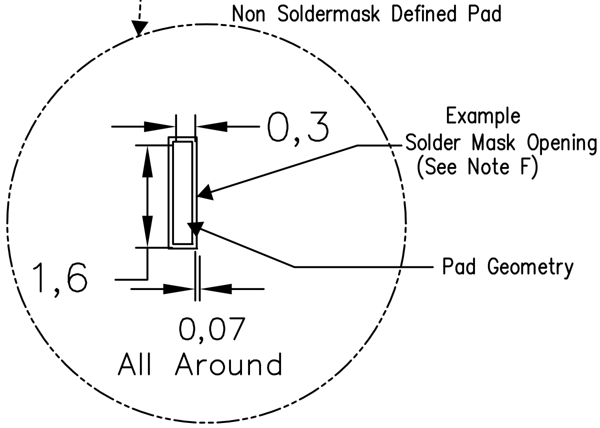
4206332–38/AC 07/12

NOTE: A. All linear dimensions are in millimeters
B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	3.4
0.127mm	5.18	3.1
0.152mm	4.9	2.8
0.178mm	4.7	2.7

4207609-22/R 07/12

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.