DS1339
Serial Real-Time Clock

www.maxim-ic.com

FEATURES

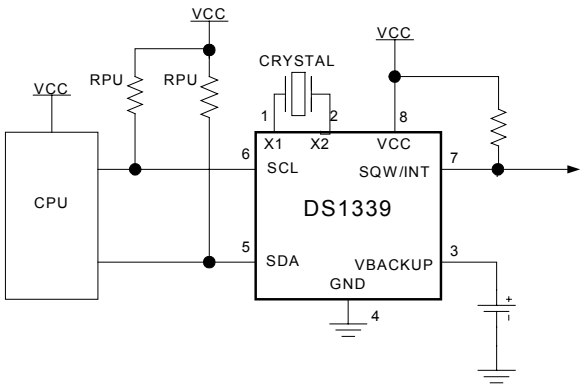
- Real-time clock (RTC) counts seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- 2-wire serial interface
- Two time-of-day alarms
- Programmable square-wave output
- Oscillator stop flag
- Automatic power-fail detect and switch circuitry
- Trickle charge capability

ORDERING INFORMATION

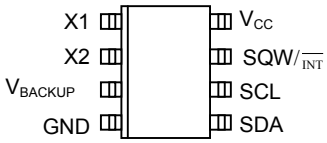
PART	PIN-PACKAGE	TOP MARK
DS1339U-2	8 µSOP	1339 ##-2
DS1339U-3	8 µSOP	1339 ##-3
DS1339U-33	8 µSOP	1339 ##-33

= second line, revision code
2 = 2.0V, V_{CC} ±10%
3 = 3.0V, V_{CC} ±10%
33 = 3.3V, V_{CC} ±10%

TYPICAL OPERATING CIRCUIT



PIN ASSIGNMENT (Top View)



8-Pin µSOP

Package Dimension Information

http://www.maxim-ic.com/TechSupport/DallasPackInfo.htm

PIN DESCRIPTION

V_{CC}	- Power Supply
X1, X2	- 32.768kHz Crystal Connection
GND	- Ground
SDA	- Serial Data
SCL	- Serial Clock
V_{BACKUP}	- Secondary Power Supply
SQW/$\overline{INT}$	- Square-Wave/Interrupt Output

APPLICATIONS

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)
- Other (Utility Meter, Vending Machine, Thermostat, Modem)

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://www.maxim-ic.com/errata.*

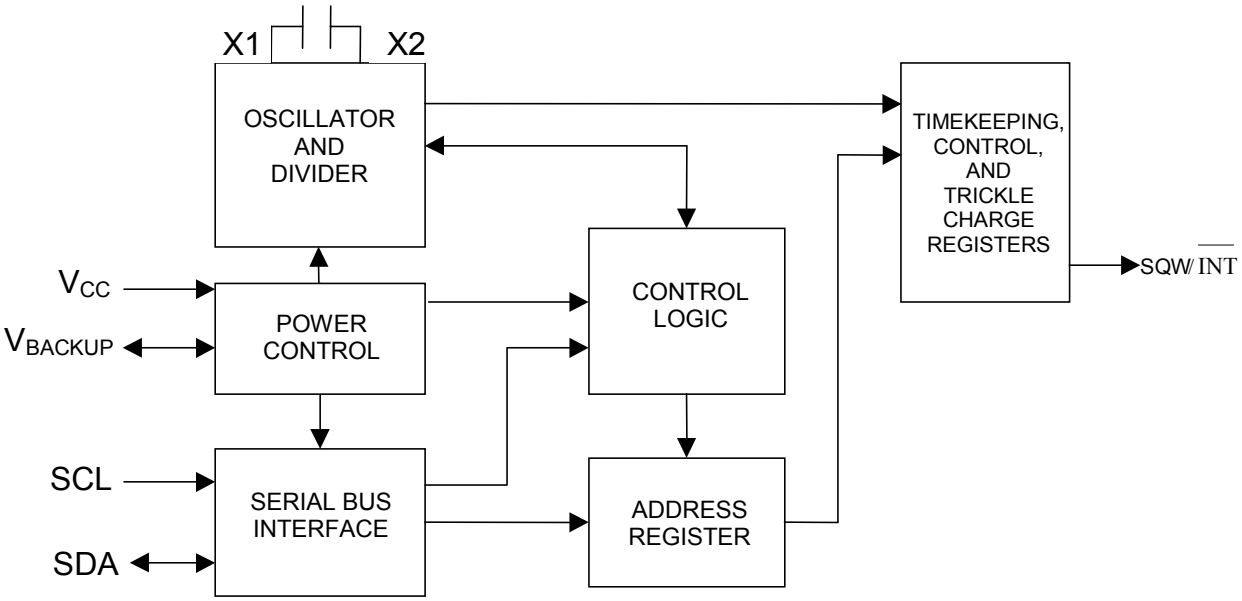
DESCRIPTION

The DS1339 serial real-time clock is a low-power clock/date device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially by a 2-wire bidirectional bus. The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1339 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply.

OPERATION

The DS1339 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels. The block diagram in Figure 1 shows the main elements of the serial real-time clock.

Figure 1. BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

V_{CC}, GND – DC power is provided to the device on these pins.

SCL (Serial Clock Input) – SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) – SDA is the input/output pin for the 2-wire serial interface. The SDA pin is an open-drain output and requires an external pullup resistor.

V_{BACKUP} (Secondary Supply Input) – Connection for a secondary power supply. Supply voltage must be held between 1.3V and 3.7V for proper operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.

SQW/$\overline{\text{INT}}$ (Square-Wave/Interrupt Output) – Programmable square-wave or interrupt-output signal. The SQW/$\overline{\text{INT}}$ pin is an open-drain output and requires an external pullup resistor.

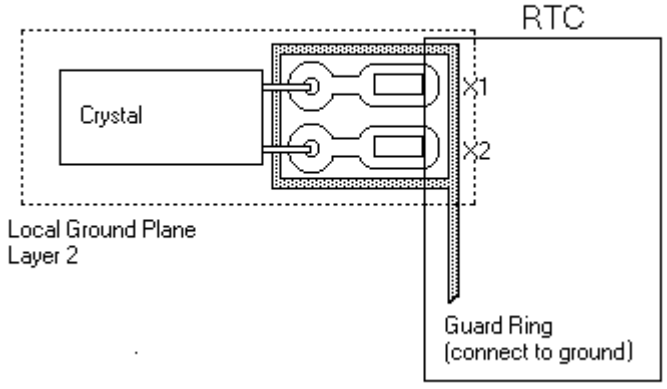
X1, X2 – These signals are connections for a standard 32.768kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF.

For more information about crystal selection and crystal layout considerations, refer to *Application Note 58* "Crystal Considerations with Dallas Real-Time Clocks."

The DS1339 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

The oscillator is controlled by an enable bit in the control register. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

TYPICAL PC BOARD LAYOUT FOR CRYSTAL



CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Refer to *Application Note 58* "Crystal Considerations with Dallas Real-Time Clocks" for detailed information.

ADDRESS MAP

The address map for the registers of the DS1339 is shown in Figure 2. During a multibyte access, when the address pointer reaches the end of the register space (10h), it wraps around to location 00h. On a 2-wire START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock can continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Figure 2. DS1339 TIMEKEEPER REGISTERS

ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FUNCTION	RANGE
00H	0	10 SECONDS			SECONDS				Seconds	00–59
01H	0	10 MINUTES			MINUTES				Minutes	00–59
02H	0	12/24	AM/PM 10HR	10HR	HOUR				Hours	1–12 + AM/PM 00–23
03H	0	0	0	0	0	DAY			Day	1–7
04H	0	0	10 DATE		DATE				Date	00–31
05H	CENTURY	0	0	10 MO	MONTH				Month/ Century	01–12 + Century
06H	10 YEAR				YEAR				Year	00–99
07H	A1M1	10 SECONDS			SECONDS				Alarm 1 Seconds	00–59
08H	A1M2	10 MINUTES			MINUTES				Alarm 1 Minutes	00–59
09H	A1M3	12/24	AM/PM 10HR	10HR	HOUR				Alarm 1 Hours	1–12 + AM/PM 00-23
0AH	A1M4	DY/DT	10 DATE		DAY DATE				Alarm 1 Day Alarm 1 Date	1–7 1–31
0BH	A2M2	10 MINUTES			MINUTES				Alarm 2 Minutes	00–59
0CH	A2M3	12/24	AM/PM 10HR	10HR	HOUR				Alarm 2 Hours	1–12 + AM/PM 00–23
0DH	A2M4	DY/DT	10 DATE		DAY DATE				Alarm 2 Day Alarm 2 Date	1–7 1–31
0EH	$\overline{\text{EOSC}}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	—
10H	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charge	—

Note: *Unless otherwise specified, the registers' state are not defined when power is first applied or V_{CC} and V_{BACKUP} falls below the V_{BACKUP} min.*

TIME AND DATE OPERATION

The time and date information is obtained by reading the appropriate register bytes. The real-time clock registers are illustrated in Figure 2. The time and date are set or initialized by writing the appropriate register bytes. The contents of the time and date registers are in the binary coded decimal (BCD) format. The DS1339 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). All hours values, including the alarms, must be re-entered whenever the 12/24-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START or STOP, and when the address pointer rolls over to 0. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

ALARMS

The DS1339 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the SQW/$\overline{\text{INT}}$ output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Figure 3). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Figure 3 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/DT bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/DT is written to a logic 0, the alarm is the result of a match with date of the month. If DY/DT is written to a logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag (A1F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/$\overline{\text{INT}}$ signal.

Figure 3. ALARM MASK BITS

DY/DT	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/DT	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 second of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

SPECIAL PURPOSE REGISTERS

The DS1339 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

CONTROL REGISTER (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{EOSC}}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE

$\overline{\text{EOSC}}$ (Enable Oscillator) – This bit when set to logic 0 starts the oscillator. When this bit is set to a logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

BBSQI (Battery-Backed Square-Wave and Interrupt Enable) – This bit when set to a logic 1 enables the square-wave or interrupt output when V_{CC} is absent and the DS1339 is being powered by the V_{BACKUP} pin. When BBSQI is a logic 0, the SQW/$\overline{\text{INT}}$ pin goes high impedance when V_{CC} falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

RS2 and RS1 (Rate Select) – These bits control the frequency of the square-wave output when the square wave has been enabled. Figure 4 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

Figure 4. SQUARE-WAVE OUTPUT FREQUENCY

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

INTCN (Interrupt Control) – This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the Alarm 1 or Alarm 2 registers activate the SQW/$\overline{\text{INT}}$ pin (provided that the alarms are enabled).When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{\text{INT}}$ pin. This bit is set to logic 0 when power is first applied.

A1IE (Alarm 1 Interrupt Enable) – When set to logic 1, this bit permits the A1F bit in the status register to assert SQW/$\overline{\text{INT}}$ (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the an interrupt signal. The A1IE bit is disabled (logic 0) when power is first applied.

A2IE (Alarm 2 Interrupt Enable) – When set to a logic 1, this bit permits the A2F bit in the status register to assert SQW/$\overline{\text{INT}}$ (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

STATUS REGISTER (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

OSF (Oscillator Stop Flag) – A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit is edge-triggered and set to logic 1 anytime the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on both V_{CC} and V_{BACKUP} are insufficient to support oscillation.
3) The $\overline{\text{EOSC}}$ bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to a logic 0. Attempting to write to logic 1 leaves the value unchanged.

A1F (Alarm 1 Flag) – A logic 1 in the A1F bit indicates that the time matched the Alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{\text{INT}}$ pin is also be asserted. A1F

is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

A2F (Alarm 2 Flag) – A logic 1 in the A2F bit indicates that the time matched the Alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{\text{INT}}$ pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

TRICKLE CHARGE REGISTER (10h)

The simplified schematic of Figure 6 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode select (DS) bits (bits 2 and 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. The ROUT bits (bits 0, 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Bit values are shown in Figure 5.

Figure 5. TRICKLE CHARGE REGISTER (10h) BIT VALUES

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor

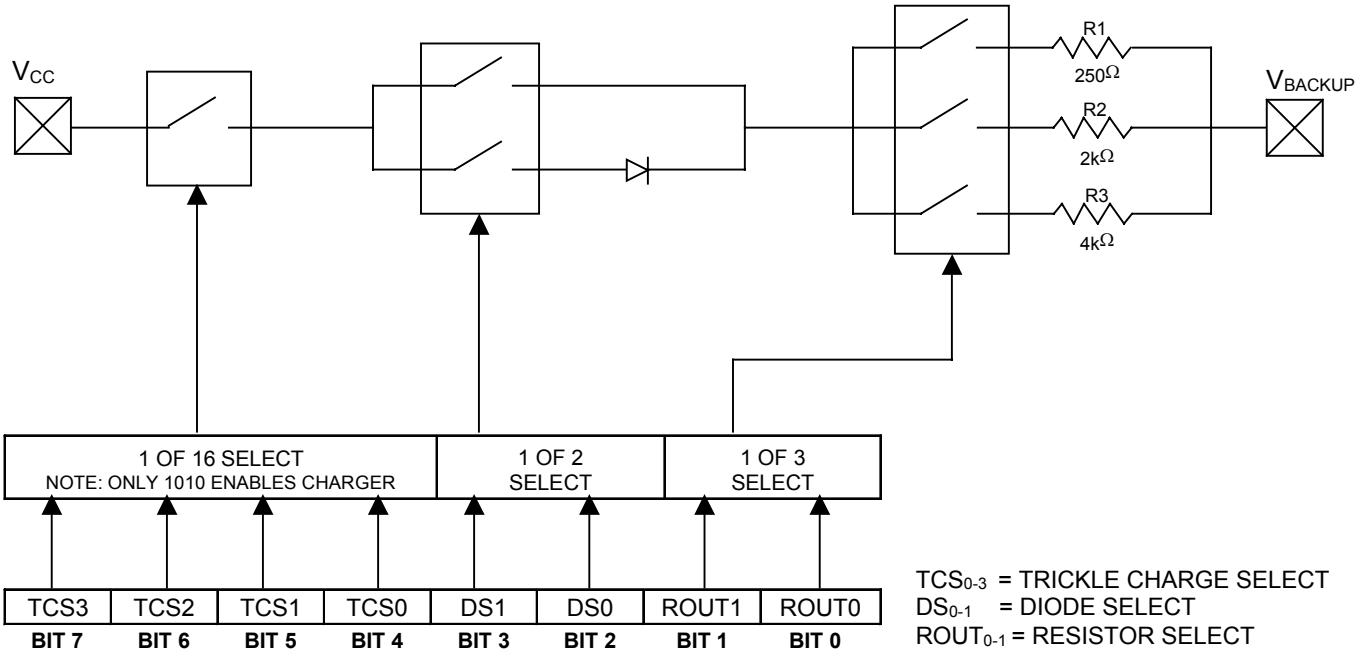
The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example:

Assume that a system power supply of 3.3V is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would, therefore, be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap or battery charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and, therefore, the charge current decreases.

Figure 6. PROGRAMMABLE TRICKLE CHARGE



2-WIRE SERIAL DATA BUS

The DS1339 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1339 operates as a slave on the 2-wire bus. Connections to the bus are made by the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 7):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

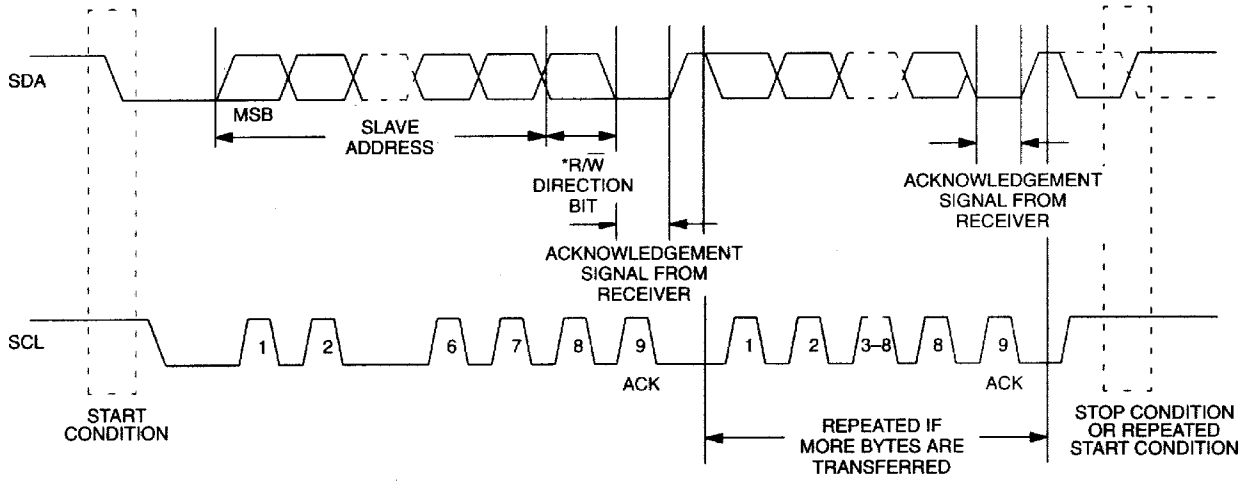
Data Valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 7. DATA TRANSFER ON 2-WIRE SERIAL BUS



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data Transfer from a Master Transmitter to a Slave Receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data Transfer from a Slave Transmitter to a Master Receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the MSB first.

The DS1339 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 8). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1339 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a write, is a 0. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. After the DS1339 acknowledges the slave address + write bit, the master transmits a register address to the DS1339. This sets the register pointer on the DS1339, with the DS1339 acknowledging the transfer. The master can then transmit zero or more bytes of data, with the DS1339 acknowledging each byte received. The address pointer increments after each byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1339 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 9). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1339 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which, for a read, is a 1. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. The DS1339 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The address pointer is incremented after each byte is transferred. The DS1339 must receive a "not acknowledge" to end a read.

Figure 8. DATA WRITE: SLAVE RECEIVER MODE

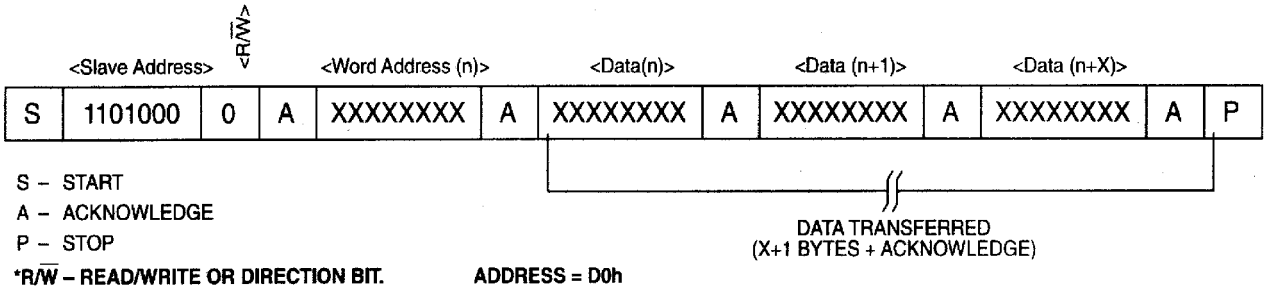
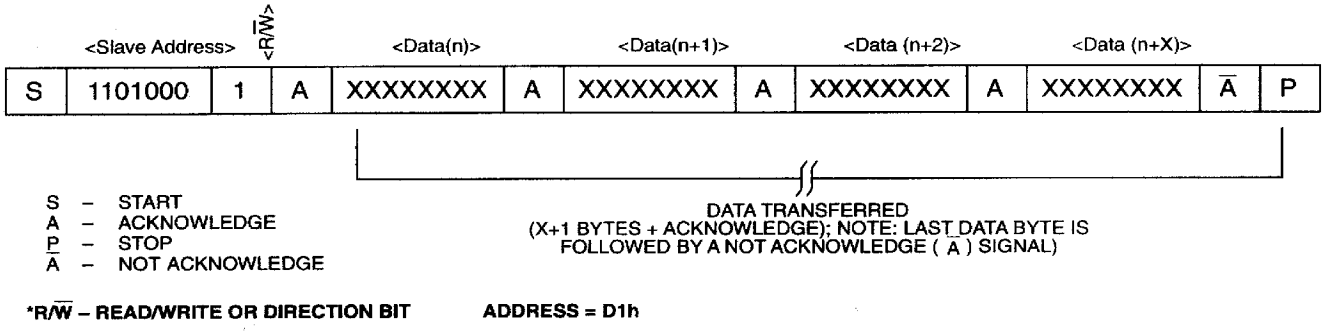


Figure 9. DATA READ: SLAVE TRANSMITTER MODE



ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature Range	See IPC/JEDEC J-STD-020A

**This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS (T_A = -40°C to +85°C) (Note 12)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage, DS1339-2	V_{CC}	1.8	2.0	2.2	V	
Supply Voltage, DS1339-3	V_{CC}	2.7	3.0	3.3	V	
Supply Voltage, DS1339-33	V_{CC}	2.97	3.3	3.63	V	
Backup Supply Voltage	V_{BACKUP}	1.3	3.0	3.7	V	
Logic 1	V_{IH}	0.7 V_{CC}		V_{CC} + 0.5	V	
Logic 0	V_{IL}	-0.5		0.3 V_{CC}	V	
Power-Fail Voltage, DS1339-2	V_{PF}	1.58	1.70	1.80	V	
Power-Fail Voltage, DS1339-3	V_{PF}	2.45	2.59	2.70	V	
Power-Fail Voltage, DS1339-33	V_{PF}	2.70	2.85	2.97	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = MIN to MAX, T_A = -40°C to +85°C) (Note 12)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}			1	µA	1
I/O Leakage	I_{LO}			1	µA	2
Logic 0 Out V_{OL} = 0.4V, V_{CC} > V_{CC} Min (-3, -33), V_{CC} ≥ 2.0V (-2)	I_{OL}			3	mA	2
Logic 0 Out V_{OL} = 0.2 (V_{CC}) 1.8V < V_{CC} < 2.0V (DS1339-2)	I_{OL}			3	mA	2
Logic 0 Out V_{OL} - 0.2 (V_{CC}) 1.3V < V_{CC} < 1.8V (DS1339-2)	I_{OL}			250	µA	2
V_{CC} Active Current	I_{CCA}			450	µA	3
Vcc Standby Current	I_{CCS}		80	150	µA	4
Trickle Charge Resistor Register 10h = A5h, V_{CC} = Typ, V_{BACKUP} = 0V	R1		250		Ω	
Trickle Charge Resistor Register 10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V	R2		2000		Ω	
Trickle Charge Resistor Register 10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V	R3		4000		Ω	
V_{BACKUP} Leakage Current	I_{BKLKG}		25	100	nA	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 0V, T_A = -40°C to +85°C) (Note 12)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{BACKUP} Current $\overline{EOSC}$ = 0, SQW Off	I_{BKOSC}		400	700	nA	10
V_{BACKUP} Current $\overline{EOSC}$ = 0, SQW On	I_{BKSQW}		600	1000	nA	10
V_{BACKUP} Current $\overline{EOSC}$ = 1	I_{BKDR}		10	100	nA	10

CRYSTAL SPECIFICATIONS*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Nominal Frequency	F_O		32.768		kHz	
Series Resistance	ESR			45	kΩ	
Load Capacitance	C_L		6		pF	

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58 *"Crystal Considerations for Dallas Real-Time Clocks" for additional specifications.*

CHIP AND PACKAGE INFORMATION

TRANSISTOR COUNT: 10,950
PROCESS: CMOS

THERMAL RESISTANCE, TYP, µsop: θ_{JA}, +207°C/W, θ_{JC} +40°C/W

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = MIN to MAX, **T_A = -40°C to +85°C**) (Note 12)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	Fast Mode	100		400	kHz	
		Standard Mode			100		
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode	1.3			µs	
		Standard Mode	4.7				
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode	0.6			µs	5
		Standard Mode	4.0				
LOW Period of SCL Clock	t_{LOW}	Fast Mode	1.3			µs	
		Standard Mode	4.7				
HIGH Period of SCL Clock	t_{HIGH}	Fast Mode	0.6			µs	
		Standard Mode	4.0				
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode	0.6			µs	
		Standard Mode	4.7				
Data Hold Time	$t_{HD:DAT}$	Fast Mode	0		0.9	µs	6, 7
		Standard Mode	0				
Data Setup Time	$t_{SU:DAT}$	Fast Mode	100			ns	9
		Standard Mode	250				
Rise Time of Both SDA and SCL Signals	t_R	Fast Mode	$20 + 0.1C_B$		300	ns	8
		Standard Mode			1000		
Fall Time of Both SDA and SCL Signals	t_F	Fast Mode	$20 + 0.1C_B$		300	ns	8
		Standard Mode					
Setup Time for STOP Condition	$t_{SU:STO}$	Fast Mode	0.6			µs	
		Standard Mode	4.0				
Capacitive Load for Each Bus Line	C_B				400	pF	8
I/O Capacitance	$C_{I/O}$			10		pF	
Oscillator Stop Flag (OSF) Delay	t_{OSF}			100		ms	11

Figure 10. TIMING DIAGRAM

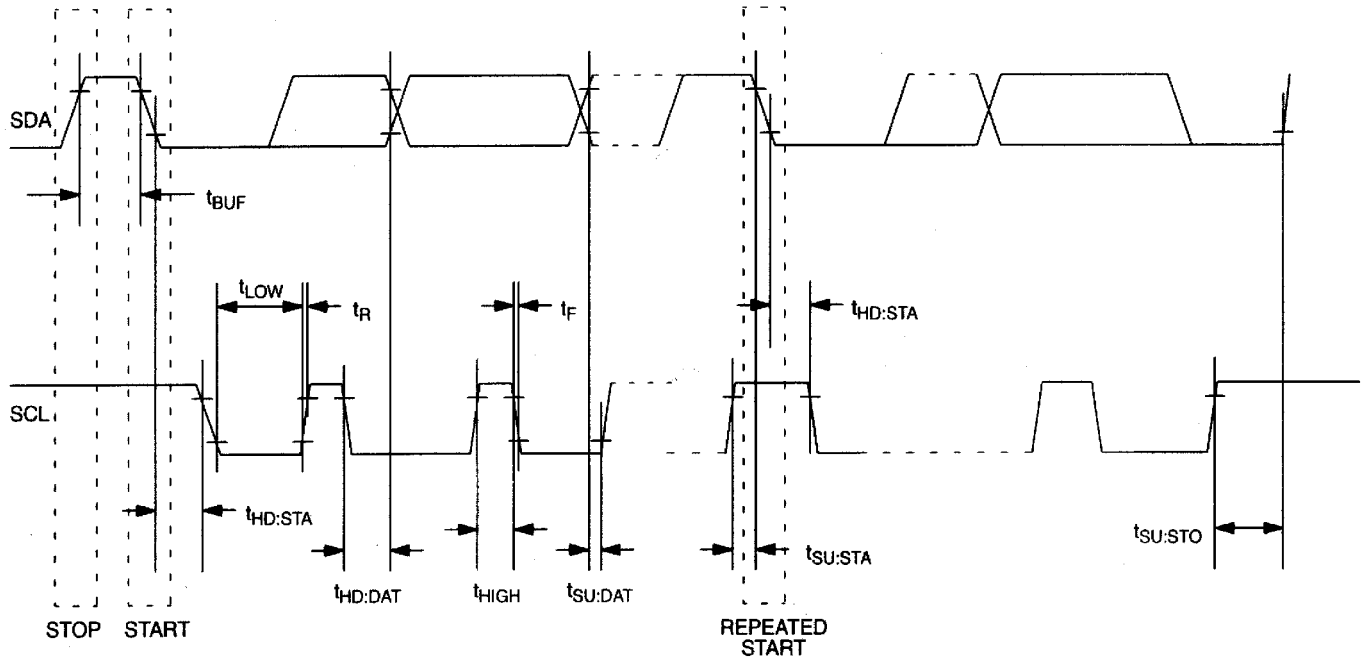
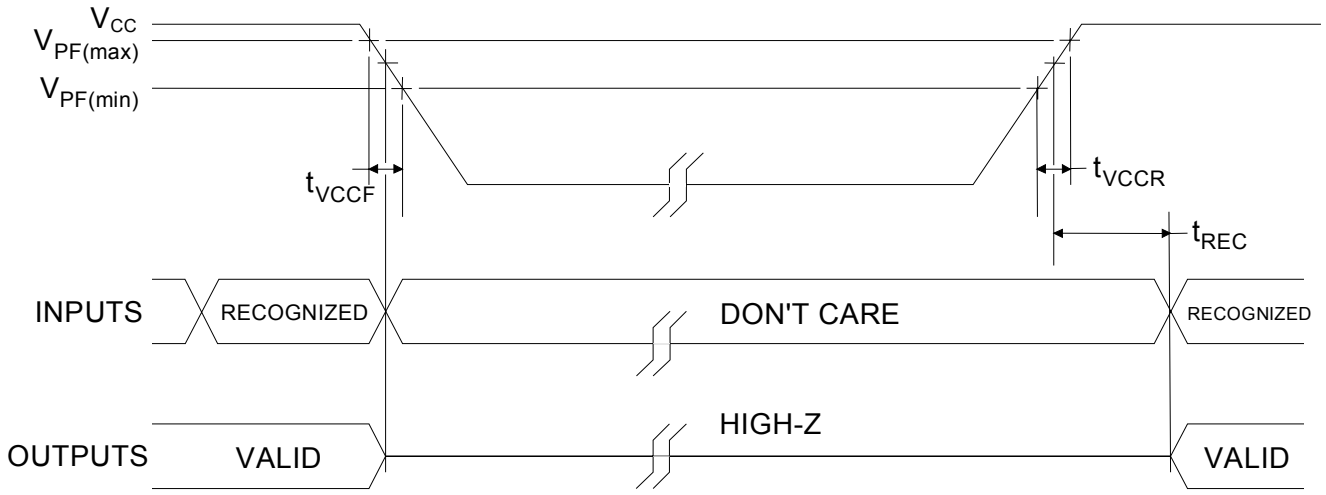


Figure 11. POWER-UP/DOWN TIMING



POWER-UP DOWN CHARACTERISTICS (T_A = -40°C to +85°C) (Note 12)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-up	t_{REC}			2	ms	13
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}	300			µs	
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}	0			µs	

Warning: Under no circumstances are negative undershoots, of any amplitude, allowed when the device is in backup-battery mode.

NOTES:

1) SCL only.
2) SDA, and SQW/$\overline{INT}$.
3) I_{CCA}: SCL at f_{SC} max, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charge disabled.
4) Specified with 2-wire bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charge disabled.
5) After this period, the first clock pulse is generated.
6) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8) C_B: Total capacitance of one bus line in pF.
9) A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
10) Using recommended crystal on X1 and X2.
11) The parameter t_{OSF} is the period of time the oscillator must be stopped in order for the OSF flag to be set over the voltage range of $0V \leq V_{CC} \leq V_{CCMAX}$ and $1.3V \leq V_{BACKUP} \leq 3.7V$.
12) Limits at -40°C are guaranteed by design and are not production tested.
13) This delay applies only if the oscillator is running. If the oscillator is disabled or stopped, no power-up delay occurs.