DALLAS SEMICONDUCTOR

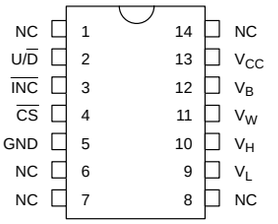
DS1666, DS1666S
Audio Digital Resistor

FEATURES

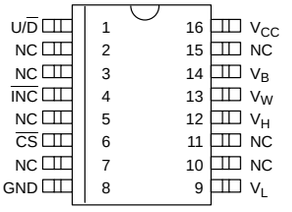
- 128 position, digitally controlled potentiometer
- Operates from a +5 volts power supply with TTL signal inputs
- Wide analog voltage range of ±5 volts
- Resistive elements are temperature compensated to ±20 percent end to end
- Low–power CMOS
- 14–pin DIP or 16–pin SOIC for surface mount applications
- Default position on power up sets wiper position at 10%
- Operating temperature range
  - –40°C to +85°C; industrial

		Resolution/Step		
Resistance values		Low End	High End	–3dB Point
DS1666–10	10KΩ	24Ω	152Ω	1.1 MHz
DS1666–50	50KΩ	122Ω	759Ω	200 KHz
DS1666–100	100KΩ	243Ω	1.519KΩ	100 KHz

PIN ASSIGNMENT



14–PIN DIP (300 MIL)
See Mech. Drawings Section



16–PIN SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

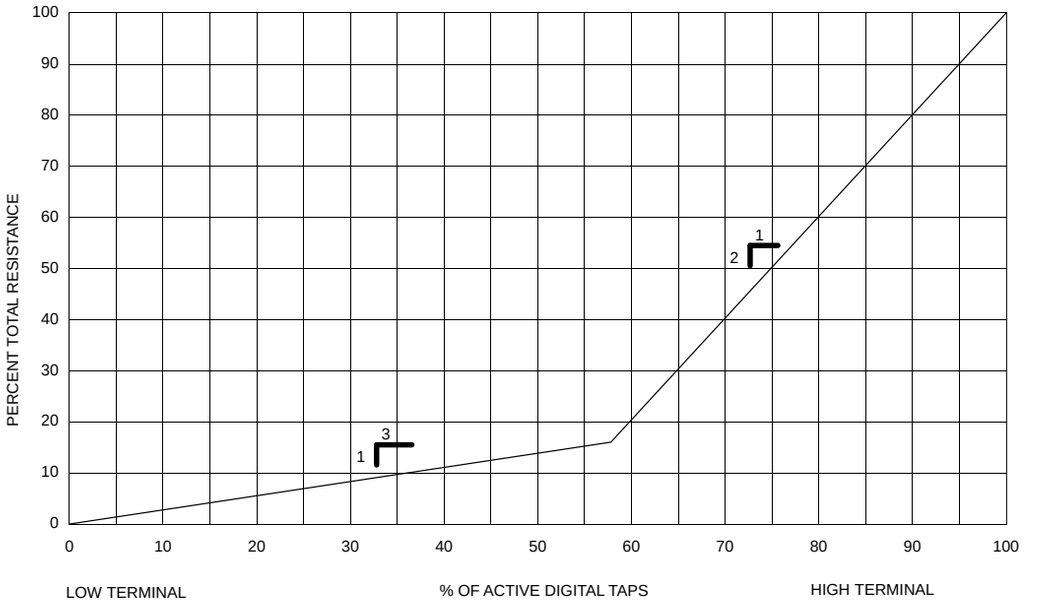
V_H	–	High Terminal of Resistor
V_L	–	Low Terminal of Resistor
V_W	–	Wiper Terminal of Resistor
U/$\overline{D}$	–	Up/Down Control
$\overline{INC}$	–	Wiper Movement Control
$\overline{CS}$	–	Chip Select for Wiper Movement
NC	–	No Connection
V_{CC}	–	+5 Volts
GND	–	Ground
V_B	–	0 to –5 Volts

DESCRIPTION

The DS1666 is a solid–state potentiometer which is set to value by digitally controlled resistive elements. The potentiometer is composed of 127 resistive sections. Between each resistive section and both ends of the potentiometer are TAP points accessible to the wiper. The position of the wiper on the resistance array is controlled by the $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$ inputs. The position of the wiper defaults to the 10% position on power up. The resolution of the DS1666 is shown in Figure 1.

The DS1666 Digital Audio Resistor is uniquely designed to provide a potentiometer that is logarithmic rather than linear across its entire range. The lower half of the potentiometer advances 1% of total resistance for each 3% of scale advanced, providing for precise amplification of low volume signals. The upper half of the potentiometer advances 2% of resistance for every 1% of scale advanced, providing for the lower resolution gain required for high volume amplification.

GRAPH OF AUDIO TAPER Figure 1



OPERATION

The $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$ inputs control the position of the wiper along the resistor array (Figure 1). When $\overline{CS}$ is active (low), a high to low transition on the $\overline{INC}$ will increment or decrement an internal counter depending on the level of the U/$\overline{D}$ pin. When the U/$\overline{D}$ pin is low, the counter will decrement. When the U/$\overline{D}$ pin is high, the counter will increment. The state of the U/$\overline{D}$ pin can be changed while $\overline{CS}$ is active allowing for precise adjustment during calibration. The output of the counter is decoded to set the position of the wiper. When the $\overline{CS}$ input transitions to the high (inactive) level, the value of the counter is stored and the wiper position is maintained until power (V_{CC}) is lost. When power is restored, the DS1666 returns to the default setting and positions the wiper to 10 percent. The value of the end–to–end and end–to–wiper position is indeterminate while V_{CC} is not applied.

The DS1666 has a resistor array that resembles an audio taper potentiometer as shown in Figure 1 1. Since the taper is not linear, exact resistance values for each of the 128 positions of the resistor is not specified. However, the end-to-end resistance is specified to be within ±20 percent of the stated resistor value over an industrial temperature range of –40°C to +85°C.

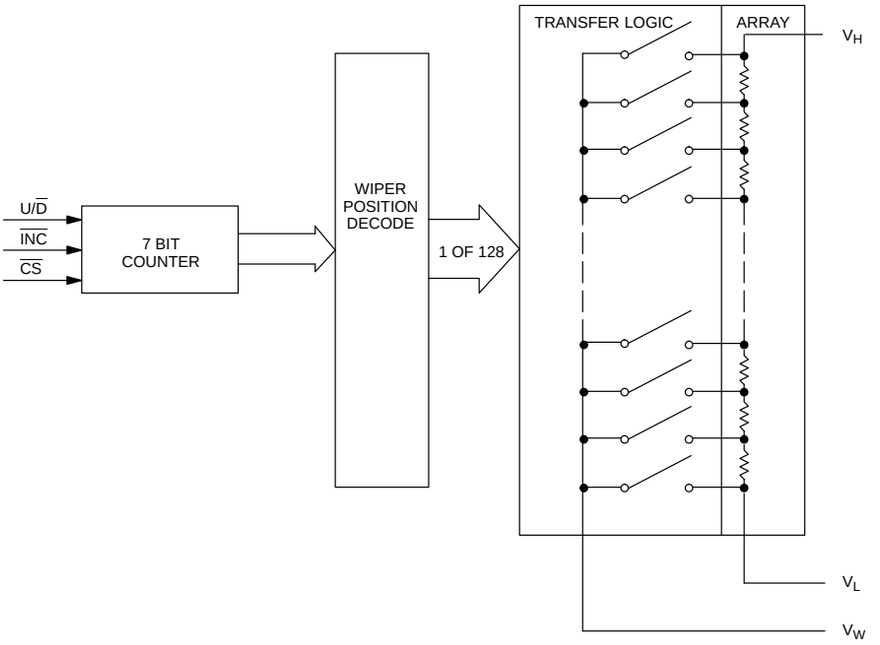
ANALOG CHARACTERISTICS

End–to–End Resistance Tolerance = ±20 percent
Typical Noise = <120 dB/Hz REF:IV
Temperature Coefficient = ±800 PPM/°C typical
Resistance at tap #74=18% ± 2% of total resistance.

PIN DESCRIPTIONS

V_H	The high end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_L	The Low end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_W	The wiper terminal of the potentiometer. The value of the wiper is controlled by the U/$\overline{D}$ and the $\overline{INC}$ pins.
Up/Down (U/$\overline{D}$)	The U/$\overline{D}$ input controls the direction of the wiper movement when setting the potentiometer.
Increment ($\overline{INC}$)	Toggling $\overline{INC}$ will move the potentiometer wiper by either incrementing or decrementing the counter.
Chip Select ($\overline{CS}$)	The device is selected when $\overline{CS}$ input is low. The current counter value is stored when CS is returned high.

BLOCK DIAGRAM Figure 2



MODE SELECTION Figure 3

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↓	H	WIPER UP
L	↓	L	WIPER DOWN
↑	H	X	STORE WIPER POSITION

ABSOLUTE MAXIMUM RATINGS*

Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, and V_{CC} Relative to Ground	–0.5V to +7.0V
Voltage on V_H, V_L, and V_W Relative to Ground	–6.5V to +6.5V
Voltage on V_B	–6.5V to Ground
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	–0.5		+0.8	V	1
V_H, V_L, V_W Voltage	V_R	V_B–0.3		V_{CC}+0.3	V	1
V_B Voltage	V_B	–5.5		GND	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		0.1	5	mA	3
Input Leakage	I_{LI}	–1		+1	µA	2
Wiper Resistance	R_W		350	650	Ω	
Wiper Current	I_W			1	mA	3

CAPACITANCE

(t_A = 25°C)

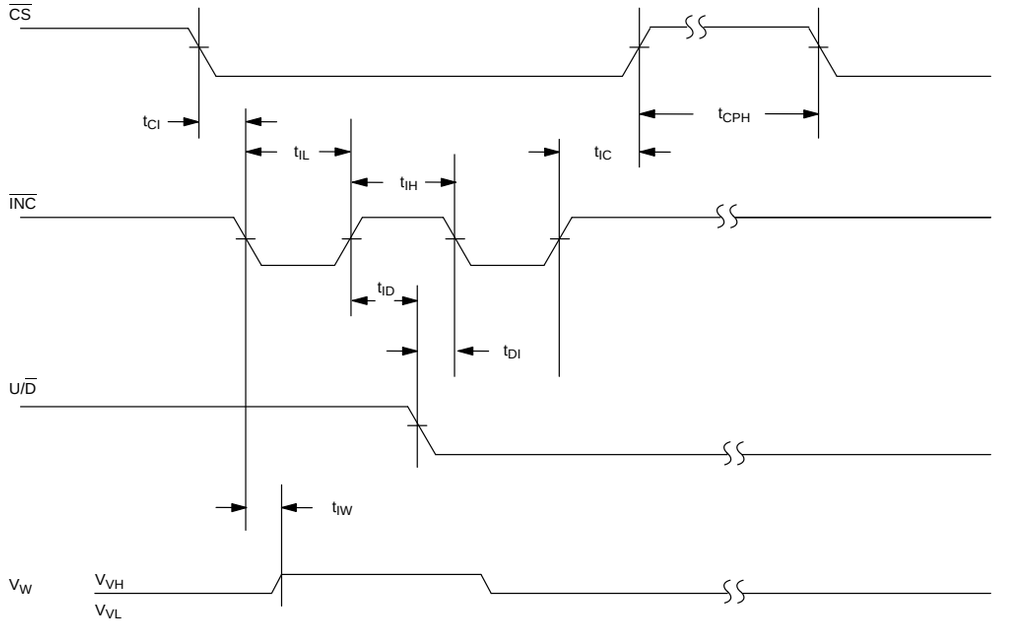
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Capacitance	C_{IN}	t_A=25°C	6	10	pF	2

AC ELECTRICAL CHARACTERISTICS

(t_A=–40°C to +85°C; V_{CC}=+5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}	100			ns	
$\overline{INC}$ High to U/$\overline{D}$ Change	t_{ID}	100			ns	
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}	1			µs	
$\overline{INC}$ Low Period	t_{IL}	500			ns	
INC High Period	t_{IH}	1			µs	
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}	500			ns	
$\overline{CS}$ Deselect Time	t_{CPH}	100			ns	

AC TIMING Figure 4



NOTES:

1. All voltages are referenced to ground.
2. This parameter is periodically sampled and not 100% tested.
3. Typical values are for t_A = 25°C and nominal supply voltages.
4. Wiper output open circuited.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10 ns
Input Level	1.5V

DS1666 ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	OPERATING TEMPERATURE	VERSION
DS1666–010	14L DIP	–40°C TO +85°C	10KΩ
DS1666–050	14L DIP	–40°C TO +85°C	50KΩ
DS1666–100	14L DIP	–40°C TO +85°C	100KΩ
DS1666S–010	16L SOIC (300 MIL)	–40°C TO +85°C	10KΩ
DS1666S–050	16L SOIC (300 MIL)	–40°C TO +85°C	50KΩ
DS1666S–100	16L SOIC (300 MIL)	–40°C TO +85°C	100KΩ

DATA SHEET REVISION SUMMARY

The following represent the key differences between 07/26/93 and 06/18/97 version of the DS1666 data sheet. Please review this summary carefully.

1. Remove commercial temp grade reference
2. Add order info table