National Semiconductor

DS26S10C/DS26S10M/DS26S11C/DS26S11M Quad Bus Transceivers

General Description

The DS26S10 and DS26S11 are quad Bus Transceivers consisting of 4 high speed bus drivers with open-collector outputs capable of sinking 100 mA at 0.8V and 4 high speed bus receivers. Each driver output is connected internally to the high speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active low enable gate controls the 4 drivers so that outputs of different device drivers can be connected together for party-line operation.

The bus output high-drive capability in the low state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2V.

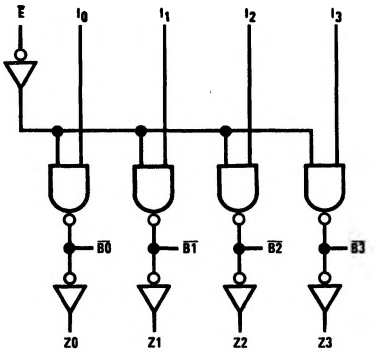
The DS26S10 and DS26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has 2 ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND 1 and GND 2 should be tied to the ground bus external to the device package.

Features

- Input to bus is inverting on DS26S10
- Input to bus is non-inverting on DS26S11
- Quad high speed open-collector bus transceivers
- Driver outputs can sink 100 mA at 0.8V maximum
- Advanced Schottky processing
- PNP inputs to reduce input loading

Logic Diagrams

DS26S10



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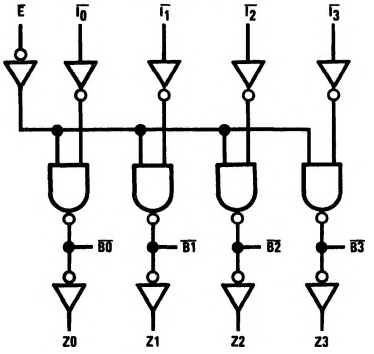
DS26S11



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} Max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5 mA

Maximum Power Dissipation* at 25°C

Cavity Package	1433 mW
Molded Package	1362 mW
PLCC Package	TBD mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C, derate PLCC package TBD mW/°C above 25°C.

Operating Conditions

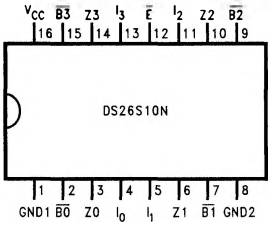
	Min	Max	Units
Supply Voltage (V_{CC})			
DS26S10C, DS26S11C	4.75	5.25	V
DS26S10M, DS26S11M	4.5	5.5	V
Temperature (T_A)			
DS26S10C, DS26S11C	0	+70	°C
DS26S10M, DS26S11M	−55	+125	°C

Electrical Characteristics (Unless otherwise noted)

Symbol	Parameter	Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage (Receiver Outputs)	V_{CC} = Min, I_{OH} = −1 mA, V_{IN} = V_{IL} or V_{IH}	Military	2.5	3.4		V
			Commercial	2.7	3.4		V
V_{OL}	Output Low Voltage (Receiver Outputs)	V_{CC} = Min, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input High Level (Except Bus)	Guaranteed Input Logical High for All Inputs		2.0			V
V_{IL}	Input Low Level (Except Bus)	Guaranteed Input Logical Low for All Inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 2.7V	Enable			20	μA
			Data			30	μA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short-Circuit Current (Except Bus)	V_{CC} = Max, (Note 3)	Military	−20		−55	mA
			Commercial	−18		−60	mA
I_{CCL}	Power Supply Current (All Bus Outputs Low)	V_{CC} = Max, Enable = GND	DS26S10		45	70	mA
			DS26S11			80	mA

Connection Diagrams

Dual-In-Line Package



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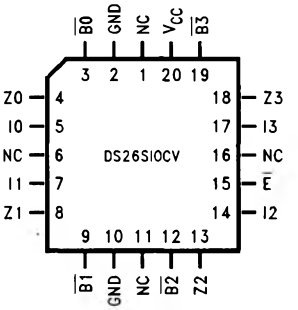
Top View
Order Number DS26S10CJ, DS26S10MJ or DS26S10CN
See NS Package Number J16A or N16A
Plastic Chip Carrier



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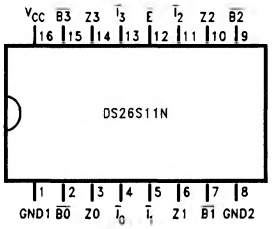
Top View

Order Number DS26S10CV
See NS Package Number V20A

Dual-In-Line Package



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Top View
Order Number DS26S11CJ, DS26S11MJ or DS26S11CN
See NS Package Number J16A or N16A

Bus Input/Output Characteristics

Symbol	Parameter	Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OL}	Output Low Voltage	V_{CC} = Min	Military	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Commercial	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = Max		V_O = 0.8V			−50	μA
			Military	V_O = 4.5V			200	
			Commercial	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4V, V_{CC} = Max		Military	2.4	2.0		V
				Commercial	2.25	2.0		
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4V, V_{CC} = Min		Military		2.0	1.6	V
				Commercial		2.0	1.75	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = 25°C, V_{CC} = 5V)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	R_B = 50Ω, C_B = 50 pF (Note 1)	DS26S10		10	15	ns
t_{PHL}	Data Input to Bus				10	15	ns
t_{PLH}	Data Input to Bus		DS26S11		12	19	ns
t_{PHL}	Data Input to Bus				12	19	ns
t_{PLH}	Enable Input to Bus		DS26S10		14	18	ns
t_{PHL}	Enable Input to Bus				13	18	ns
t_{PLH}	Enable Input to Bus		DS26S11		15	20	ns
t_{PHL}	Enable Input to Bus				14	20	ns
t_{PLH}	Bus to Receiver Out	R_B = 50Ω, R_L = 280Ω, C_B = 50 pF (Note 1), C_L = 15 pF			10	15	ns
t_{PHL}	Bus to Receiver Out				10	15	ns
t_r	Bus	R_B = 50Ω, C_B = 50 pF (Note 1)		4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1: Includes probe and jig capacitance.

Truth Tables

DS26S10

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

DS26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

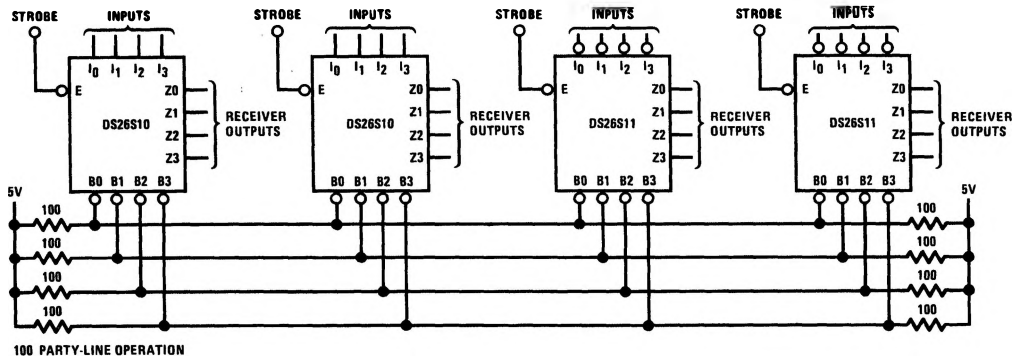
H = High voltage level

L = Low voltage level

X = Don't care

Y = Voltage level of bus (assumes control by another bus transceiver)

Typical Application



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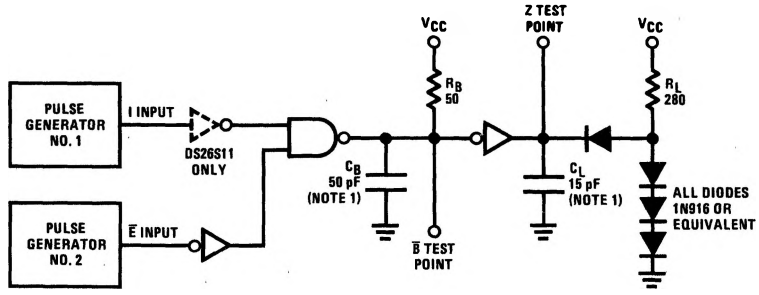
AC Test Circuit and Switching Time Waveforms



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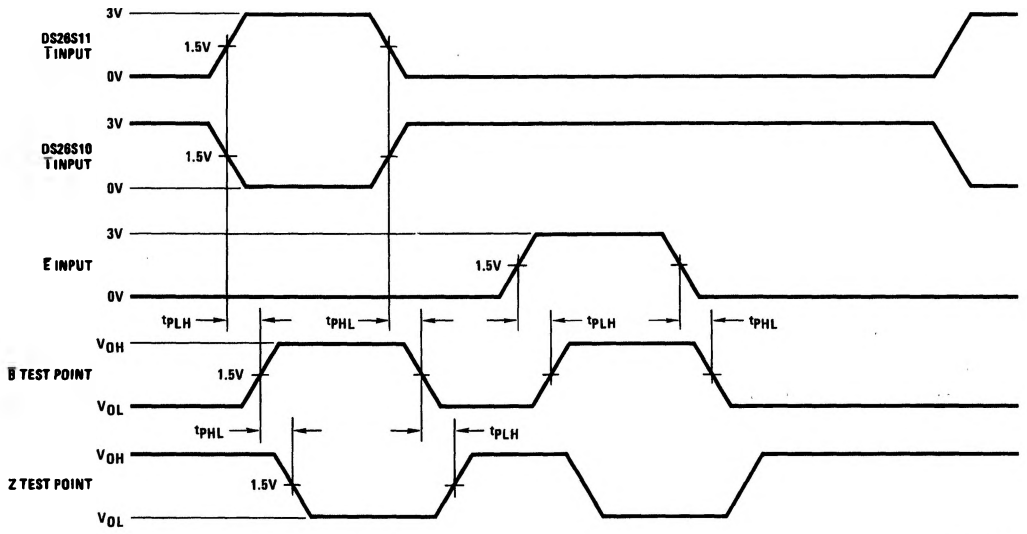
Note 1: Includes probe and jig capacitance.



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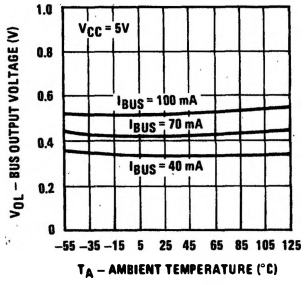
Typical Performance Characteristics

Typical Bus Output Low Voltage vs Ambient Temperature



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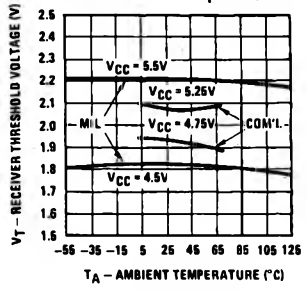
Receiver Threshold Variation vs Ambient Temperature



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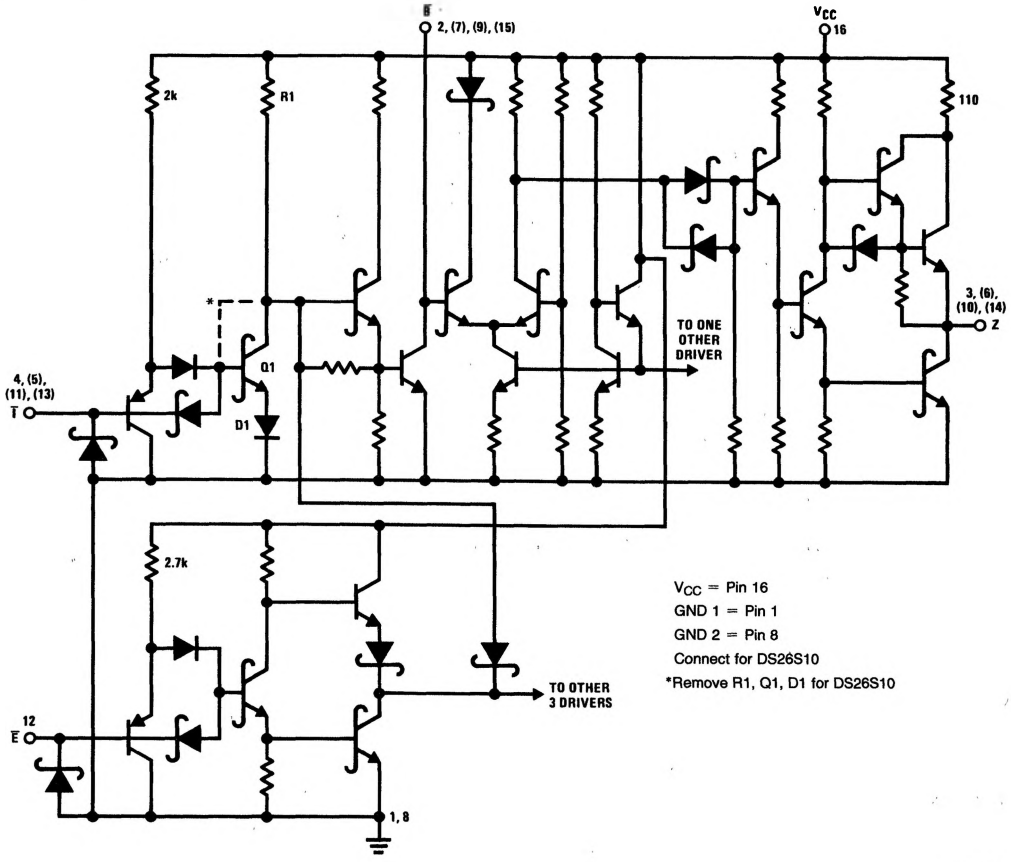
Schematic Diagram



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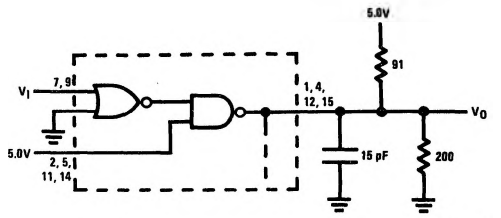
AC Test Circuits and Switching Waveforms



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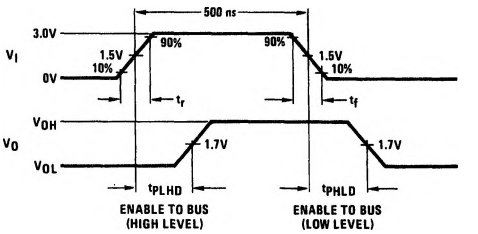

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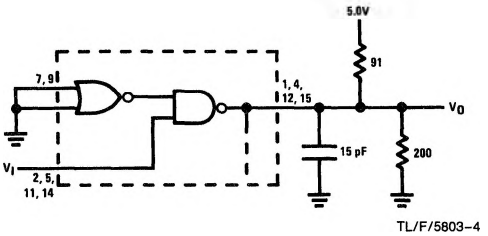
Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 1. Disable Delays



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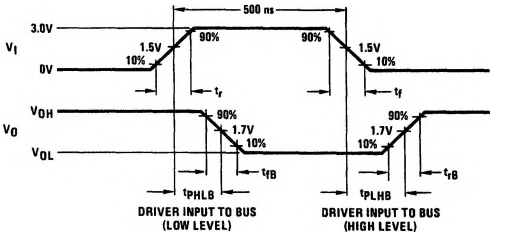

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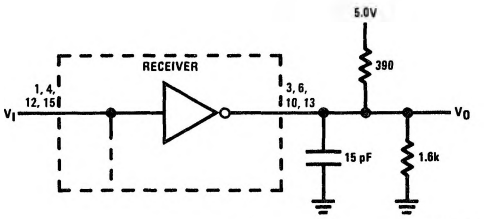
Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 2. Driver Propagation Delays



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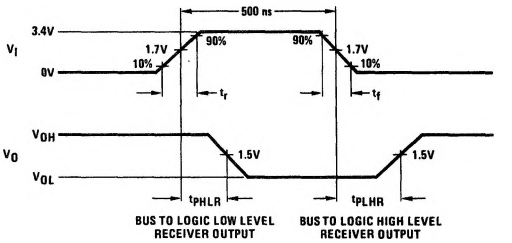

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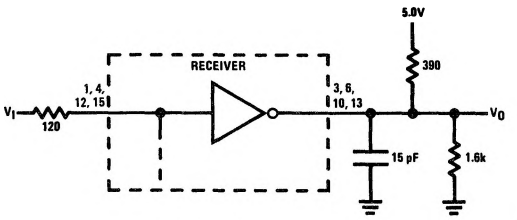
Note: $t_r = t_f = 15$ ns. Pulse width = 500 ns measured between 1.7V levels. f = 1 MHz.

FIGURE 3. Receiver Propagation Delays



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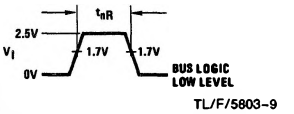

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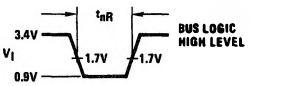
$t_r = t_f = 2.5$ ns

(a) Receiver Output (V_O) to Remain Greater than 2.2V



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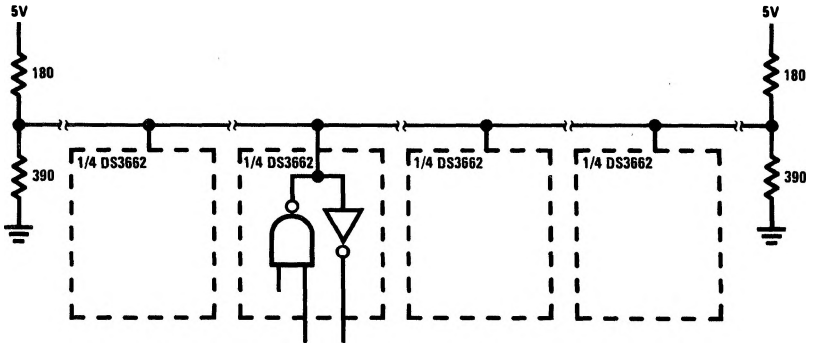
$t_r = t_f = 2.5$ ns

(b) Receiver Output (V_O) to Remain Less than 0.7V

FIGURE 4. Receiver Noise Immunity: "No Response at Output" Input Waveforms

Typical Application

120Ω Unified Data Bus



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