National Semiconductor

DS55451/2/3/4, DS75450/1/2/3/4 Series Dual Peripheral Drivers

General Description

The DS75450 series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

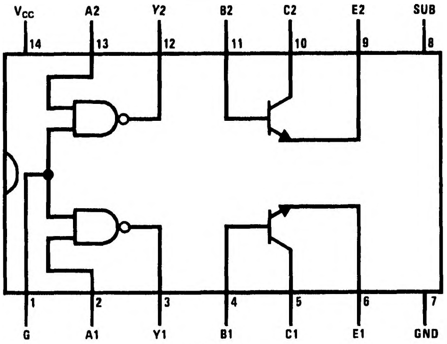
The DS75450 is a general purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. The device offers the system designer the flexibility of tailoring the circuit to the application.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

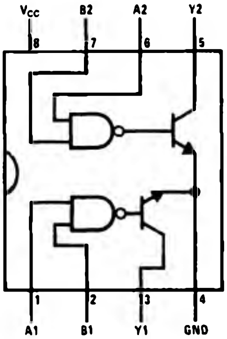
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

Connection Diagrams (Dual-In-Line and Metal Can Packages)



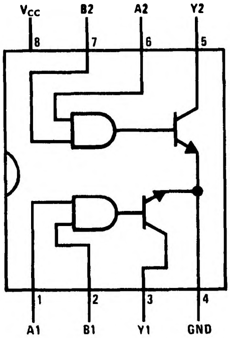
TL/F/5824-1

Top View
Order Number DS75450N
See NS Package Number N14A



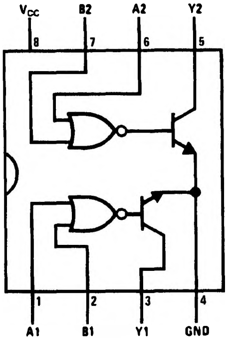
TL/F/5824-2

Top View
Order Number DS55451J-8, DS75451M or DS75451N



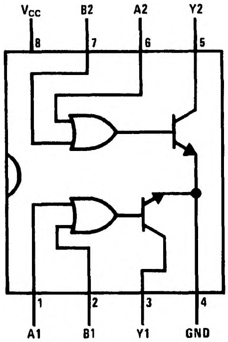
TL/F/5824-3

Top View
Order Number DS55452J-8, DS75452M or DS75452N



TL/F/5824-4

Top View
Order Number DS55453J-8, DS75453M or DS75453N



TL/F/5824-5

Top View
Order Number DS55454J-8, DS75454M or DS75454N

See NS Package Numbers J08A, M08A* or N08E

*See Note 6 and Appendix E regarding S.O. package power dissipation constraints.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS75450	35V
Collector-to-Substrate Voltage	
DS75450	35V
Collector-Base Voltage	
DS75450	35V
Collector-Emitter Voltage (Note 4)	
DS75450	30V
Emitter-Base Voltage	
DS75450	5.0V
Output Voltage (Note 5)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Collector Current (Note 6)	
DS75450	300 mA
Output Current (Note 6)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
DS75450 Maximum Power (Note 6)	
Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
DS75451/2/3/4 Maximum Power (Note 6)	
Dissipation† at 25°C	
Cavity Package	1090 mW
Molded DIP Package	957 mW
TO-5 Package	760 mW
SO Package	632 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

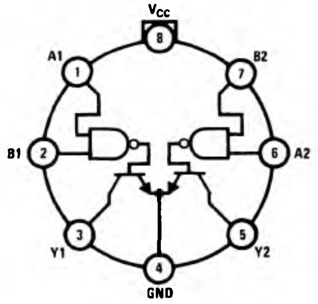
Operating Conditions (Note 7)

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

†Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C; derate SO package 7.56 mW/°C above 25°C.

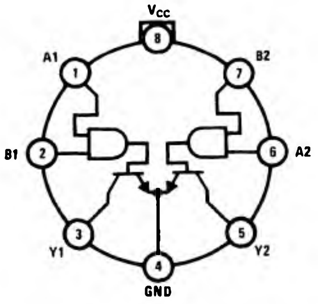
Connection Diagrams (Dual-In-Line and Metal Can Packages) (Continued)



TL/F/5824-6

Top View

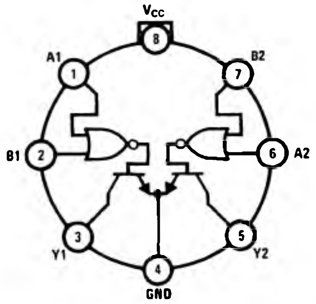
Order Number DS55451H



TL/F/5824-7

Top View

Order Number DS55452H



TL/F/5824-8

Top View

(Pin 4 is in Electrical Contact with the Case)

Order Number DS55453H

See NS Package Number H08C

Electrical Characteristics DS75450 (Notes 8 and 9)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TTL GATES							
V_{IH}	High Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400 μA, *(Figure 2)*		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA *(Figure 1)*			0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*	Input A			1	mA
			Input G			2	mA

Electrical Characteristics DS75450 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
TTL GATES (Continued)								
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*		Input A			40	μA
				Input G			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*		Input A			−1.6	mA
				Input G			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, *(Figure 5)*, (Note 10)			−18		−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*				2	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*				6	11	mA
OUTPUT TRANSISTORS								
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0 μA			35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500Ω			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0 μA			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 11)	T_A = +25°C	I_C = 100 mA	25			
				I_C = 300 mA	30			
			T_A = 0°C	I_C = 100 mA	20			
				I_C = 300 mA	25			
V_{BE}	Base-Emitter Voltage	(Note 11)		I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1.05	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 11)		I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.5	0.7	V

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	μA
					DS75451, DS75453			100	μA
				V_{IL} = 0.8V	DS55452, DS55454			300	μA
					DS75452, DS75454			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*					40	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*				−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V	DS55451/DS75451		7	11	mA
			V_I = 0V	DS55452/DS75452		11	14	mA
			V_I = 5V	DS55453/DS75453		8	11	mA
			V_I = 0V	DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V	DS55451/DS75451		52	65	mA
			V_I = 5V	DS55452/DS75452		56	71	mA
			V_I = 0V	DS55453/DS75453		54	68	mA
			V_I = 5V	DS55454/DS75454		61	79	mA

Switching Characteristics DS75450 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		12	22	ns
			R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		8	15	ns
			R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*			7	12	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*			9	15	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, I_C ≈ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S − 6.5			mV
t_D	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			8	15	ns
t_R	Rise Time				12	20	ns
t_S	Storage Time				7	15	ns
t_F	Full Time				6	15	ns

Switching Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, I_O ≈ 300 mA, *(Figure 15)*		V_S − 6.5			mV

Switching Characteristics (Continued)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: Value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.

Note 5: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 6: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 7: For the DS75450 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

Note 8: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS75450 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 10: Only one output at a time should be shorted.

Note 11: These parameters must be measured using pulse techniques. t_W = 300 µs, duty cycle < 2%.

Note 12: Applies to output transistors only.

Truth Tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55452/DS75452

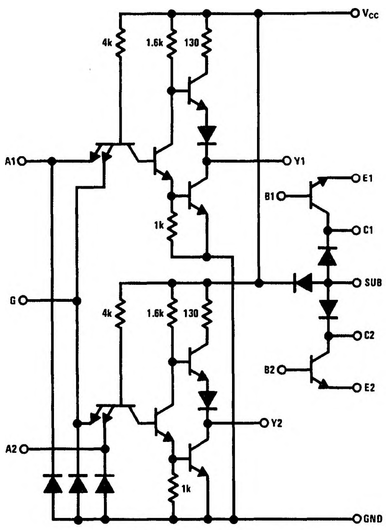
A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

DS55454/DS75454

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

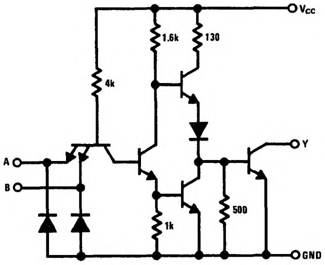
Schematic Diagrams

DS75450



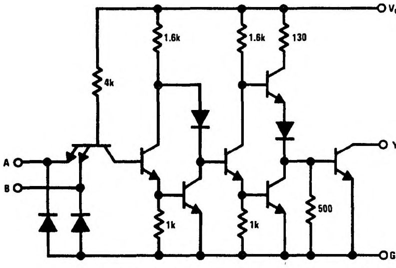
Resistor values shown are nominal. TL/F/5824-10

DS55451/DS75451



Resistor values shown are nominal. TL/F/5824-11

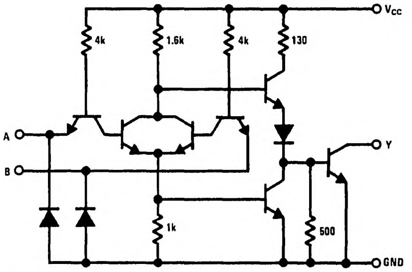
DS55452/DS75452



Resistor values shown are nominal. TL/F/5824-12

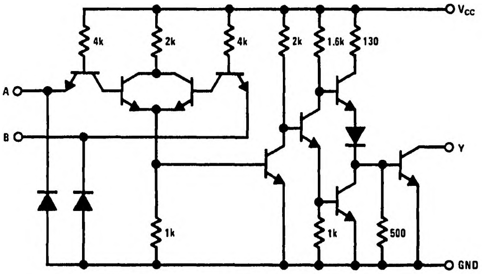
Schematic Diagrams (Continued)

DS55453/DS75453



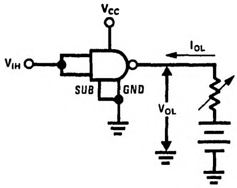
Resistor values shown are nominal. TL/F/5824-13

DS55454/DS75454



Resistor values shown are nominal. TL/F/5824-14

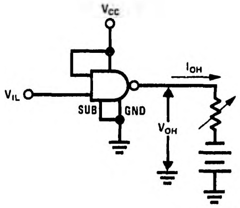
DC Test Circuits



TL/F/5824-15

Both inputs are tested simultaneously.

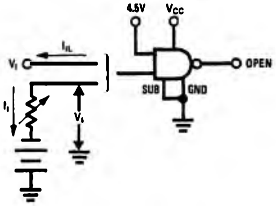
FIGURE 1. V_{IH}, V_{OL}



TL/F/5824-16

Each input is tested separately.

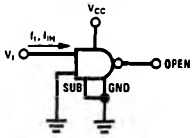
FIGURE 2. V_{IL}, V_{OH}



TL/F/5824-17

Each input is tested separately.

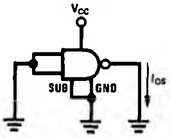
FIGURE 3. V_I, I_{IL}



TL/F/5824-18

Each input is tested separately.

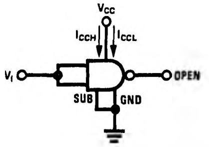
FIGURE 4. I_I, I_{IH}



TL/F/5824-19

Each input is tested separately.

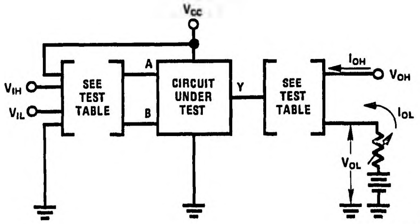
FIGURE 5. I_{OS}



TL/F/5824-20

Both gates are tested simultaneously.

FIGURE 6. I_{CCH}, I_{CCL}

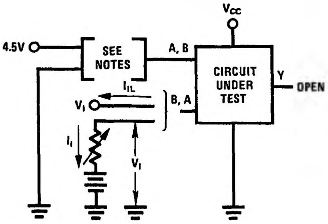


TL/F/5824-21

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55451	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55453	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OH}
DS55454	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}

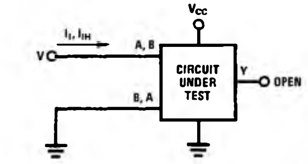
DC Test Circuits (Continued)



Note A: Each input is tested separately.
Note B: When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded.
For all other circuits it is at 4.5V.

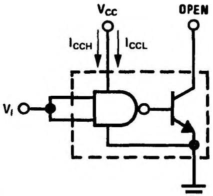
TL/F/5824-22

FIGURE 8. V$_I$, V$_{IL}$



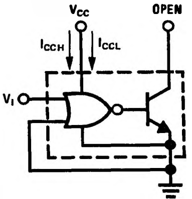
Each input is tested separately. TL/F/5824-23

FIGURE 9. I$_I$, I$_{IH}$



Both gates are tested simultaneously. TL/F/5824-24

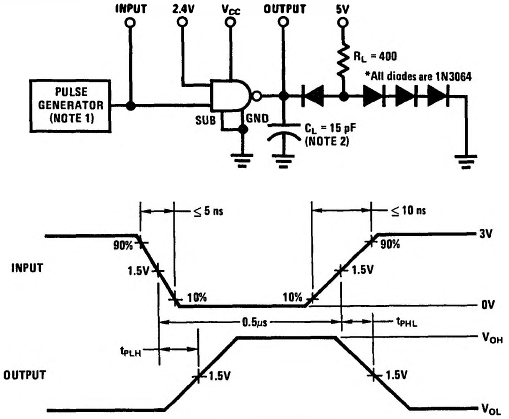
FIGURE 10. I$_{CCH}$, I$_{CCL}$ for AND, NAND Circuits



Both gates are tested simultaneously. TL/F/5824-25

FIGURE 11. I$_{CCH}$, I$_{CCL}$ for OR, NOR Circuits

AC Test Circuits and Switching Time Waveforms



TL/F/5824-26

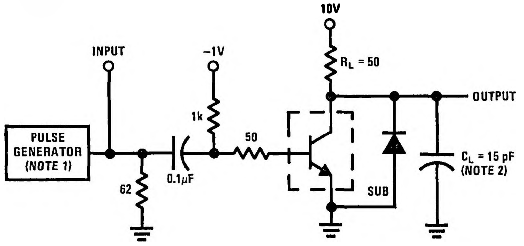
TL/F/5824-27

Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z$_{OUT}$ ≈ 50Ω.

Note 2: C$_L$ includes probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS75450 Only)

AC Test Circuits and Switching Time Waveforms (Continued)



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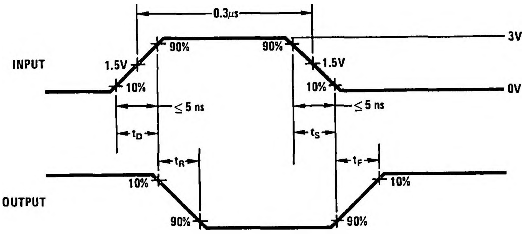

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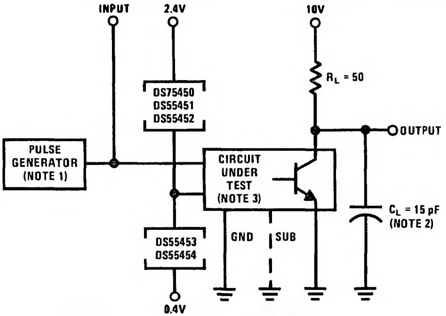
Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor (DS75450 Only)



Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.

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Note 2: C_L includes probe and jig capacitance.

Note 3: When testing DS75450, connect output V to transistor base and ground the substrate terminal.

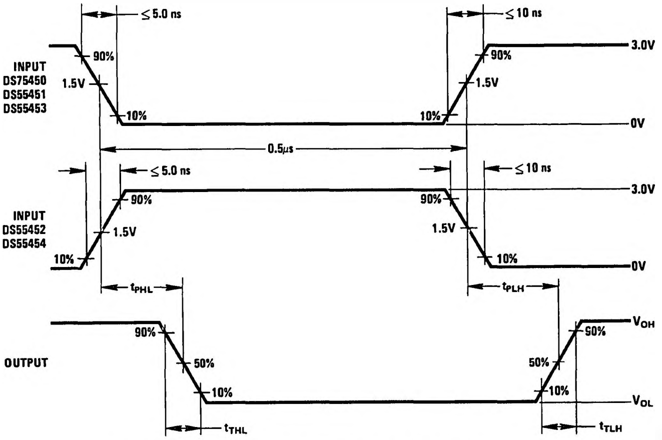

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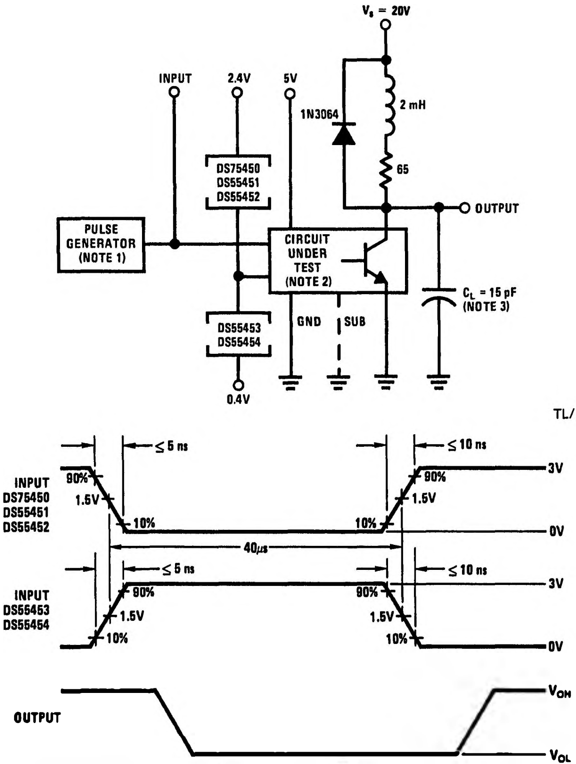
FIGURE 14. Switching Times of Complete Drivers

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824-32

TL/F/5824-33

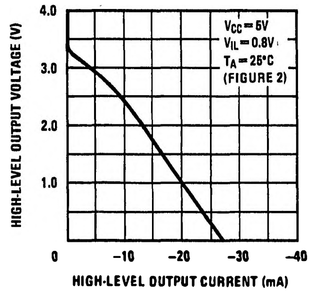
Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: When testing DS75450, connect output V to transistor base with a 600Ω resistor from there to ground and ground the substrate terminal.

Note 3: C_L includes probe and jig capacitance.

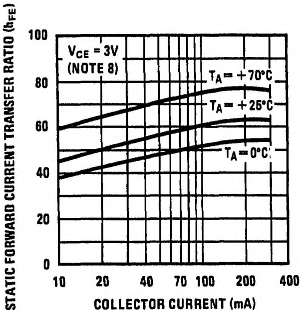
FIGURE 15. Latch-UP Test of Complete Drivers

Typical Performance Characteristics



TL/F/5824-34

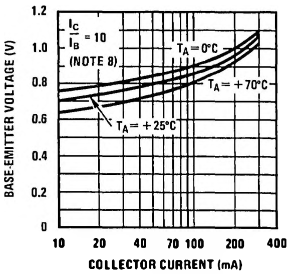
FIGURE 16. DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current



TL/F/5824-35

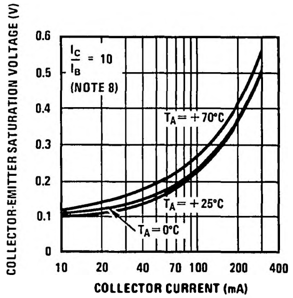
FIGURE 17. DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

Typical Performance Characteristics (Continued)



TL/F/5824-36

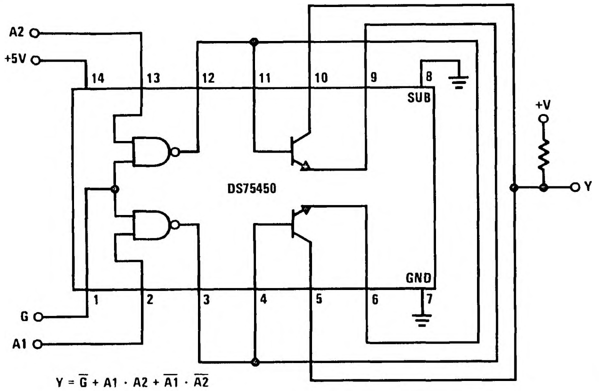
FIGURE 18. DS75450 Transistor Base-Emitter Voltage vs Collector Current



TL/F/5824-37

FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

Typical Applications



$Y = \overline{G} + A1 \cdot A2 + \overline{A1} \cdot \overline{A2}$

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FIGURE 20. Gated Comparator

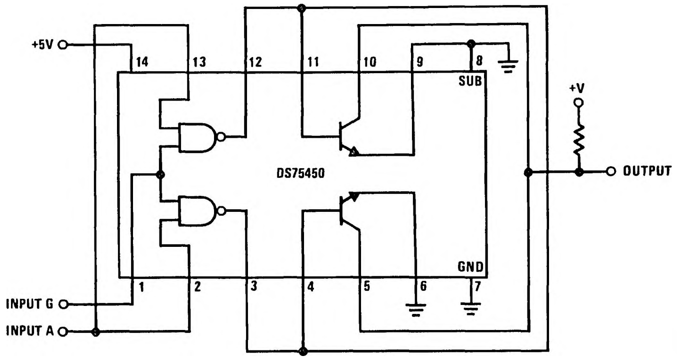

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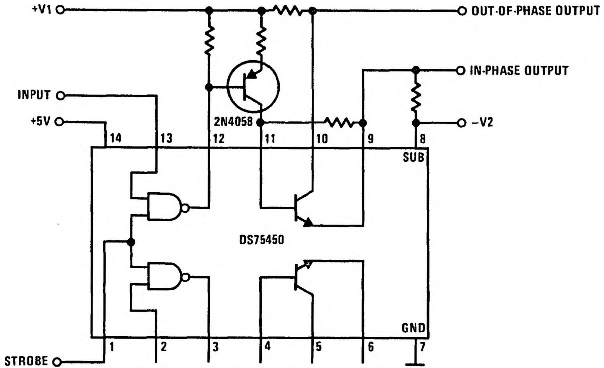
FIGURE 21. 500 mA Sink

Typical Applications (Continued)



This side can perform the same or another function.

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FIGURE 22. Floating Switch

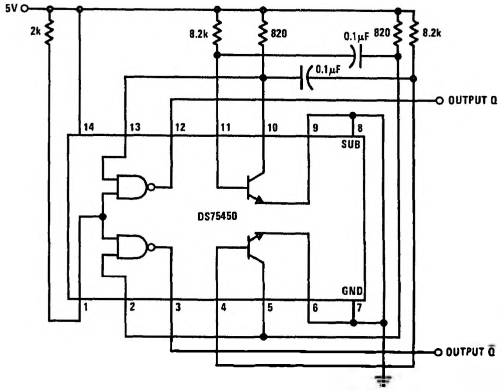

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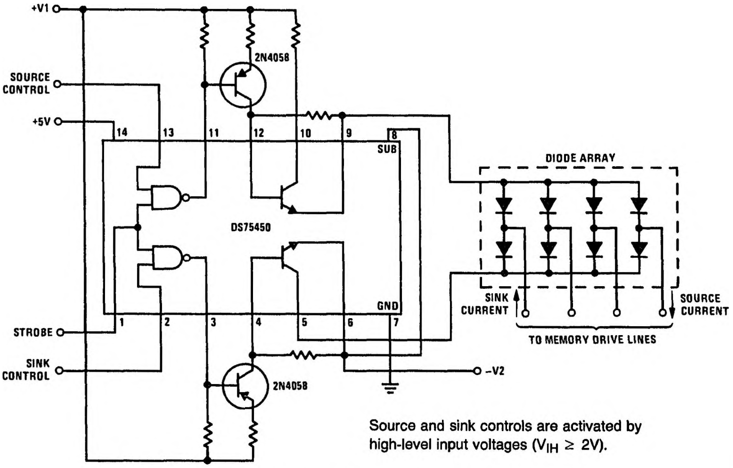
FIGURE 23. Square-Wave Generator



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

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FIGURE 24. Core Memory Driver

Typical Applications (Continued)

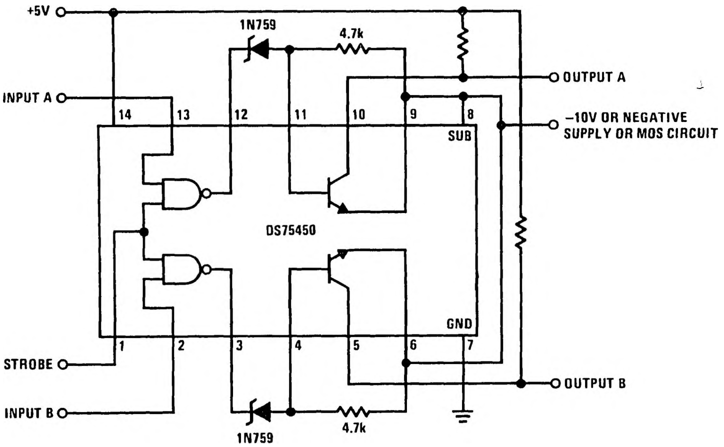

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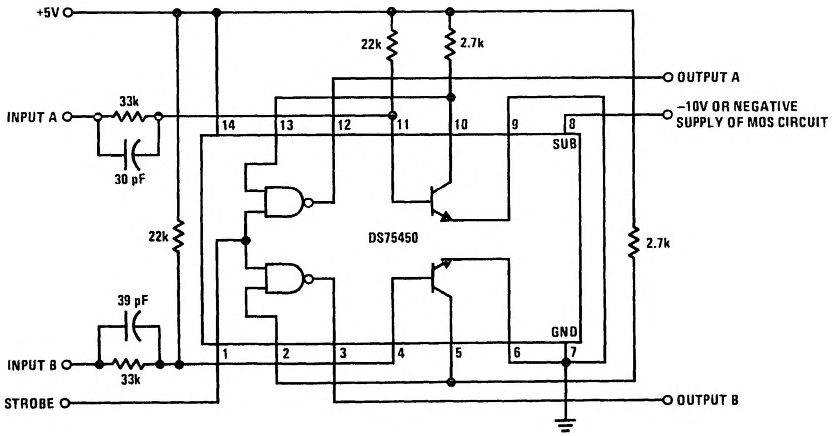
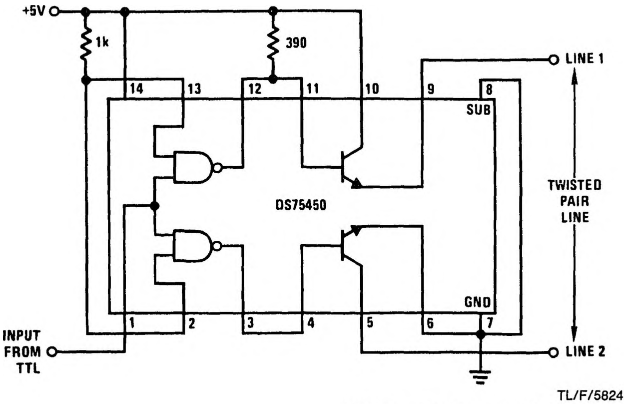
FIGURE 25. Dual TTL-to-MOS Driver



TL/F/5824-44

FIGURE 26. Dual MOS-to-TTL Driver



Termination is made at the receiving end as follows:
Line 1 is terminated to ground through Z_O/Z;
Line 2 is terminated to +5V through Z_O/Z;
where Z_O is the line impedance.

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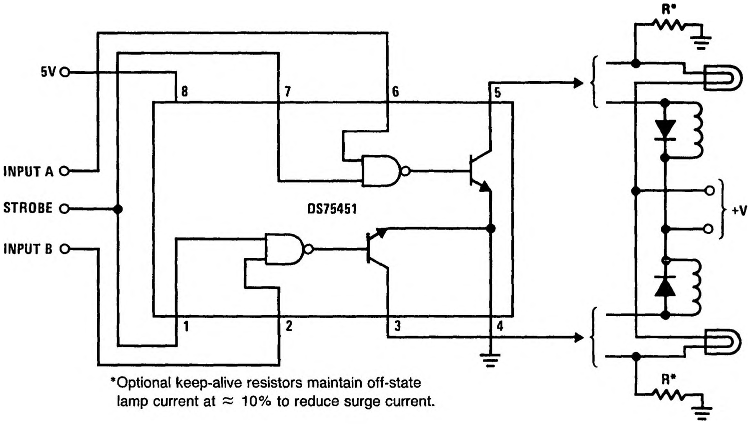
FIGURE 27. Balanced Line Driver

Typical Applications (Continued)



*Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

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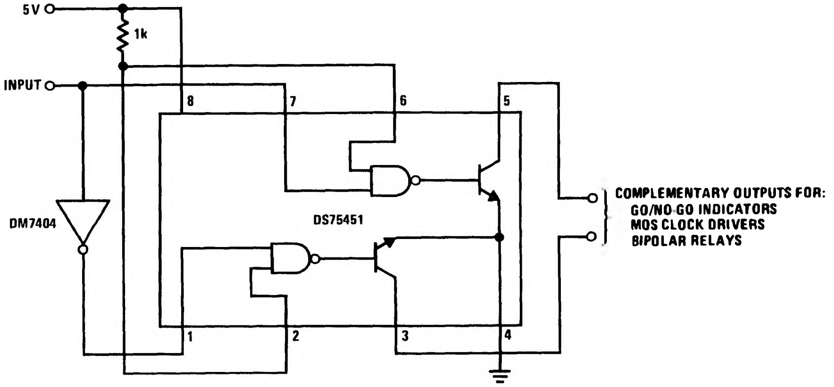
FIGURE 28. Dual Lamp or Relay Driver

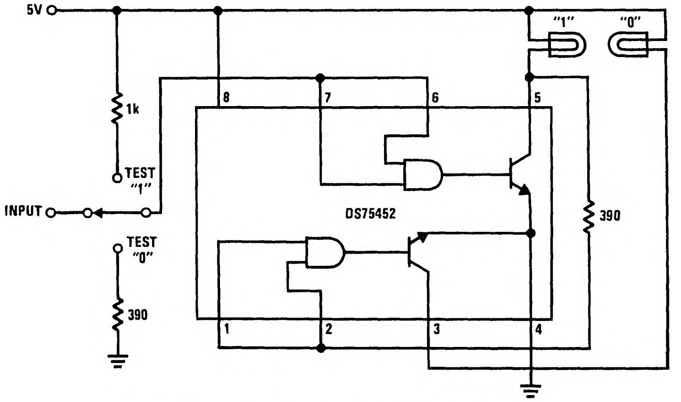


COMPLEMENTARY OUTPUTS FOR:
GO/NO-GO INDICATORS
MOS CLOCK DRIVERS
BIPOLAR RELAYS

TL/F/5824-47

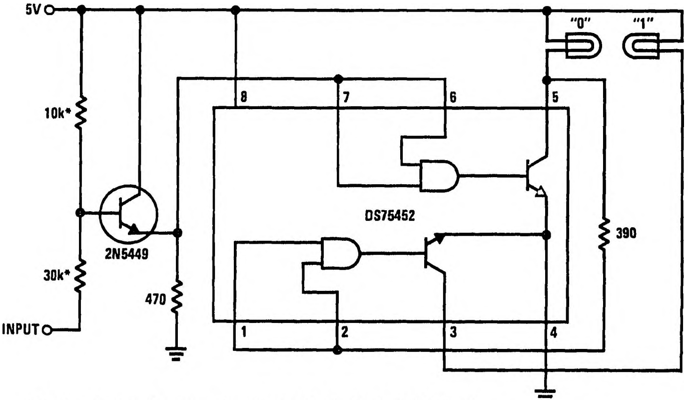
FIGURE 29. Complementary Driver

Typical Applications (Continued)



TL/F/5824-48

FIGURE 30. TTL or DTL Positive Logic-Level Detector



*The two input resistors must be adjusted for the level of MOS input.

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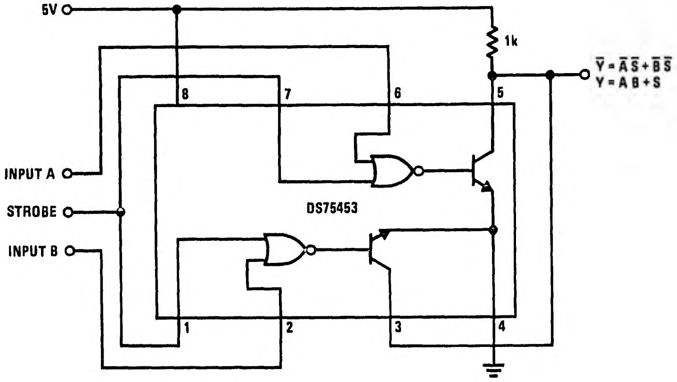
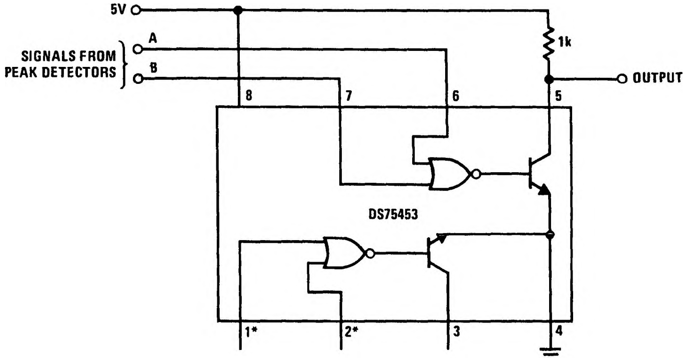
FIGURE 31. MOS Negative Logic-Level Detector



TL/F/5824-50

FIGURE 32. Logic Signal Comparator

Typical Applications (Continued)



*If inputs are unused, they should be connected to +5V through a 1k resistor.

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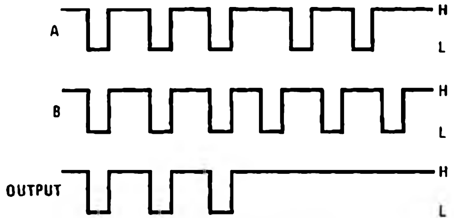
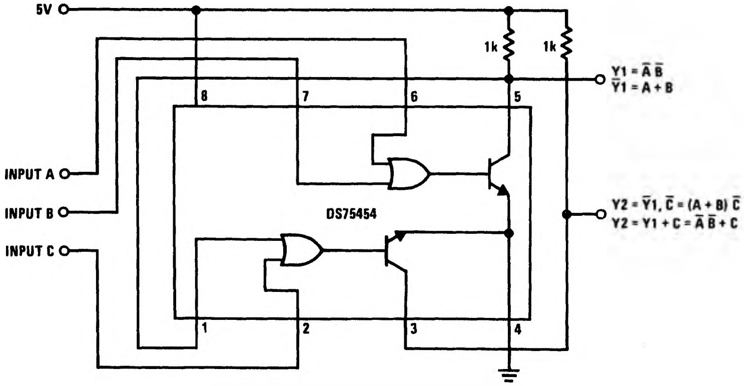


Low output occurs only when inputs are low simultaneously.

TL/F/5824-52

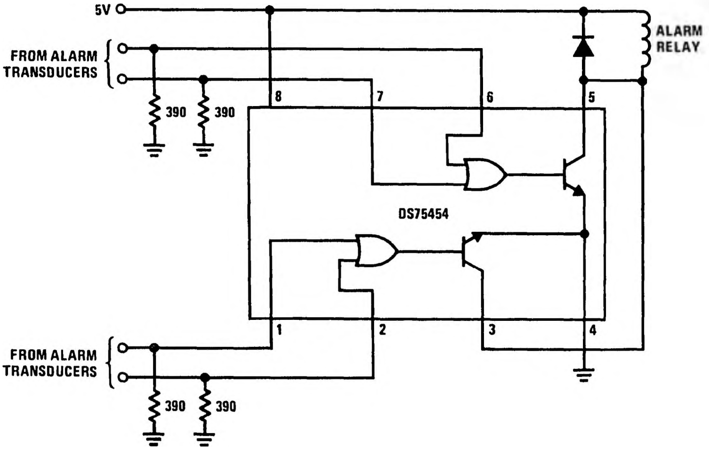
FIGURE 33. In-Phase Detector



TL/F/5824-53

FIGURE 34. Multifunction Logic-Signal Comparator

Typical Applications (Continued)



TL/F/5824-54

FIGURE 35. Alarm Detector