

## DS89C21 Differential CMOS Line Driver and Receiver Pair

Check for Samples: [DS89C21](#)

### FEATURES

- Meets TIA/EIA-422-A (RS-422) and CCITT V.11 Recommendation
- **LOW POWER** Design—15 mW Typical
- **Guaranteed AC Parameters:**
  - Maximum Driver Skew 2.0 ns
  - Maximum Receiver Skew 4.0 ns
- **Extended Temperature Range:** –40°C to +85°C
- Available in SOIC Packaging
- Operates over 20 Mbps
- Receiver OPEN Input Failsafe Feature

### DESCRIPTION

The DS89C21 is a differential CMOS line driver and receiver pair, designed to meet the requirements of TIA/EIA-422-A (RS-422) electrical characteristics interface standard. The DS89C21 provides one driver and one receiver in a minimum footprint. The device is offered in an 8-pin SOIC package.

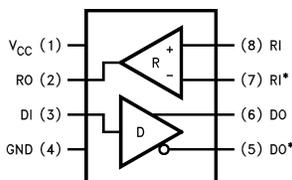
The CMOS design minimizes the supply current to 6 mA, making the device ideal for use in battery powered or power conscious applications.

The driver features a fast transition time specified at 2.2 ns, and a maximum differential skew of 2 ns making the driver ideal for use in high speed applications operating above 10 MHz.

The receiver can detect signals as low as 200 mV, and also incorporates hysteresis for noise rejection. Skew is specified at 4 ns maximum.

The DS89C21 is compatible with TTL and CMOS levels (DI and RO).

### Connection Diagram



See Package Number D (R-PDSO-G8)

### Truth Table Driver

Input	Outputs	
DI	DO	DO*
H	H	L
L	L	H

### Truth Table Receiver

Inputs	Output
RI–RI*	RO
$V_{DIFF} \geq +200$ mV	H
$V_{DIFF} \leq -200$ mV	L
OPEN <sup>(1)</sup>	H

(1) Non-terminated



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)(2)(3)</sup>

Supply Voltage ( $V_{CC}$ )	7V
Driver Input Voltage (DI)	-1.5V to $V_{CC} + 1.5V$
Driver Output Voltage (DO, DO <sup>*</sup> )	-0.5V to +7V
Receiver Input Voltage— $V_{CM}$ (RI, RI <sup>*</sup> )	±14V
Differential Receiver Input Voltage— $V_{DIFF}$ (RI, RI <sup>*</sup> )	±14V
Receiver Output Voltage (RO)	-0.5V to $V_{CC} + 0.5V$
Receiver Output Current (RO)	±25 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering 4 sec.)	+260°C
Maximum Junction Temperature	150°C
Maximum Package Power Dissipation @+25°C	
D Package	714 mW
Derate D Package	5.7 mW/°C above +25°C

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) ESD Rating: HBM (1.5 kΩ, 100 pF) all pins ≥ 2000V.EIAJ (0Ω, 200 pF) ≥ 250V

### Recommended Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.50	5.50	V
Operating Temperature ( $T_A$ )	-40	+85	°C
Input Rise or Fall Time (DI)		500	ns

### Electrical Characteristics <sup>(1)(2)</sup>

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
<b>DRIVER CHARACTERISTICS</b>							
$V_{IH}$	Input Voltage HIGH		DI	2.0		$V_{CC}$	V
$V_{IL}$	Input Voltage LOW			GND		0.8	V
$I_{IH}, I_{IL}$	Input Current	$V_{IN} = V_{CC}, GND, 2.0V, 0.8V$			0.05	±10	μA
$V_{CL}$	Input Clamp Voltage	$I_{IN} = -18 \text{ mA}$				-1.5	V

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
- (2) All typicals are given for  $V_{CC} = 5.0V$  and  $T_A = 25^\circ\text{C}$ .

**Electrical Characteristics <sup>(1)(2)</sup> (continued)**

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V <sub>OD1</sub>	Unloaded Output Voltage	No Load		DO, DO*		4.2	6.0	V
V <sub>OD2</sub>	Differential Output Voltage	R <sub>L</sub> = 100Ω			2.0	3.0		V
ΔV <sub>OD2</sub>	Change in Magnitude of V <sub>OD2</sub> for Complementary Output States					5.0	400	mV
V <sub>OD3</sub>	Differential Output Voltage	R <sub>L</sub> = 150Ω			2.1	3.1		V
V <sub>OD4</sub>	Differential Output Voltage	R <sub>L</sub> = 3.9 kΩ				4.0	6.0	V
V <sub>OC</sub>	Common Mode Voltage	R <sub>L</sub> = 100Ω				2.0	3.0	V
ΔV <sub>OC</sub>	Change in Magnitude of V <sub>OC</sub> for Complementary Output States					2.0	400	mV
I <sub>OSD</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0V			-30	-115	-150	mA
I <sub>OFF</sub>	Output Leakage Current	V <sub>CC</sub> = 0V	V <sub>OUT</sub> = +6V			0.03	+100	μA
			V <sub>OUT</sub> = -0.25V			-0.08	-100	μA
<b>RECEIVER CHARACTERISTICS</b>								
V <sub>TL</sub> , V <sub>TH</sub>	Differential Thresholds	V <sub>IN</sub> = +7V, 0V, -7V		RI, RI*	-200	±25	+200	mV
V <sub>HYS</sub>	Hysteresis	V <sub>CM</sub> = 0V			20	50		mV
R <sub>IN</sub>	Input Impedance	V <sub>IN</sub> = -7V, +7V, Other = 0V			5.0	9.5		kΩ
I <sub>IN</sub>	Input Current	Other Input = 0V, V <sub>CC</sub> = 5.5V and V <sub>CC</sub> = 0V	V <sub>IN</sub> = +10V		+1.0	+1.5		mA
			V <sub>IN</sub> = +3.0V		0	+0.22		mA
			V <sub>IN</sub> = +0.5V			-0.04		mA
			V <sub>IN</sub> = -3V		0	-0.41		mA
			V <sub>IN</sub> = -10V		-1.25	-2.5		mA
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -6 mA	V <sub>DIFF</sub> = +1V	RO	3.8	4.9		V
			V <sub>DIFF</sub> = OPEN		3.8	4.9		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = +6 mA, V <sub>DIFF</sub> = -1V			0.08	0.3	V	
I <sub>OSR</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0V			-25	-85	-150	mA
<b>DRIVER AND RECEIVER CHARACTERISTICS</b>								
I <sub>CC</sub>	Supply Current	No Load	DI = V <sub>CC</sub> or GND	V <sub>CC</sub>		3.0	6	mA
			DI = 2.4V or 0.5V			3.8	12	mA

**Switching Characteristics <sup>(1)(2)</sup>**

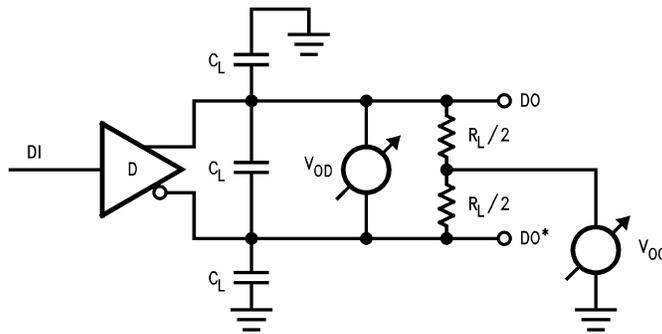
Over recommended supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
<b>DIFFERENTIAL DRIVER CHARACTERISTICS</b>							
t <sub>PLHD</sub>	Propagation Delay LOW to HIGH	R <sub>L</sub> = 100Ω	(Figure 2 Figure 3)	2	4.9	10	ns
t <sub>PHLD</sub>	Propagation Delay HIGH to LOW	C <sub>L</sub> = 50 pF		2	4.5	10	ns
t <sub>SKD</sub>	Skew,  t <sub>PLHD</sub> - t <sub>PHLD</sub>				0.4	2.0	ns
t <sub>TLH</sub>	Transition Time LOW to HIGH				2.2	9	ns
t <sub>THL</sub>	Transition Time HIGH to LOW				2.1	9	ns
<b>RECEIVER CHARACTERISTICS</b>							
t <sub>PLH</sub>	Propagation Delay LOW to HIGH	C <sub>L</sub> = 50 pF	(Figure 5 Figure 6)	6	18	30	ns
t <sub>PHL</sub>	Propagation Delay HIGH to LOW	V <sub>DIFF</sub> = 2.5V		6	17.5	30	ns
t <sub>SK</sub>	Skew,  t <sub>PLH</sub> - t <sub>PHL</sub>	V <sub>CM</sub> = 0V			0.5	4.0	ns
t <sub>r</sub>	Rise Time				2.5	9	ns
t <sub>f</sub>	Fall Time				2.1	9	ns

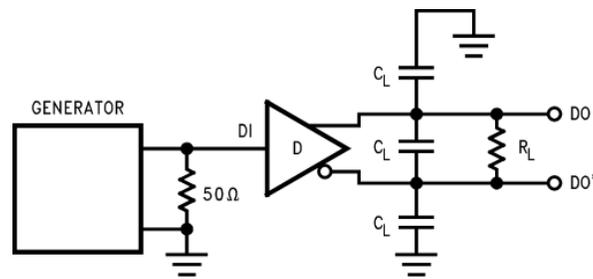
 (1) All typicals are given for V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C.

 (2) f = 1 MHz, t<sub>r</sub> and t<sub>f</sub> ≤ 6 ns.

**Parameter Measurement Information**

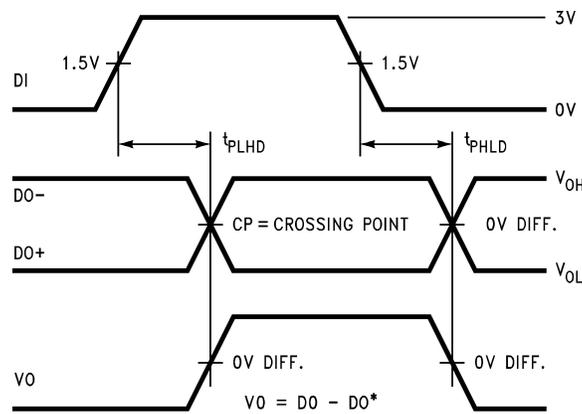


**Figure 1.  $V_{OD}$  and  $V_{OC}$  Test Circuit**

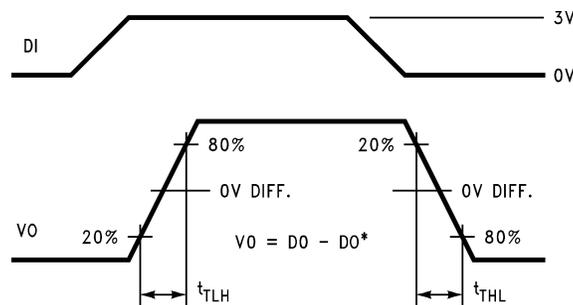


$f = 1 \text{ MHz}$ ,  $t_r$  and  $t_f \leq 6 \text{ ns}$ .

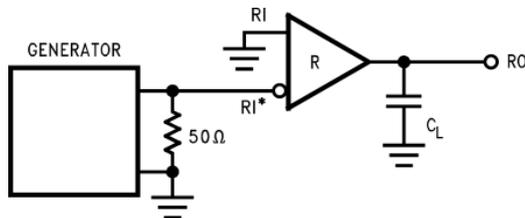
**Figure 2. Driver Propagation Delay Test Circuit**



**Figure 3. Driver Differential Propagation Delay Timing**

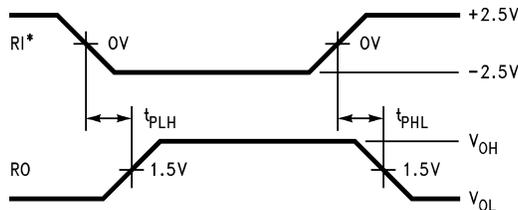


**Figure 4. Driver Differential Transition Timing**

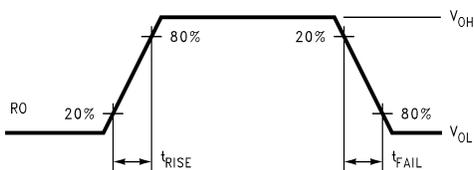


$f = 1 \text{ MHz}$ ,  $t_r$  and  $t_f \leq 6 \text{ ns}$ .

**Figure 5. Receiver Propagation Delay Test Circuit**



**Figure 6. Receiver Propagation Delay Timing**



**Figure 7. Receiver Rise and Fall Times**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS89C21TM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	DS89C 21TM	<a href="#">Samples</a>
DS89C21TM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS89C 21TM	<a href="#">Samples</a>
DS89C21TMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	DS89C 21TM	<a href="#">Samples</a>
DS89C21TMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS89C 21TM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

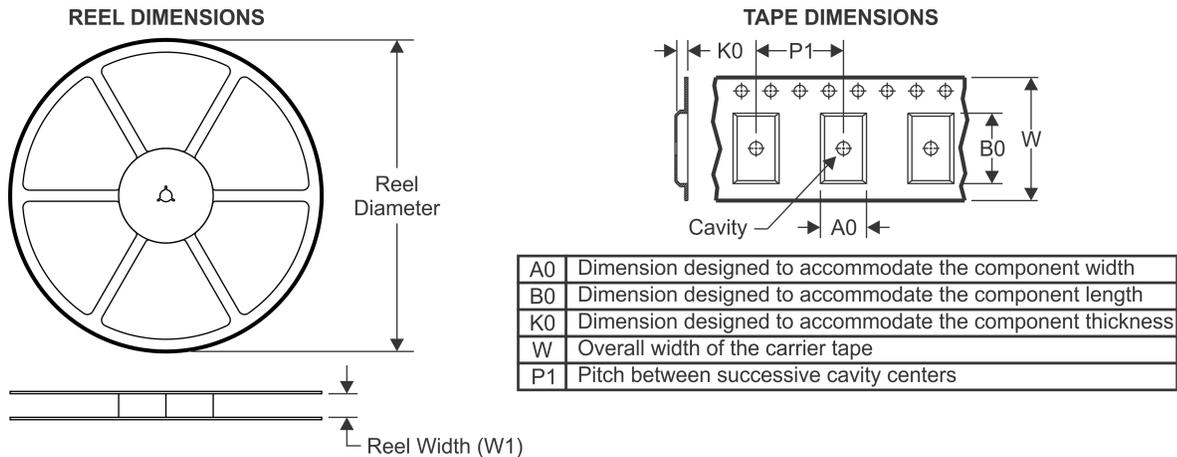
(4) Only one of markings shown within the brackets will appear on the physical device.

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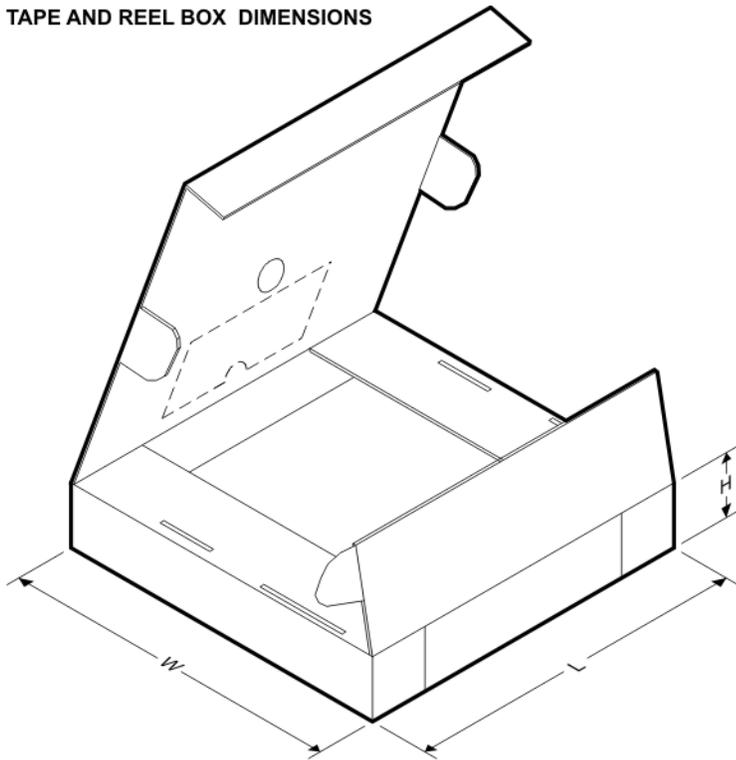
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS89C21TMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS89C21TMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

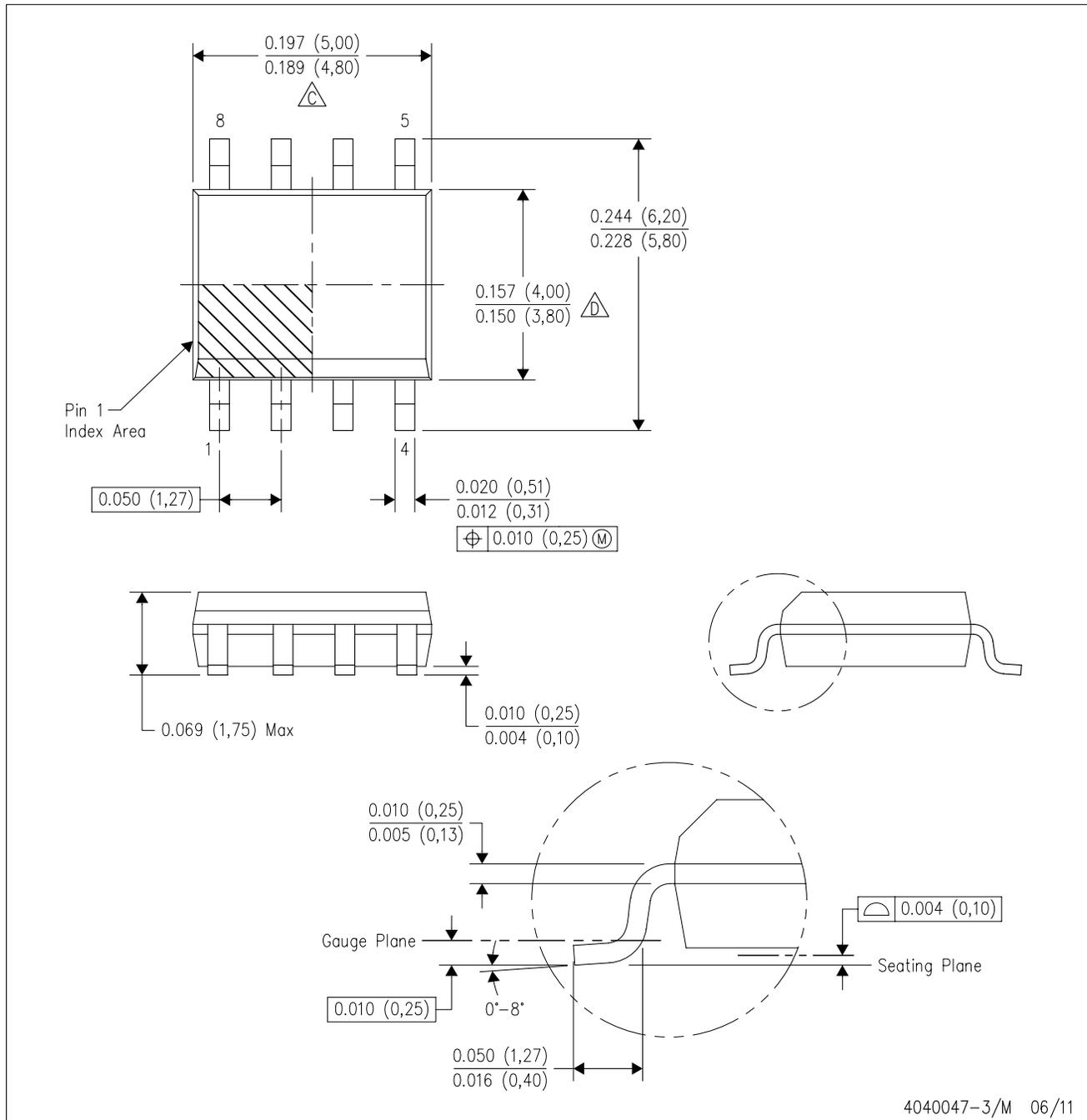


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS89C21TMX	SOIC	D	8	2500	349.0	337.0	45.0
DS89C21TMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

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