DS90LV001 800 Mbps LVDS Buffer

Check for Samples: DS90LV001

FEATURES

- **Single +3.3 V Supply**
- **LVDS receiver inputs accept LVPECL signals**
- **TRI-STATE outputs**
- **Receiver input threshold < ±100 mV**
- **Fast propagation delay of 1.4 ns (typ)**
- **Low jitter 800 Mbps fully differential data path**
- **100 ps (typ) of pk-pk jitter with PRBS = 2^{23}–1 data pattern at 800 Mbps**
- **Compatible with ANSI/TIA/EIA-644-A LVDS standard**
- **8 pin SOIC and space saving (70%) WSON package**
- **Industrial Temperature Range**

DESCRIPTION

The DS90LV001 LVDS-LVDS Buffer takes an LVDS input signal and provides an LVDS output signal. In many large systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS90LV001, available in the WSON package, will allow the receiver to be placed very close to the main transmission line, thus improving system performance.

A wide input dynamic range will allow the DS90LV001 to receive differential signals from LVPECL as well as LVDS sources. This will allow the device to also fill the role of an LVPECL-LVDS translator.

An output enable pin is provided, which allows the user to place the LVDS output in TRI-STATE.

The DS90LV001 is offered in two package options, an 8 pin WSON and SOIC.

Connection Diagram

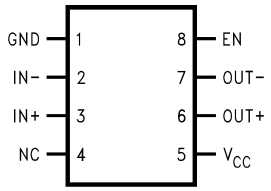
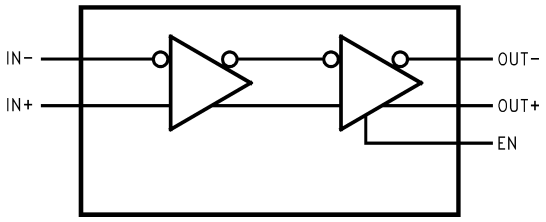


Figure 1. Top View
See Package Number D (R-PDSO-G8), NGK0008A

Block Diagram



Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage (EN)	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage (IN+, IN−)	−0.3V to +4V
LVDS Driver Output Voltage (OUT+, OUT−)	−0.3V to +4V
LVDS Output Short Circuit Current	Continuous
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
D Package	726 mW
Derate D Package	5.8 mW/°C above +25°C
NGK Package	2.44 W
Derate NGK Package	19.49 mW/°C above +25°C
ESD Ratings	
(HBM, 1.5kΩ, 100pF)	≥2.5kV
(EIAJ, 0Ω, 200pF)	≥250V

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Input Voltage	0		V_{CC}	V
Operating Free Air Temperature	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS (EN)							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V or 2.0V, V_{CC} = 3.6V			+7	+20	µA
I_{IL}	Low Level Input Current	V_{IN} = GND or 0.8V, V_{CC} = 3.6V			±1	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.6	−1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT)							
V_{OD}	Differential Output Voltage	R_L = 100Ω Figure 2 and Figure 3		250	325	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States					20	mV
V_{OS}	Offset Voltage	R_L = 100Ω Figure 2		1.080	1.19	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States					20	mV
I_{OZ}	Output TRI-STATE Current	EN = 0V, V_{OUT} = V_{CC} or GND			±1	±10	µA
I_{OFF}	Power-Off Leakage Current	V_{CC} = 0V, V_{OUT} = 3.6V or GND			±1	±10	µA
I_{OS}	Output Short Circuit Current (3)	EN = V_{CC}, V_{OUT+} and V_{OUT-} = 0V			−16	−24	mA
I_{OSD}	Differential Output Short Circuit Current (3)	EN = V_{CC}, V_{OD} = 0V			−7	−12	mA
LVDS RECEIVER DC SPECIFICATIONS (IN)							
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V, +1.2V or +3.25V			0	+100	mV
V_{TL}	Differential Input Low Threshold			−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100mV, V_{CC} = 3.3V		0.05		3.25	V
I_{IN}	Input Current	V_{IN} = +3.0V	V_{CC} = 3.6V or 0V		±1	±10	µA
		V_{IN} = 0V			±1	±10	µA
ΔI_{IN}	Change in Magnitude of I_{IN}	V_{IN} = +3.0V	V_{CC} = 3.6V or 0V		1	6	µA
		V_{IN} = 0V			1	6	µA
SUPPLY CURRENT							
I_{CCD}	Total Supply Current	EN = V_{CC}, R_L = 100Ω, C_L = 5 pF			47	70	mA
I_{CCZ}	TRI-STATE Supply Current	EN = 0V			22	35	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(2) All typical are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5pF Figure 4 and Figure 5	1.0	1.4	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	1.4	2.0	ns
t_{SKD1}	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$ (2) (3)			20	200	ps
t_{SKD3}	Part to Part Skew (2) (4)			0	60	ps
t_{SKD4}	Part to Part Skew (2) (5)				400	ps
t_{LHT}	Rise Time (2)	R_L = 100Ω, C_L = 5pF Figure 4 and Figure 6	200	320	450	ps
t_{HLT}	Fall Time (2)		200	310	450	ps
t_{PHZ}	Disable Time (Active High to Z)	R_L = 100Ω, C_L = 5pF Figure 7 and Figure 8		3	25	ns
t_{PLZ}	Disable Time (Active Low to Z)			3	25	ns
t_{PZH}	Enable Time (Z to Active High)			25	45	ns
t_{PZL}	Enable Time (Z to Active Low)			25	45	ns
t_{DJ}	LVDS Data Jitter, Deterministic (Peak-to-Peak) (6)	V_{ID} = 300mV; PRBS = 2^{23} − 1 data; V_{CM} = 1.2V at 800Mbps (NRZ)		100	135	ps
t_{RJ}	LVDS Clock Jitter, Random (6)	V_{ID} = 300mV; V_{CM} = 1.2V at 400MHz clock		2.2	3.5	ps

(1) All typical are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.
(2) The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over the PVT (process, voltage and temperature) range.
(3) t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(4) t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(5) t_{SKD4}, Part to Part Skew, is the differential channel-to- channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(6) The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over the PVT range with the following test equipment setup: HP8133A (pattern pulse generator), 5 feet of RG142B cable with DUT test board and HP83480A (digital scope mainframe) with HP83484A (50GHz scope module). The HP8133A with RG142B cable exhibit a t_{DJ} = 21ps and t_{RJ} = 1.8ps.

DC TEST CIRCUITS

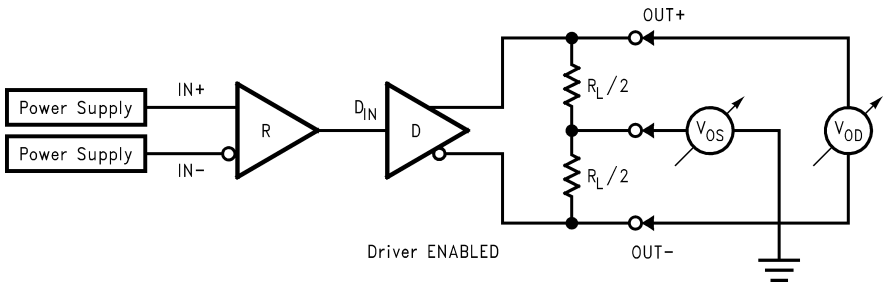


Figure 2. Differential Driver DC Test Circuit

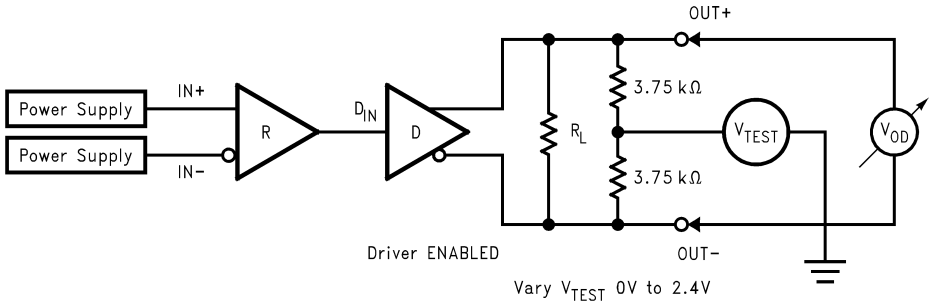


Figure 3. Differential Driver Full Load DC Test Circuit

AC TEST CIRCUITS AND TIMING DIAGRAMS

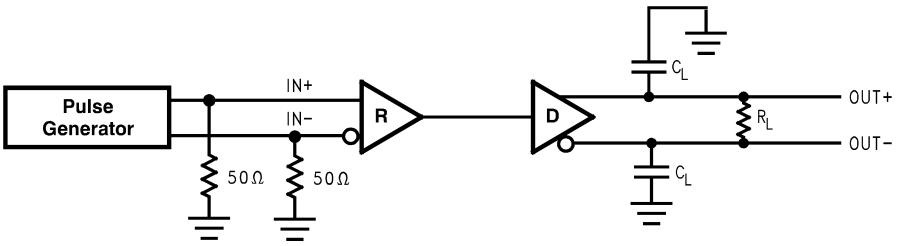


Figure 4. LVDS Output Load

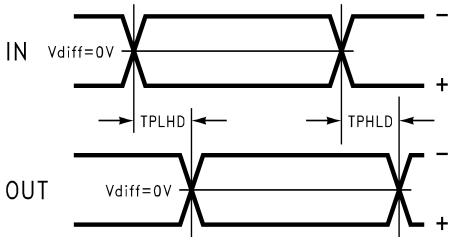


Figure 5. Propagation Delay Low-to-High and High-to-Low

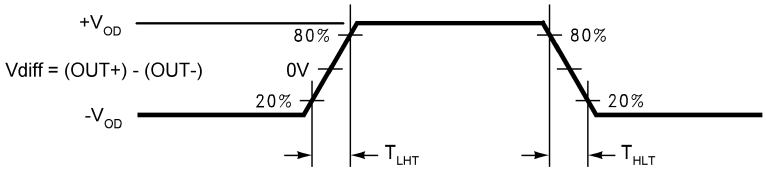


Figure 6. LVDS Output Transition Time

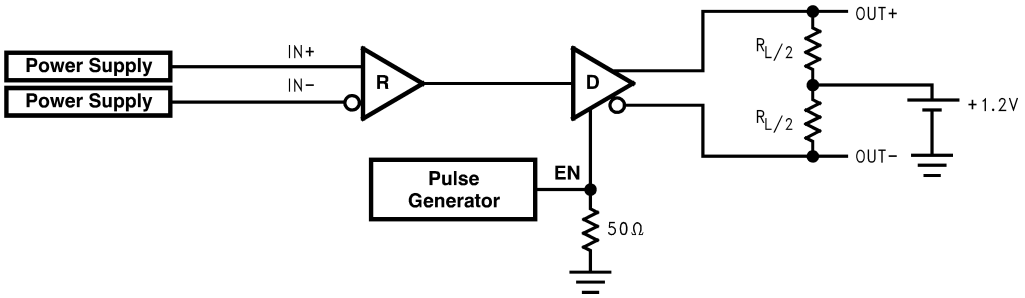


Figure 7. TRI-STATE Delay Test Circuit

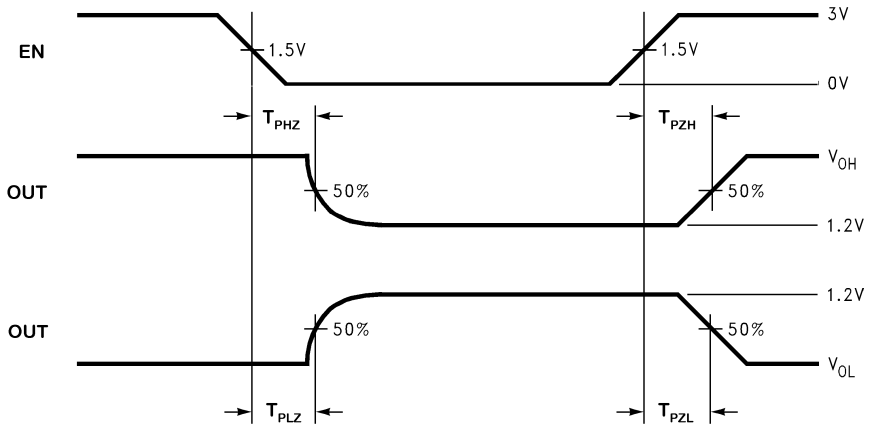


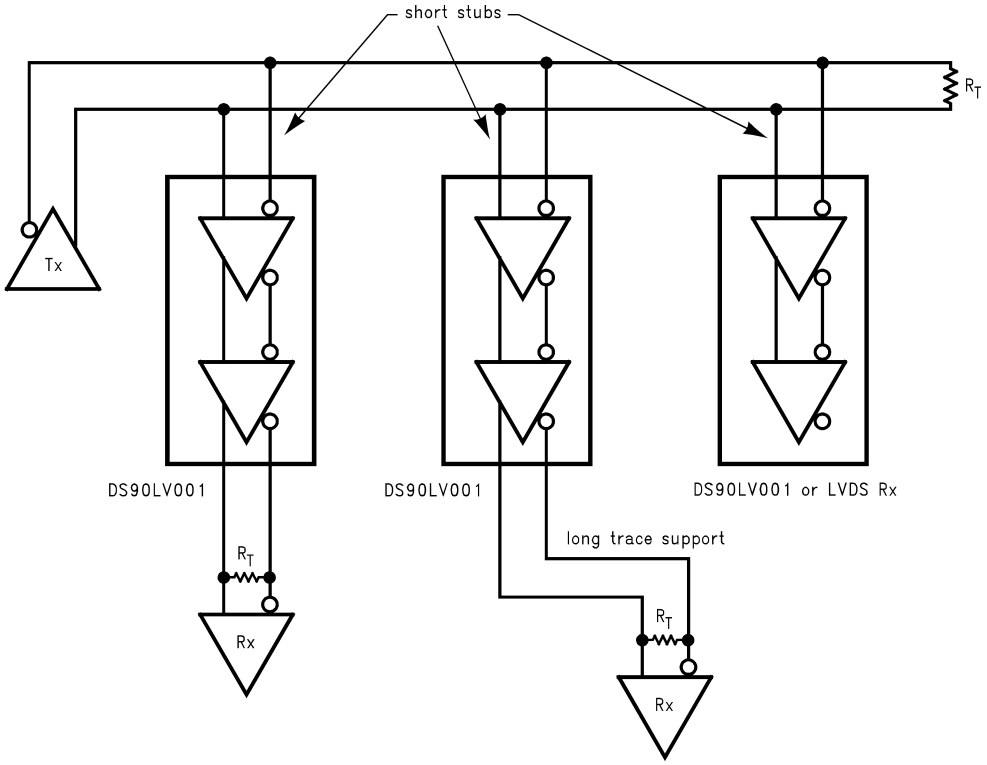
Figure 8. Output active to TRI-STATE and TRI-STATE to active output time

DS90LV001 Pin Descriptions (SOIC and WSON)

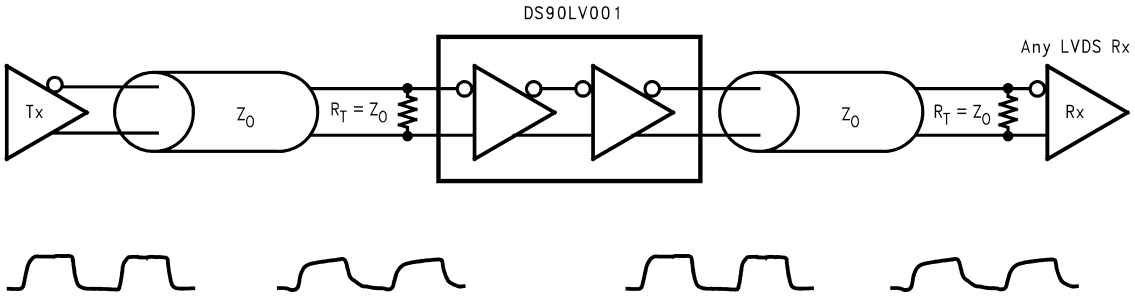
Pin Name	Pin #	Input/Output	Description
GND	1	P	Ground
IN −	2	I	Inverting receiver LVDS input pin
IN+	3	I	Non-inverting receiver LVDS input pin
NC	4		No Connect
V_{CC}	5	P	Power Supply, 3.3V ± 0.3V.
OUT+	6	O	Non-inverting driver LVDS output pin
OUT -	7	O	Inverting driver LVDS output pin
EN	8	I	Enable pin. When EN is LOW, the driver is disabled and the LVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL levels.
DAP	NA	NA	Die Attach Pad or DAP (WSON Package only). The DAP is NOT connected to the device GND nor any other pin. It is still recommended to connect the DAP to a GND plane of a PCB for enhenced heat dissipation.

TYPICAL APPLICATIONS

Backplane Stub-Hider Application



Cable Repeater Application



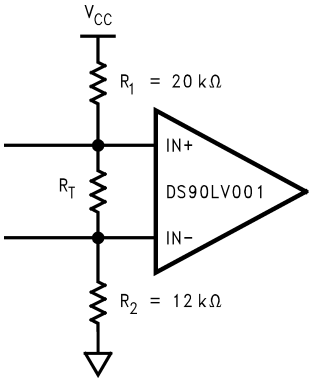
APPLICATION INFORMATION

MODE OF OPERATION

The DS90LV001 can be used as a "stub-hider." In many systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on the individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns and PCB designs often make it difficult to make the stubs as short as the designer would like. The DS90LV001, available in the WSON package, can improve system performance by allowing the receiver to be placed very close to the main transmission line either on the backplane itself or very close to the connector on the card. Longer traces to the LVDS receiver may be placed after the DS90LV001. This very small WSON package is a 75% space savings over the SOIC package.

INPUT FAILSAFE

The receiver inputs of the DS90LV001 do not have internal failsafe biasing. For point-to-point and multidrop applications with a single source, failsafe biasing may not be required. When the driver is off, the link is in-active. If failsafe biasing is required, this can be accomplished with external high value resistors. Using the equations in the LVDS Owner"s Manual Chapter 4, the IN+ should be pull to V_{CC} (3.3V) with 20kΩ and the IN− should be pull to GND with 12kΩ. This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion.



PCB LAYOUT AND POWER SYSTEM BYPASS

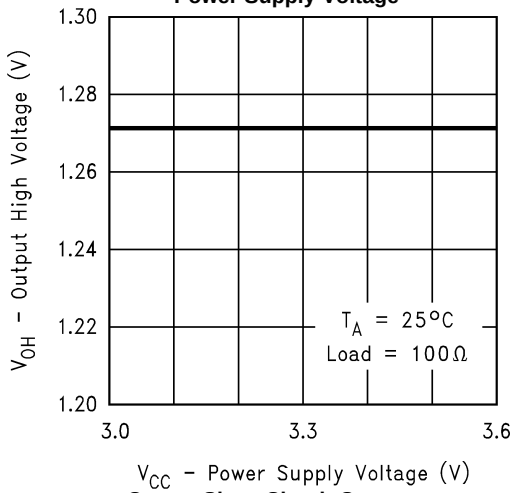
Circuit board layout and stack-up for the DS90LV001 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the DS90LV001 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

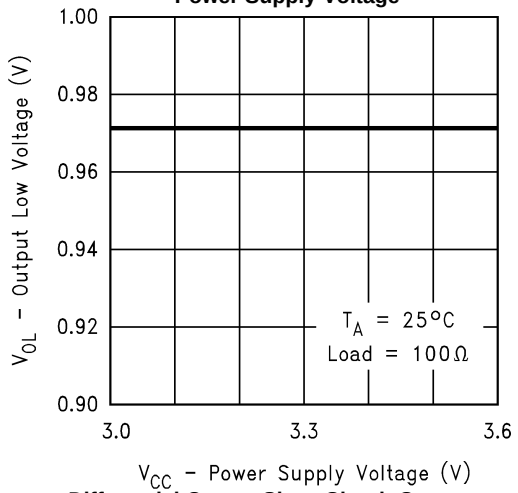
There are more common practices which should be followed when designing PCBs for LVDS signaling. Please see application note AN-1108 for guidelines. In addition, application note AN-1187 has additional information specifically related to WSON recommendations.

TYPICAL PERFORMANCE CURVES

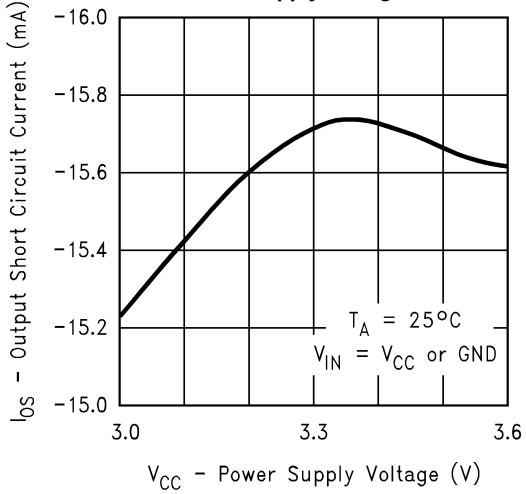
Output High Voltage vs Power Supply Voltage



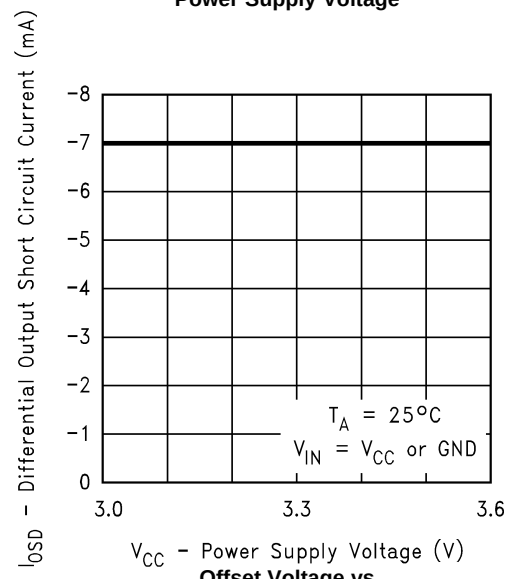
Output Low Voltage vs Power Supply Voltage



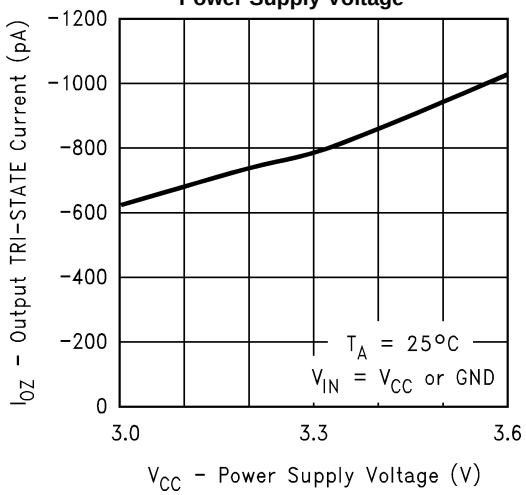
Output Short Circuit Current vs Power Supply Voltage



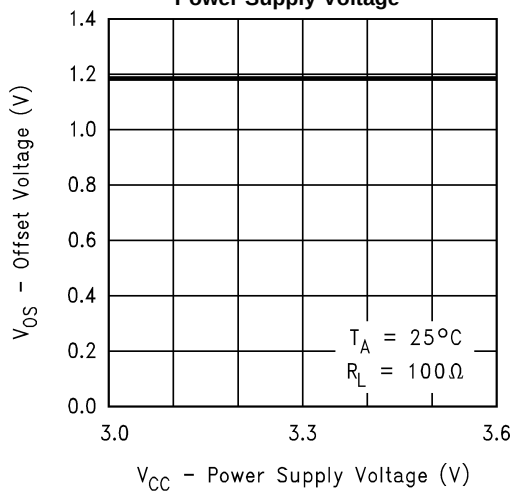
Differential Output Short Circuit Current vs Power Supply Voltage



Output TRI-STATE Current vs Power Supply Voltage

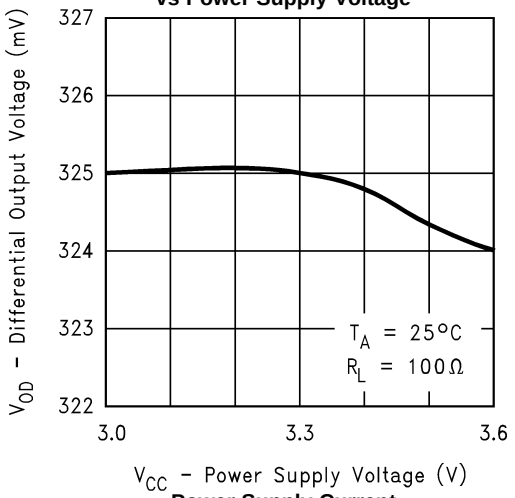


Offset Voltage vs Power Supply Voltage

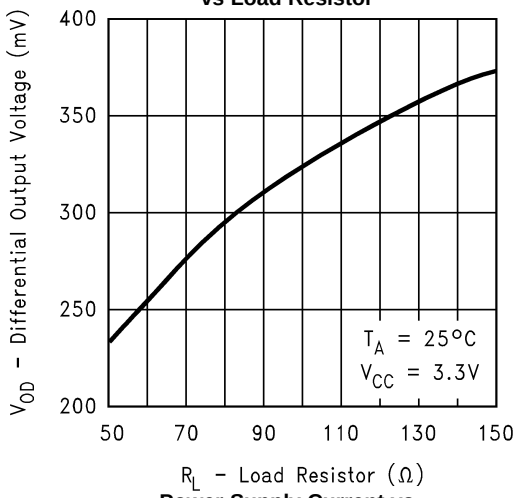


TYPICAL PERFORMANCE CURVES (continued)

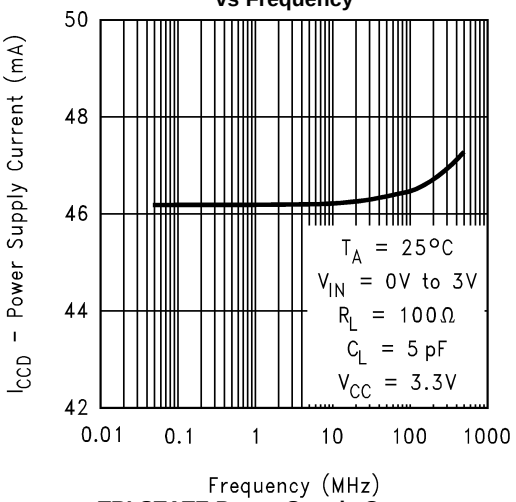
Differential Output Voltage vs Power Supply Voltage



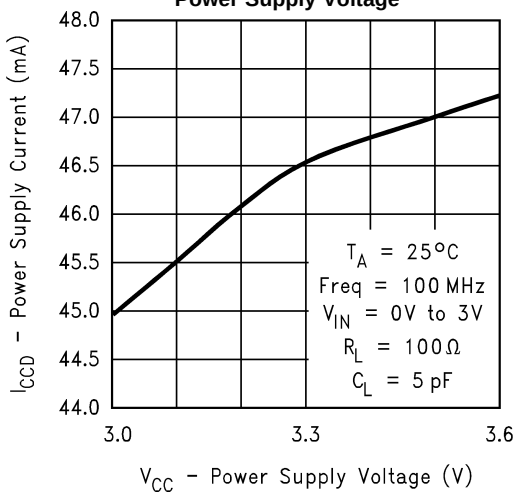
Differential Output Voltage vs Load Resistor



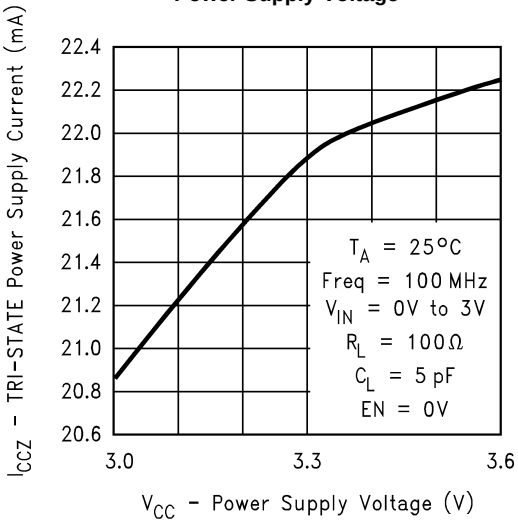
Power Supply Current vs Frequency



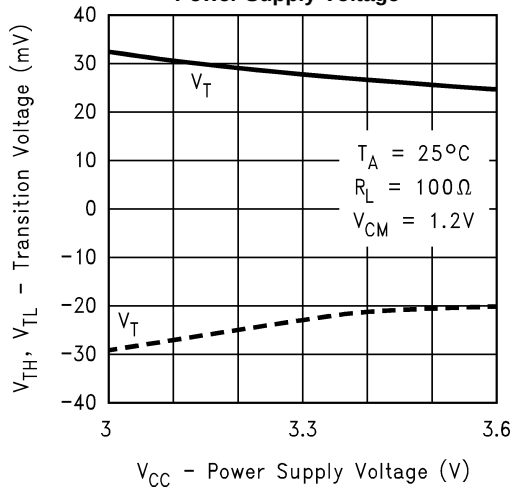
Power Supply Current vs Power Supply Voltage



TRI-STATE Power Supply Current vs Power Supply Voltage

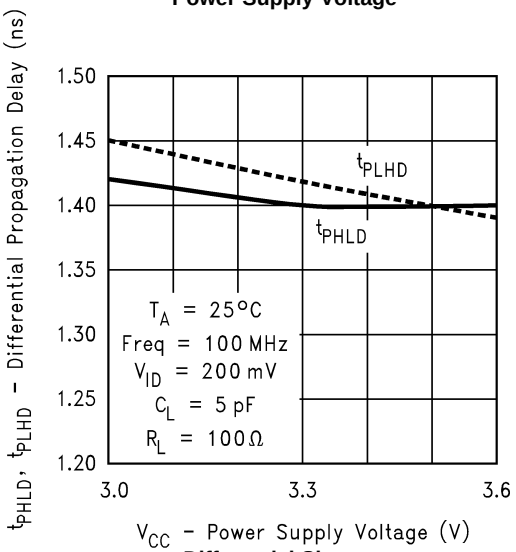


Differential Transition Voltage vs Power Supply Voltage

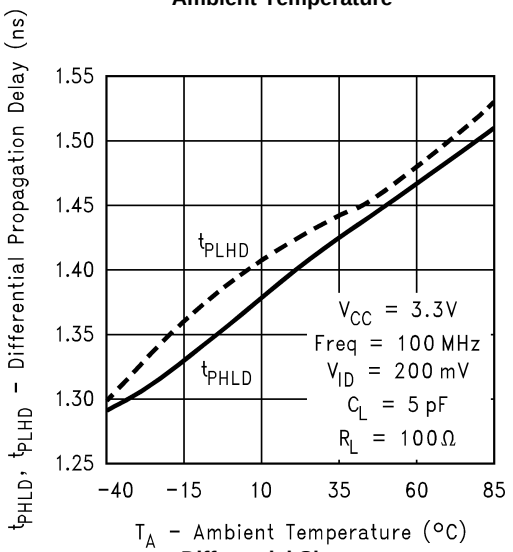


TYPICAL PERFORMANCE CURVES (continued)

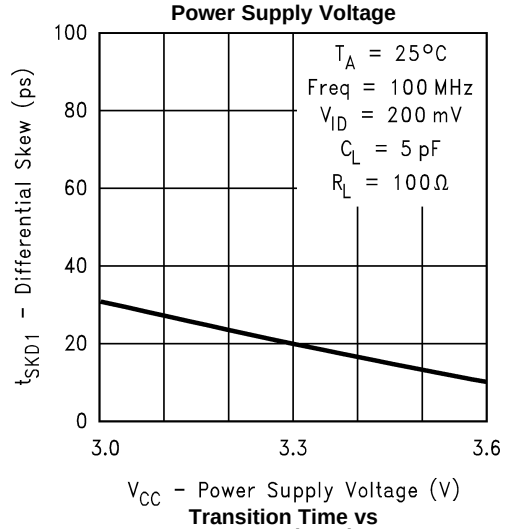
Differential Propagation Delay vs Power Supply Voltage



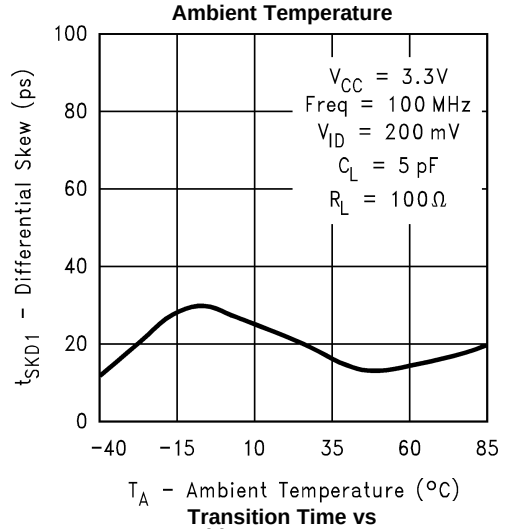
Differential Propagation Delay vs Ambient Temperature



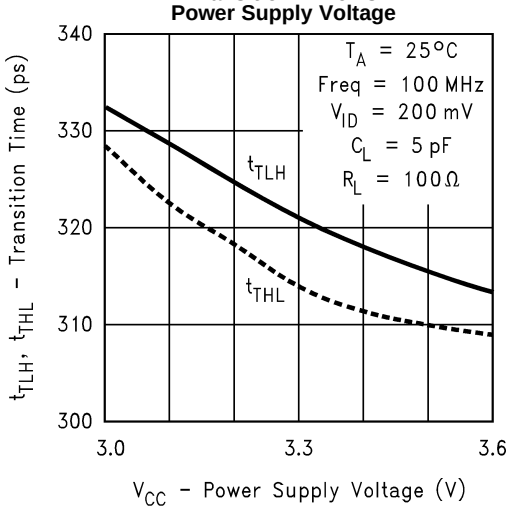
Differential Skew vs Power Supply Voltage



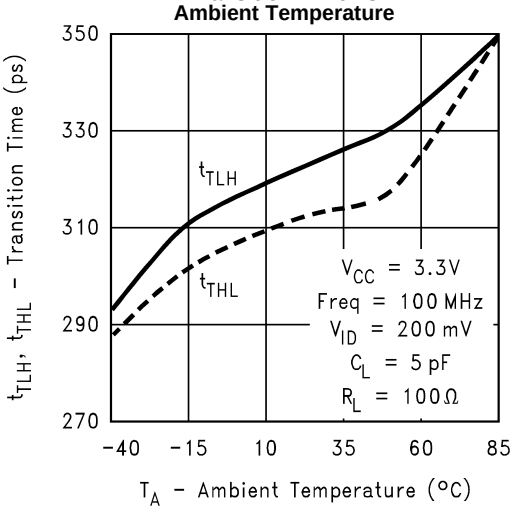
Differential Skew vs Ambient Temperature



Transition Time vs Power Supply Voltage

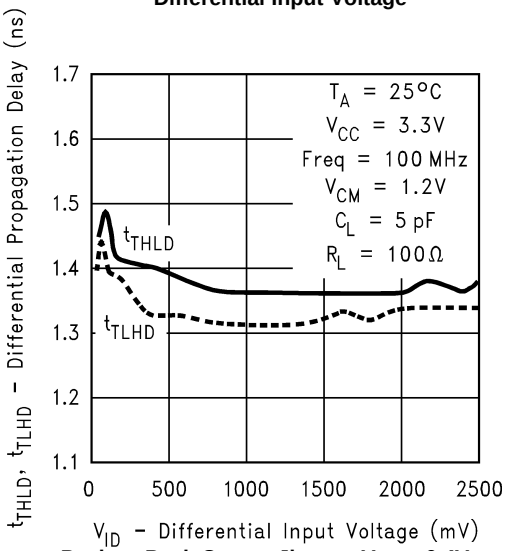


Transition Time vs Ambient Temperature

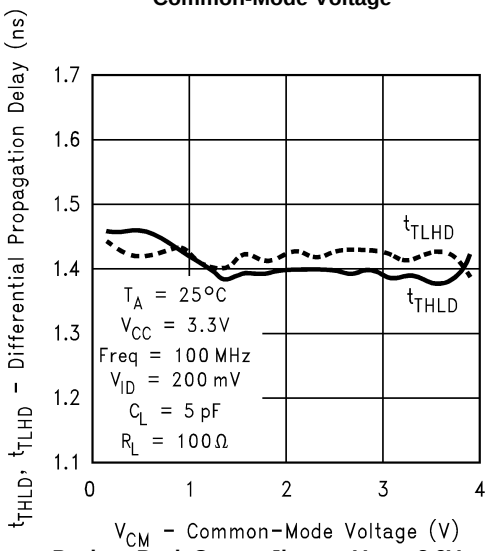


TYPICAL PERFORMANCE CURVES (continued)

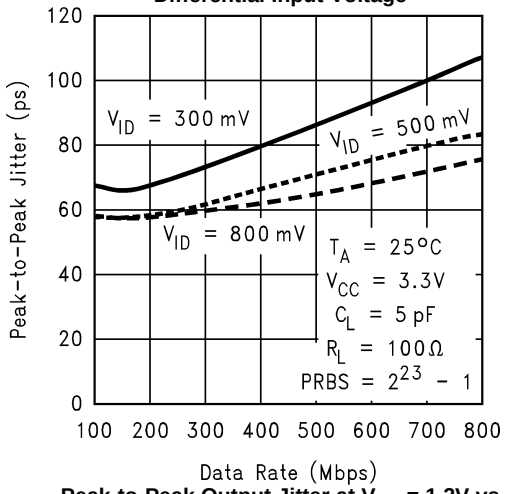
Differential Propagation Delay vs Differential Input Voltage



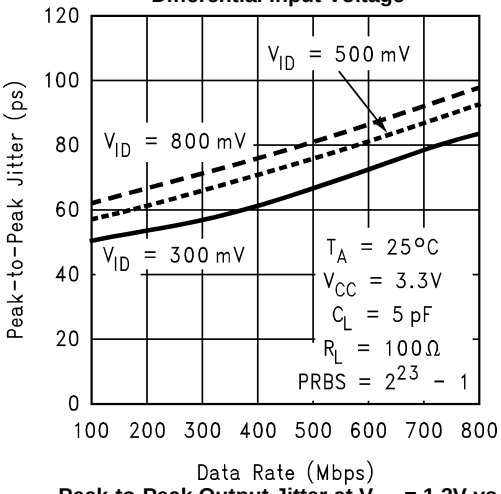
Differential Propagation Delay vs Common-Mode Voltage



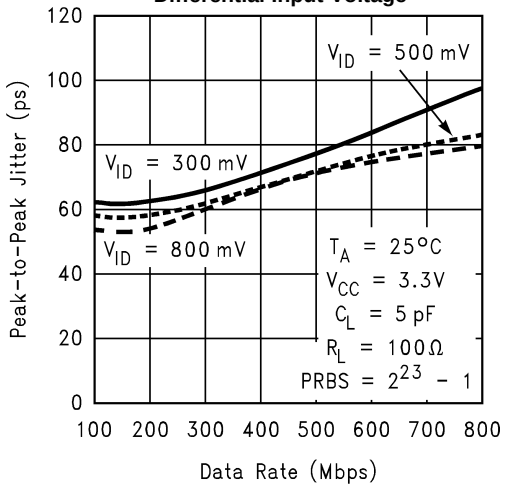
Peak-to-Peak Output Jitter at V_{CM} = 0.4V vs Differential Input Voltage



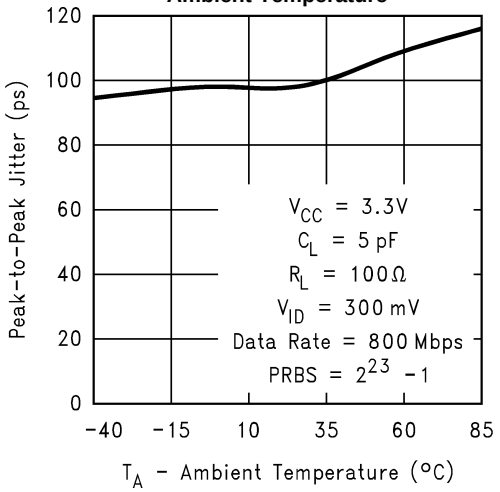
Peak-to-Peak Output Jitter at V_{CM} = 2.9V vs Differential Input Voltage



Peak-to-Peak Output Jitter at V_{CM} = 1.2V vs Differential Input Voltage



Peak-to-Peak Output Jitter at V_{CM} = 1.2V vs Ambient Temperature



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90LV001TLD	ACTIVE	WSON	NGK	8	1000	TBD	Call TI	Call TI	-40 to 85	001	Samples
DS90LV001TLD/NOPB	ACTIVE	WSON	NGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	001	Samples
DS90LV001TLDX	ACTIVE	WSON	NGK	8	4500	TBD	Call TI	Call TI	-40 to 85	001	Samples
DS90LV001TLDX/NOPB	ACTIVE	WSON	NGK	8	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	001	Samples
DS90LV001TM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LV001 TM	Samples
DS90LV001TM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LV001 TM	Samples
DS90LV001TMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LV001 TM	Samples
DS90LV001TMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LV001 TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

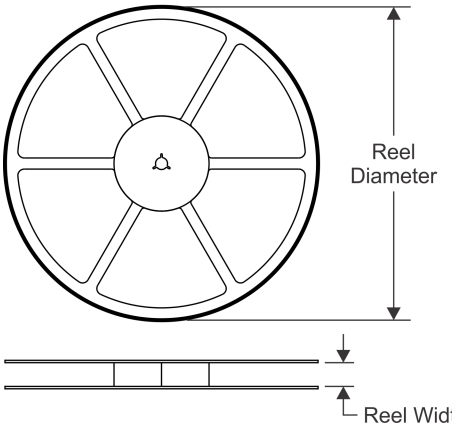
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

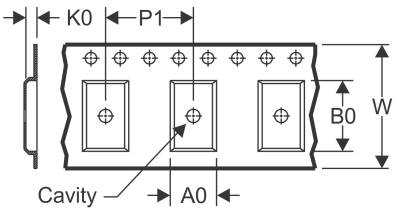
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

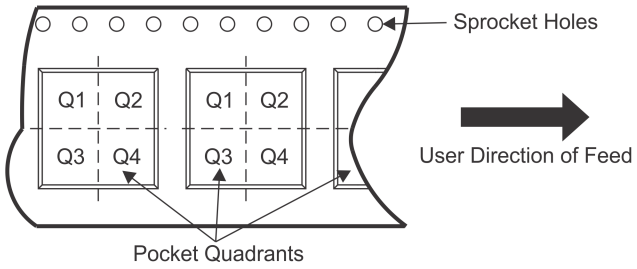


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

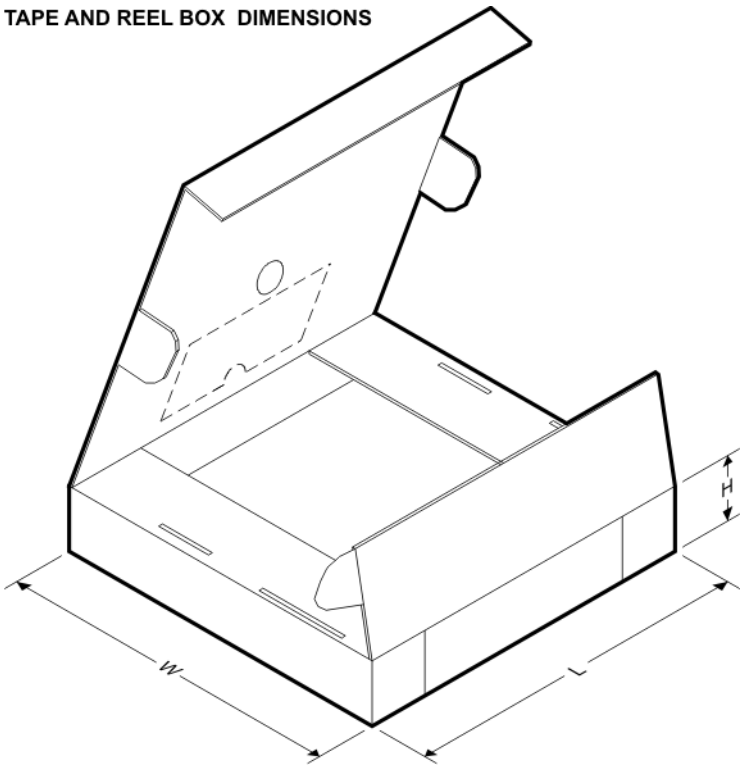
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV001TLD	WSON	NGK	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS90LV001TLD/NOPB	WSON	NGK	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS90LV001TLDX	WSON	NGK	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS90LV001TLDX/NOPB	WSON	NGK	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS90LV001TMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS90LV001TMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

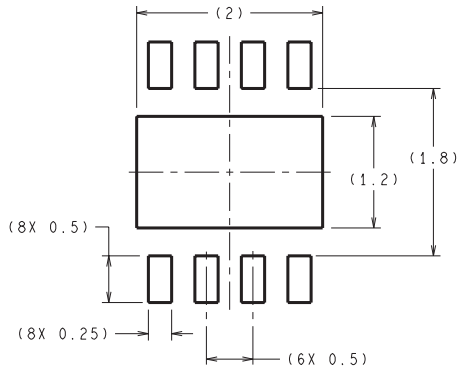
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

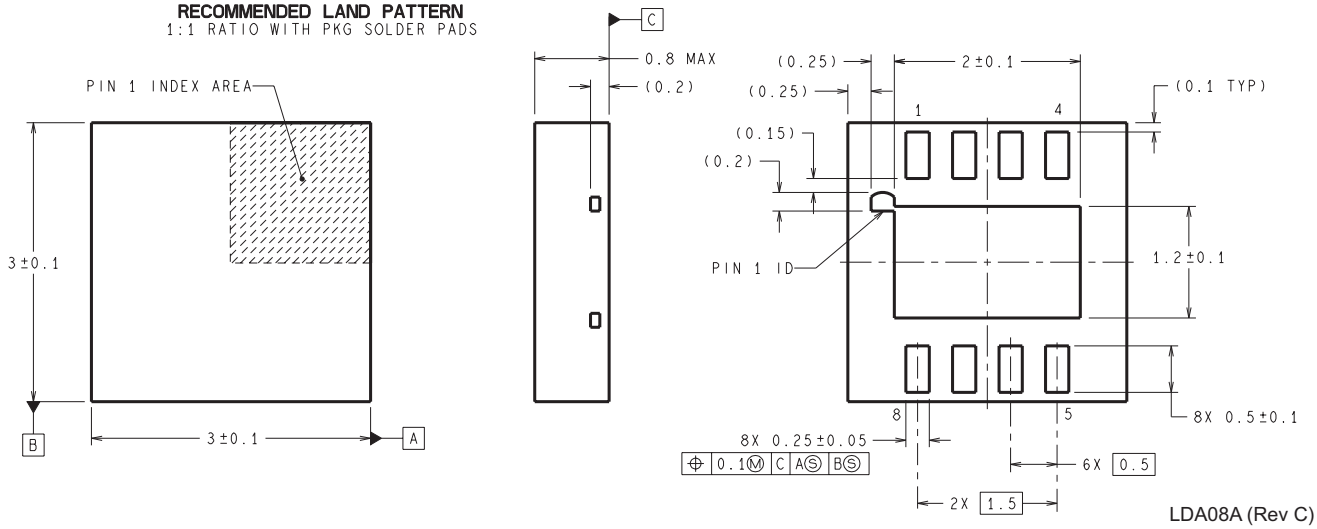
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV001TLD	WSON	NGK	8	1000	210.0	185.0	35.0
DS90LV001TLD/NOPB	WSON	NGK	8	1000	213.0	191.0	55.0
DS90LV001TLDX	WSON	NGK	8	4500	349.0	337.0	45.0
DS90LV001TLDX/NOPB	WSON	NGK	8	4500	367.0	367.0	35.0
DS90LV001TMX	SOIC	D	8	2500	349.0	337.0	45.0
DS90LV001TMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

NGK0008A



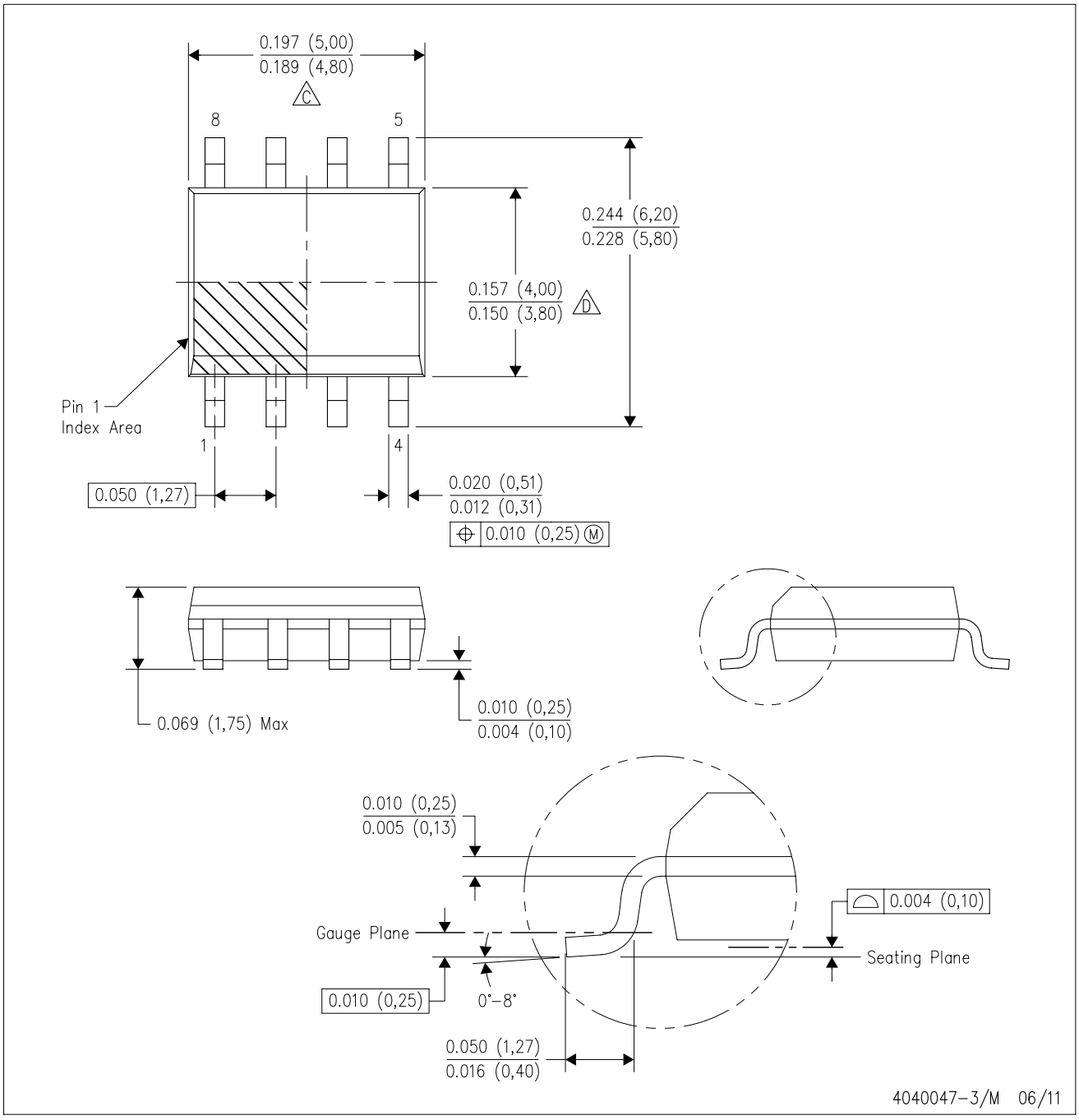
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



LDA08A (Rev C)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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