DS90UB927Q 5MHz - 85MHz 24-bit Color FPD-Link III Serializer with Bidirectional Control Channel

Check for Samples: DS90UB927-Q1, DS90UB927Q, DS90UB927Q-Q1

FEATURES

- **Bidirectional control channel interface with I2C compatible serial control bus**
- **Low EMI FPD-Link video input**
- **Supports high definition (720p) digital video format**
- **5MHz – 85MHz PCLK supported**
- **RGB888 + VS, HS, DE and I2S audio supported**
- **Up to 4 I2S Digital Audio inputs for surround sound applications**
- **4 Bidirectional GPIO channels with 2 dedicated pins**
- **Single 3.3V supply with 1.8V or 3.3V compatible LVCMOS I/O interface**
- **AC-coupled STP Interconnect up to 10 meters**
- **DC-balanced & scrambled Data with Embedded Clock**
- **Supports repeater application**
- **Internal pattern generation**
- **Low power modes minimize power dissipation**
- **Automotive grade product: AEC-Q100 Grade 2 qualified**
- **>8kV HBM and ISO 10605 ESD rating**
- **Backward compatible modes**

APPLICATIONS

- **Automotive Display for Navigation**
- **Rear Seat Entertainment Systems**
- **Automotive Driver Assistance**
- **Automotive Megapixel Camera Systems**

DESCRIPTION

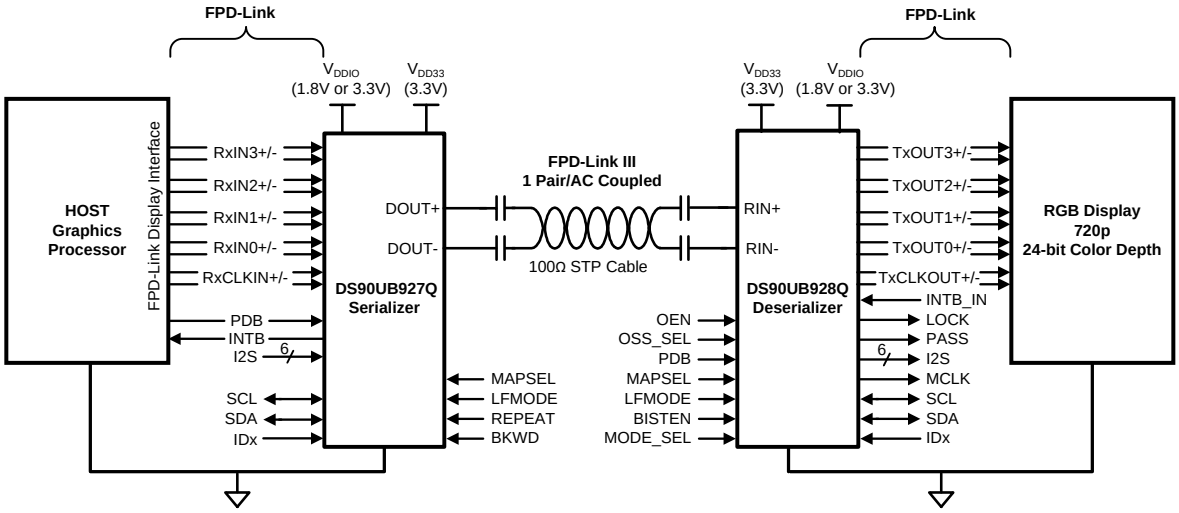
The DS90UB927Q serializer, in conjunction with a DS90UB928Q or DS90UB926Q deserializer, provides a complete digital interface for concurrent transmission of high-speed video, audio, and control data for automotive display and image sensing applications.

The chipset is ideally suited for automotive video display systens with HD formats and automotive vision systems with megapixel resolutions. The DS90UB927Q incorporates an embedded bidirectional control channel and low latency GPIO controls. This device translates a FPD-Link video interface into a single-pair high-speed serialized interface. The FPD-Link III serial bus scheme supports full duplex, high speed forward channel data transmission and low-speed back channel communication over a single differential link. Consolidation of audio, video, and control data over a single differential pair reduces the interconnect size and weight, while also eliminating skew issues and simplifying system design.

The DS90UB927Q serializer embeds the clock and level shifts the signals to high-speed differential signaling. Up to 24 RGB data bits are serialized along with three video control signals, and up to four I2S data inputs.

The FPD-Link data interface allows for easy interfacing with data sources while also minimizing EMI and bus width. EMI on the high-speed FPD-Link III bus is minimized using low voltage differential signaling, data scrambling and randomization, and dc-balancing.

Applications Diagram



Megapixel Camera Application Diagram

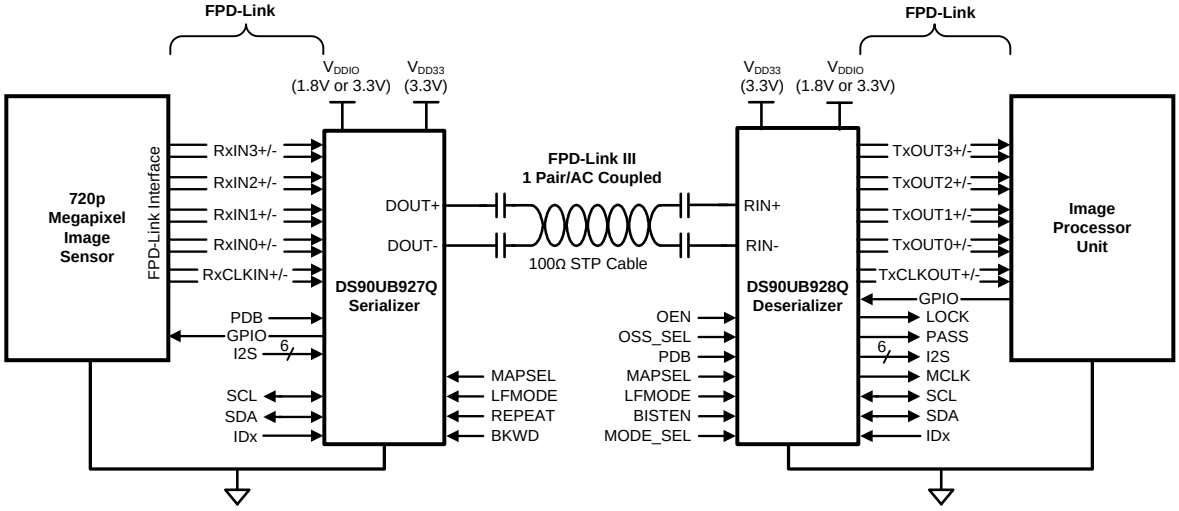


Figure 1. Megapixel Camera Application Diagram

DS90UB927Q Pin Diagram

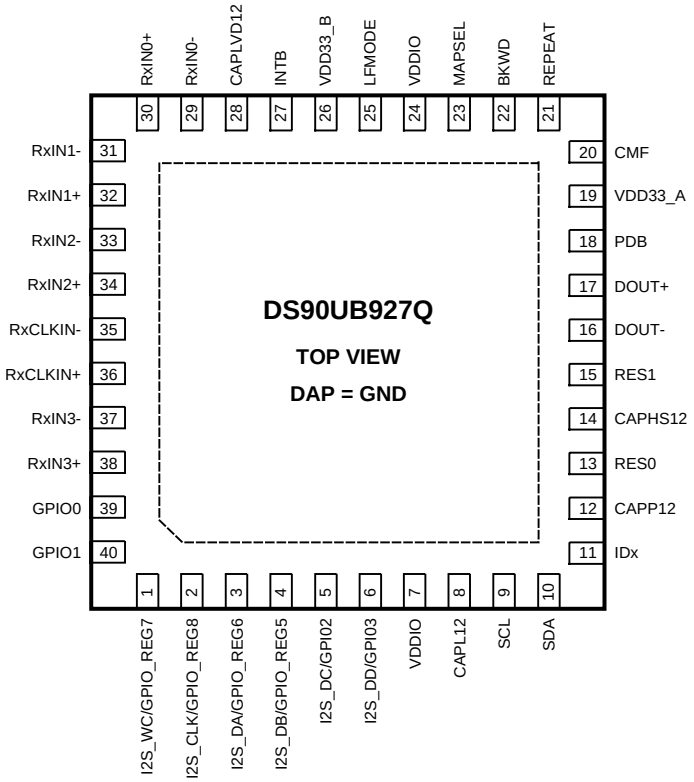


Figure 2. DS90UB927Q — Top View

Pin Descriptions

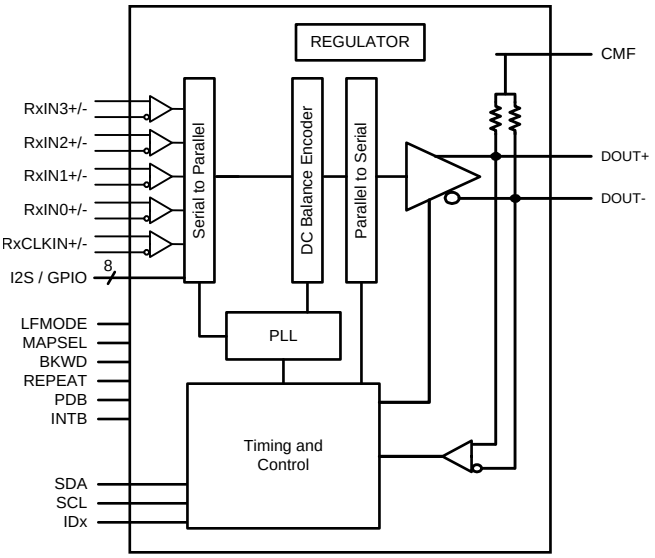
Pin Name	Pin #	I/O, Type	Description
FPD-Link Input Interface			
RxIN[3:0]+	38, 34, 32, 30	I, LVDS	True LVDS Data Inputs Each pair requires external 100Ω differential termination for standard LVDS levels
RxIN[3:0]-	37, 33, 31, 29	I, LVDS	Inverting LVDS Data Inputs Each pair requires external 100Ω differential termination for standard LVDS levels
RxCLKIN+	36	I, LVDS	True LVDS Clock Input The pair requires external 100Ω differential termination for standard LVDS levels
RxCLKIN-	35	I, LVDS	Inverting LVDS Clock Input The pair requires external 100Ω differential termination for standard LVDS levels
LVCMOS Parallel Interface			
I2S_WC I2S_CLK	1 2	I, LVCMOS w/ pull down	Digital Audio Interface I2S Word Clock and I2S Bit Clock Inputs Shared with GPIO_REG7 and GPIO_REG8 Table 3
I2S_DA I2S_DB I2S_DC I2S_DD	3 4 5 6	I, LVCMOS w/ pull down	Digital Audio Interface I2S Data Inputs Shared with GPIO_REG6, GPIO_REG5, GPIO2, GPIO3
GPIO[1:0]	40, 39	I/O, LVCMOS w/ pull down	General Purpose I/O See Table 1
REPEAT	21	I, LVCMOS w/ pull down	Repeater Mode Select REPEAT = 0, Repeater Mode disabled (Default) REPEAT = 1, Repeater Mode enabled Requires a 10kΩ pull-up if set HIGH

Pin Name	Pin #	I/O, Type	Description
BKWD	22	I, LVCMOS w/ pull down	Backward Compatible Mode Select BKWD = 0, interfacing to DS90UH926/8Q (Default) BKWD = 1, interfacing to DS90UR906/8Q, DS90UR916Q Requires a 10kΩ pull-up if set HIGH
MAPSEL	23	I, LVCMOS w/ pull down	FPD-Link Input Map Select MAPSEL = 0, LSBs on RxIN3± (Default) MAPSEL = 1, MSBs on RxIN3± See Figure 14and Figure 15 Requires a 10kΩ pull-up if set HIGH
LFMODE	25	I, LVCMOS w/ pull down	Low Frequency Mode Select LFMODE = 0, 15MHz ≤ RxCLKIN ≤ 85MHz (Default) LFMODE = 1, 5MHz ≤ RxCLKIN < 15MHz Requires a 10kΩ pull-up if set HIGH
Optional Parallel Interface			
GPIO[3:2]	6, 5	I/O, LVCMOS w/ pull down	General Purpose I/O Shared with I2S_DD and I2S_DC See Table 1
GPIO_REG[8:5]	2, 1, 3, 4	I/O, LVCMOS w/ pull down	Register-Only General Purpose I/O Shared with I2S_CLK, I2S_WC, I2S_DA, I2S_DB See Table 2
Control and Configuration			
PDB	18	I, LVCMOS w/ pull-down	Power-down Mode Input Pin Must be driven or pulled up to V_{DD33}. Refer to “Power Up Requirements and PDB Pin" in the Applications Information Section. PDB = H, device is enabled (normal operation) PDB = L, device is powered down. When the device is in the powered down state, the Driver Outputs are both HIGH, the PLL is shutdown, and I_{DD} is minimized. Control Registers are **RESET**.
SCL	9	I/O, LVCMOS Open Drain	I2C Clock Input / Output Interface Must have an external pull-up to V_{DD33}. **DO NOT FLOAT.** Recommended pull-up: 4.7kΩ.
SDA	10	I/O, LVCMOS Open Drain	I2C Data Input / Output Interface Must have an external pull-up to V_{DD33}. **DO NOT FLOAT.** Recommended pull-up: 4.7kΩ.
IDx	11	I, Analog	I2C Address Select External pull-up to V_{DD33} is required under all conditions. **DO NOT FLOAT.** Connect to external pull-up to V_{DD33} and pull-down to GND to create a voltage divider. See Figure 25and Table 4
Status			
INTB	27	O, LVCMOS Open Drain	Interrupt INTB = H, normal INTB = L, Interrupt request Recommended pull-up: 4.7kΩ to V_{DDIO}. **DO NOT FLOAT.**
FPD-Link III Serial Interface			
DOUT+	17	I/O, LVDS	True Output The output must be AC-coupled with a 0.1µF capacitor.
DOUT-	16	I/O, LVDS	Inverting Output The output must be AC-coupled with a 0.1µF capacitor.
CMF	20	Analog	Common Mode Filter. Connect 0.1µF to GND (required)
Power(1) and Ground			
VDD33_A VDD33_B	19 26	Power	Power to on-chip regulator **3.0 V - 3.6 V**. Each pin requires a 4.7µF capacitor to GND
VDDIO	7, 24	Power	LVCMOS I/O Power **1.8 V ±5% OR 3.0 V - 3.6 V**. Each pin requires 4.7µF capacitor to GND
GND	DAP	Ground	Large metal contact at the bottom center of the device package **Connect to the ground plane (GND) with at least 9 vias.**
Regulator Capacitor			

(1) The V_{DD} (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise.

Pin Name	Pin #	I/O, Type	Description
CAPP12 CAPHS12 CAPLVD12	12 14 28	CAP	Decoupling capacitor connection for on-chip regulator Each requires a 4.7µF decoupling capacitor to GND.
CAPL12	8	CAP	Decoupling capacitor connection for on-chip regulator Requires two 4.7µF decoupling capacitors to GND
Other			
RES[1:0]	15, 13	GND	Reserved Connect to GND.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Parameter	DS90UB927Q	Unit
Supply Voltage – V_{DD33} (2)	−0.3 to +4.0	V
Supply Voltage – V_{DDIO} (2)	−0.3 to +4.0	V
LVCMOS I/O Voltage	−0.3 to (V_{DDIO} + 0.3)	V
Serializer Output Voltage	−0.3 to +2.75	V
Junction Temperature	+150	°C
Storage Temperature	−65 to +150	°C
40 LLP Package Maximum Power Dissipation Capacity at 25°C		
Derate above 25°C	1/ θ_{JA}	°C/W
θ_{JA}	28.0	°C/W
θ_{JC}	4.4	°C/W
ESD Rating (IEC, powered-up only), R_D = 330Ω, C_S = 150pF		
Air Discharge (D_{OUT+}, D_{OUT-})	≥±15	kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8	kV
ESD Rating (ISO10605), R_D = 330Ω, C_S = 150pF		
Air Discharge (D_{OUT+}, D_{OUT-})	≥±15	kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8	kV
ESD Rating (ISO10605), R_D = 2kΩ, C_S = 150pF or 330pF		
Air Discharge (D_{OUT+}, D_{OUT-})	≥±15	kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8	kV
ESD Rating (HBM)	≥±8	kV
ESD Rating (CDM)	≥±1.25	kV
ESD Rating (MM)	≥±250	V
For soldering specifications: see product folder at www.ti.com and www.ti.com/lit/an/snoa549c/snoa549c.pdf		

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) The DS90UB927Q V_{DD33} and V_{DDIO} voltages require a specific ramp rate during power up. The power supply ramp time must be less than 1.5ms with a monotonic rise

Recommended Operating Conditions

Parameter	Min	Nom	Max	Units
Supply Voltage (V_{DD33})	3.0	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO}) Note: V_{DDIO} < V_{DD33}+0.3V	3.0	3.3	3.6	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
PCLK Frequency	5		85	MHz
Supply Noise ((1))			100	mV_{P-P}

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DD33} and V_{DDIO}supplies with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 50MHz. The Des on the other hand shows no error when the noise frequency is less than 50 MHz.

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
LVCMOS I/O								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0V to 3.6V (4)		PDB	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0V to 3.6V (4)			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO} = 3.0V to 3.6V (4)			−15	±1	+15	µA
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0V to 3.6V		GPIO[1:0] I2S_CLK I2S_WC I2S_D[A,B,C,D] LFMODE MAPSEL BKWD REPEAT	2.0		V_{DDIO}	V
		V_{DDIO} = 1.71V to 1.89V			0.65* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0V to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71V to 1.89V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0V to 3.6V		−15	±1	+15	µA
			V_{DDIO} = 1.71V to 1.89V		−15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4mA	V_{DDIO} = 3.0V to 3.6V	GPIO[3:0], GPO_REG[8:5]	2.4		V_{DDIO}	V
			V_{DDIO} = 1.71V to 1.89V		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4mA	V_{DDIO} = 3.0V to 3.6V		GND		0.4	V
			V_{DDIO} = 1.71V to 1.89V		GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−55		mA
I_{OZ}	TRI-STATE® Output Current	V_{OUT} = 0V or V_{DDIO}, PDB = L,			−15		+15	µA
FPD-Link LVDS Receiver								
V_{TH}	Threshold High Voltage	V_{CM} = 1.2V		RxCLKIN± RxIN[3:0]±			+100	mV
V_{TL}	Threshold Low Voltage				−100			mV
$\|V_{ID}\|$	Differential Input Voltage Swing				200		600	mV
V_{CM}	Common Mode Voltage				0	1.2	2.4	V
I_{IN}	Input Current				−10		+10	µA
FPD-LINK III CML Driver								

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50MHz.

(4) PDB is specified to 3.3V LVCMOS only and must be driven or pulled up to V_{DD33} or to $V_{DDIO} \geq 3.0V$

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)	R_L = 100Ω, Figure 3	DOUT±	800	1000	1200	mV_{p-p}
ΔV_{OD}	Output Voltage Unbalance				1	50	mV
V_{OS}	Offset Voltage – Single-ended	R_L = 100Ω, Figure 3			2.5-0.25*V_{ODp-p} (TYP)		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended				1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, PDB = L or H (5)			−30		mA
R_T	Internal Termination Resistance - Differential			80	100	120	Ω
Supply Current							
I_{DD1}	Supply Current R_L = 100Ω, PCLK = 85MHz	Checkerboard Pattern Figure 10	V_{DD33}= 3.6V		135	160	mA
I_{DDIO1}			V_{DDIO} = 3.6V		100	500	µA
			V_{DDIO} = 1.89V		200	600	µA
I_{DD2}		Random Pattern PRBS7	V_{DD33}= 3.6V		133		mA
I_{DDIO2}			V_{DDIO} = 3.6V		100		µA
			V_{DDIO} = 1.89V		100		µA
I_{DDS}	Supply Current — Remote Auto Power Down	reg_0x01[7]=1, Back channel Idle	V_{DD33} = 3.6V		1.2	2.4	mA
I_{DDIOS}			V_{DDIO} = 3.6V		4	30	µA
			V_{DDIO} = 1.89V		5	30	µA
I_{DDZ}	Supply Current — Power Down	PDB = 0V, All other LVCMOS inputs = 0V	V_{DD33} = 3.6V		1	2.2	mA
I_{DDIOZ}			V_{DDIO} = 3.6V		8	20	µA
			V_{DDIO} = 1.89V		4	20	µA

(5) I_{OS} is not specified for an indefinite period of time. Do not hold in short circuit for more than 500ms or part damage may result

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
FPD-Link LVDS Input							
t_{RSP}	Receiver Strobe Position	Figure 6	RxCLKIN±, RXIN[3:0]±	0.25	0.5	0.75	UI
FPD-Link III CML IO							
t_{LHT}	CML Output Low-to-High Transition Time	Figure 5	DOUT+, DOUT-		100	140	ps
t_{HLT}	CML Output High-to-Low Transition Time				100	140	ps
t_{PLD}	Serializer PLL Lock Time	(4)Figure 7	PCLK = 5MHz to 85MHz			5	ms
t_{SD}	Delay — Latency	Figure 8			146*T		ns
t_{TJIT}	Output Total Jitter, Bit Error Rate ≤1E-9 Figure 9 (5) (6) (7) (8)(9)	Checkerboard Pattern PCLK=5MHz Figure 10	RxCLKIN±		0.17	0.2	UI
		Checkerboard Pattern PCLK=85MHz Figure 10			0.26	0.29	UI
t_{IJIT}	Input Jitter Tolerance, Bit Error Rate ≤1E-9 (10) (6)	f/40 < Jitter Freq < f/20, DES = DS90UH926Q	RxCLKIN±, f = 78MHz		0.6		UI
		f/40 < Jitter Freq < f/20, DES = DS90UB928Q			0.5		UI
I2S Receiver							
T_{I2S}	I2S Clock Period Figure 12, (5) (11)	RxCLKIN± f=5MHz to 85MHz	I2S_CLK, PCLK = 5MHz to 85MHz		>4/PCLK or >77		ns
T_{HC}	I2S Clock High Time Figure 12 (11)		I2S_CLK	0.35			T_{I2S}
T_{LC}	I2S Clock Low Time Figure 12 (11)		I2S_CLK	0.35			T_{I2S}
t_{sr}	I2S Set-up Time Figure 12		I2S_WC I2S_D[A,B,C,D]	0.2			T_{I2S}
t_{htr}	I2S Hold Time Figure 12		I2S_WC I2S_D[A,B,C,D]	0.2			T_{I2S}
Other I/O							

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50MHz.
(4) t_{PLD} is the time required by the device to obtain lock when exiting power-down state with an active PCLK.
(5) Specification is guaranteed by design and is not tested in production
(6) Specification is guaranteed by characterization and is not tested in production
(7) UI – Unit Interval is equivalent to one ideal serialized bit width. The UI scales with PCLK frequency.
(8) Output jitter specs are dependent upon the input clock jitter at the SER
(9) t_{TJIT} (@BER of 1E-9) specifies the allowable jitter on RxCLKIN±
(10) Jitter Frequency is specified in conjunction with DS90UB928Q PLL bandwidth.
(11) I2S specifications for t_{LC} and t_{HC} pulses must each be greater than 2 PCLK periods to guarantee sampling and supersedes the 0.35*T_{I2S_CLK} requirement. t_{LC} and t_{HC} must be longer than the greater of either 0.35*T_{I2S_CLK} or 2*PCLK

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
$t_{GPIO,FC}$	GPIO Pulse Width, Forward Channel		GPIO[3:0], PCLK = 5MHz to 85MHz	>2/PCLK			s
$t_{GPIO,BC}$	GPIO Pulse Width, Back Channel		GPIO[3:0]	20			µs

Recommended Timing for the Serial Control Bus

Over 3.3V supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition Figure 11	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition Figure 11	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD;DAT}$	Data Hold Time Figure 11	Standard Mode	0		3.45	µs
		Fast Mode	0		0.9	µs
$t_{SU;DAT}$	Data Set Up Time Figure 11	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition Figure 11	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Figure 11	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time, Figure 11	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, Figure 11	Standard Mode			300	ns
		Fast mode			300	ns

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50MHz.

DC and AC Serial Control Bus Characteristics

Over 3.3V supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	0.7* V_{DDIO}		V_{DD33}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3* V_{DD33}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA or SCL, IOL = 1.25mA	0		0.36	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	-10		+10	µA
t_R	SDA RiseTime – READ	SDA, RPU = 10kΩ, Cb ≤ 400pF, Figure 11		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Set Up Time — READ	Figure 11		560		ns
$t_{HD;DAT}$	Hold Up Time — READ	Figure 11		615		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50MHz.

AC Timing Diagrams and Test Circuits

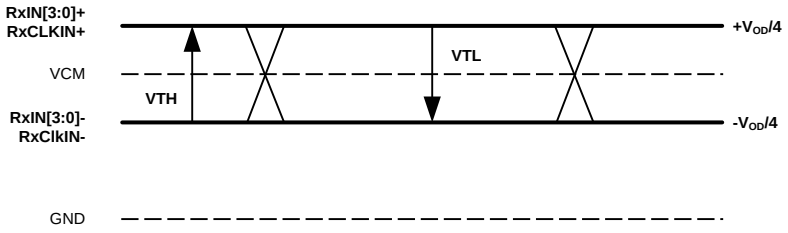
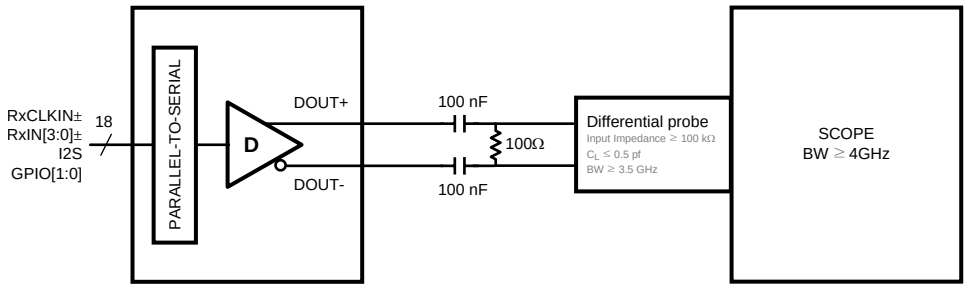


Figure 3. FPD-Link DC V_{TH}/V_{TL} Definition



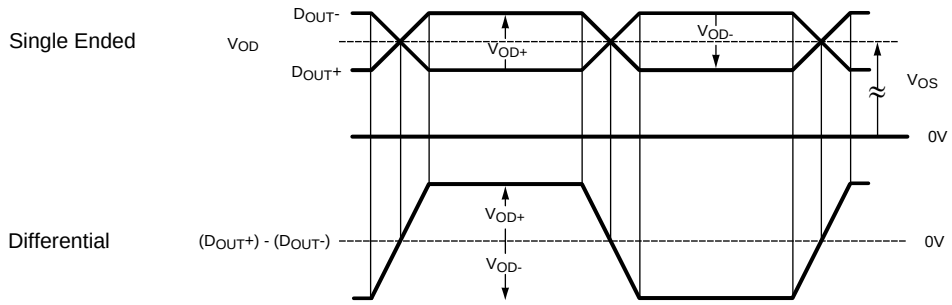


Figure 4. Serializer V_{OD} DC Output

Figure 5. Output Transition Times

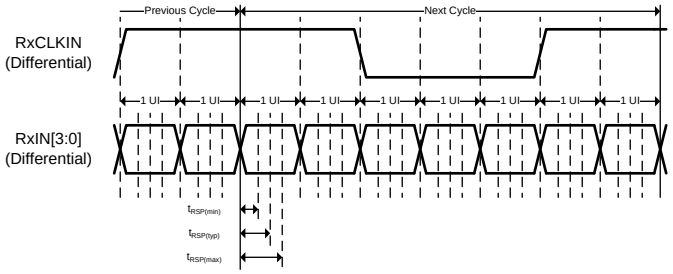


Figure 6. FPD-Link Input Strobe Position

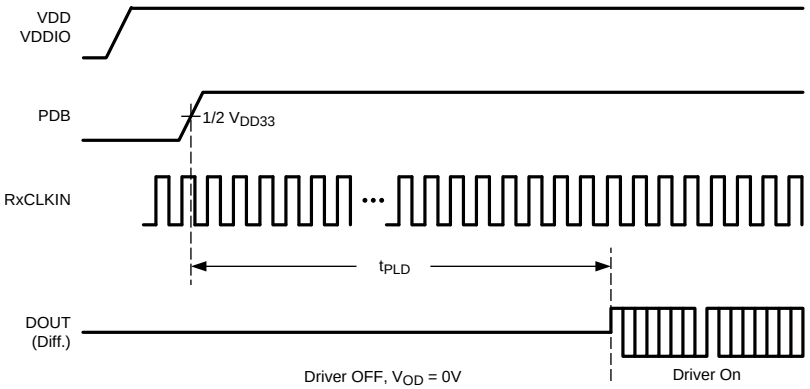


Figure 7. Serializer Lock Time

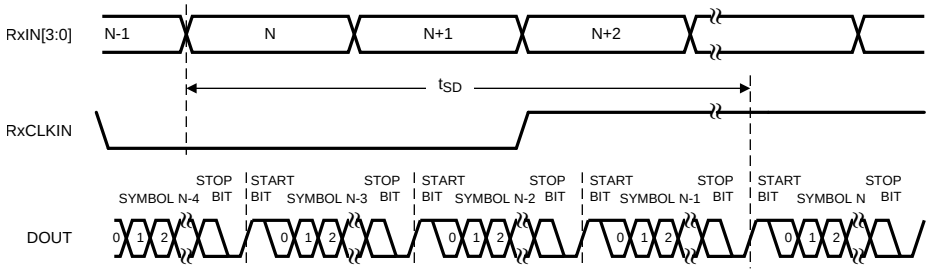


Figure 8. Latency Delay

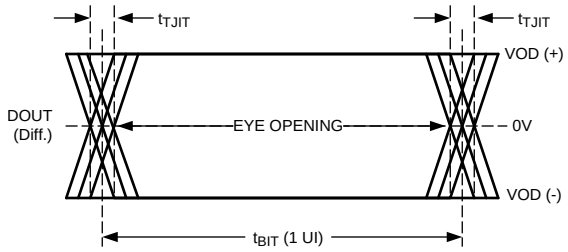


Figure 9. CML Serializer Output Jitter

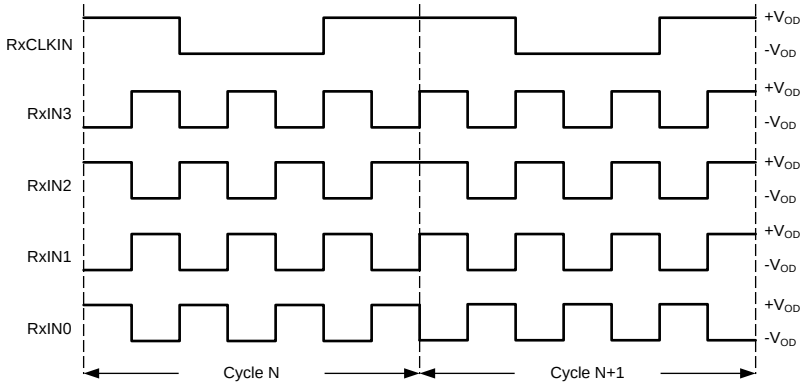


Figure 10. Checkerboard Data Pattern

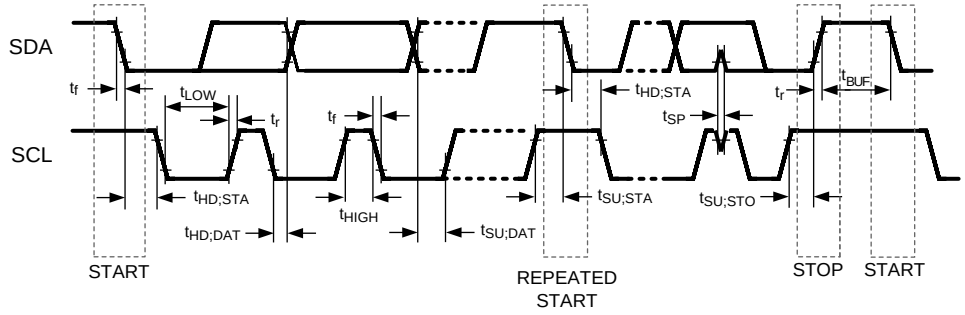


Figure 11. Serial Control Bus Timing Diagram

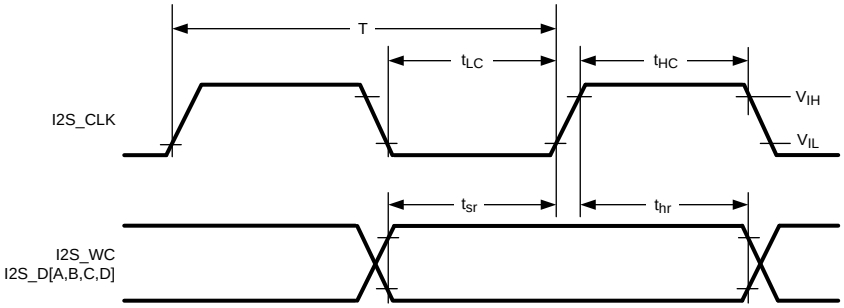


Figure 12. I2S Timing Diagram

Functional Description

The DS90UB927Q converts a FPD-Link interface (4 LVDS data channels + 1 LVDS Clock) to a FPD-Link III interface. This device transmits a 35-bit symbol over a single serial pair operating at up to a 2.975Gbps line rate. The serial stream contains an embedded clock, video control signals, RGB video data, and audio data. The payload is DC-balanced to enhance signal quality and support AC coupling.

The DS90UB927Q serializer is intended for use with a DS90UB928Q or DS90UH926Q deserializer, but is also backward compatible with DS90UR906Q, DS90UR908Q, DS90UR910Q, and DS90UR916Q FPD-Link II deserializers.

The DS90UB927Q serializer and DS90UB928Q or DS90UB926Q deserializer incorporate an I2C compatible interface. The I2C compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I2C slave devices.

The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C compatible masters at either side of the serial link.

There are two operating modes available on DS90UB927Q: display mode and camera mode. In display mode, I2C transactions originate from the host controller attached to the serializer and target either the deserializer or an I2C slave attached to the deserializer. Transactions are detected by the I2C slave in the serializer and forwarded to the I2C master in the deserializer. Similarly, in camera mode, I2C transactions originate from a controller attached to the deserializer and target either the serializer or an I2C slave attached to the serializer. Transactions are detected by the I2C slave in the deserializer and forwarded to the I2C master in the serializer.

HIGH SPEED FORWARD CHANNEL DATA TRANSFER

The High Speed Forward Channel is composed of a 35-bit frame containing RGB data, sync signals, I2C, and I2S audio transmitted from Serializer to Deserializer. Figure 13 illustrates the serial stream generated per PCLK cycle into RxCLKIN±. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, DC-balanced and scrambled.

Figure 13. FPD-Link III Serial Stream

The device supports pixel clock ranges of 5MHz to 15MHz (LFMODE=1) and 15MHz to 85MHz (LFMODE=0). This corresponds to an application payload rate range of 155Mbps to 2.635Gbps, with an actual line rate range of 525Mbps to 2.975Gbps.

LOW SPEED BACK CHANNEL DATA TRANSFER

The Low-Speed Back Channel of the DS90UB927Q provides bidirectional communication between the display and host processor. Data is transferred simultaneously over the same physical link as the high-speed forward channel data. The back channel transports I2C, CRC, and 4 bits of standard GPIO information with a 10Mbps line rate.

BACKWARD COMPATIBLE MODE

The DS90UB927Q is also backward compatible to DS90UR906Q, DS90UR908Q FPD, and DS90UR916Q FPD-Link II deserializers for PCLK frequencies ranging from 5MHz to 65MHz. It is also backward compatible with the DS90UR910Q for PCLK frequencies ranging from 5MHz to 75MHz. The serializer transmits 28-bits of data over a single serial FPD-Link II pair operating at a payload rate of 120Mbps to 1.8Gbps, corresponding to a line rate of 140Mbps to 2.1Gbps. The Backward Compatibility configuration can be selected through the BKWD pin or programmed through the configuration register (Table 5). The bidirectional control channel,, bidirectional GPIOs, I2S, and interrupt (INTB) are not active in this mode. However, local I2C access to the serializer is still available. Note: PCLK frequency range in this mode is 15MHz to 75MHz for LFMODE=0 and 5MHZ to <15MHz for LFMODE=1.

COMMON MODE FILTER PIN (CMF)

The serializer provides access to the center tap of the internal CML termination. A 0.1µF capacitor must be connected from this pin to GND for additional common-mode filtering of the differential pair (Figure 29). This increases noise rejection capability in high-noise environments.

FPD-LINK INPUT FRAME AND COLOR BIT MAPPING SELECT

The DS90UB927Q can be configured to accept 24-bit color (8-bit RGB) with 2 different mapping schemes: LSBs on RxIN[3]±, shown in Figure 14, or MSBs on RxIN[3], shown in Figure 15. Each frame corresponds to a single pixel clock (PCLK) cycle. The LVDS clock input to RxCLKIN± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by MAPSEL pin or by Register (Table 5).

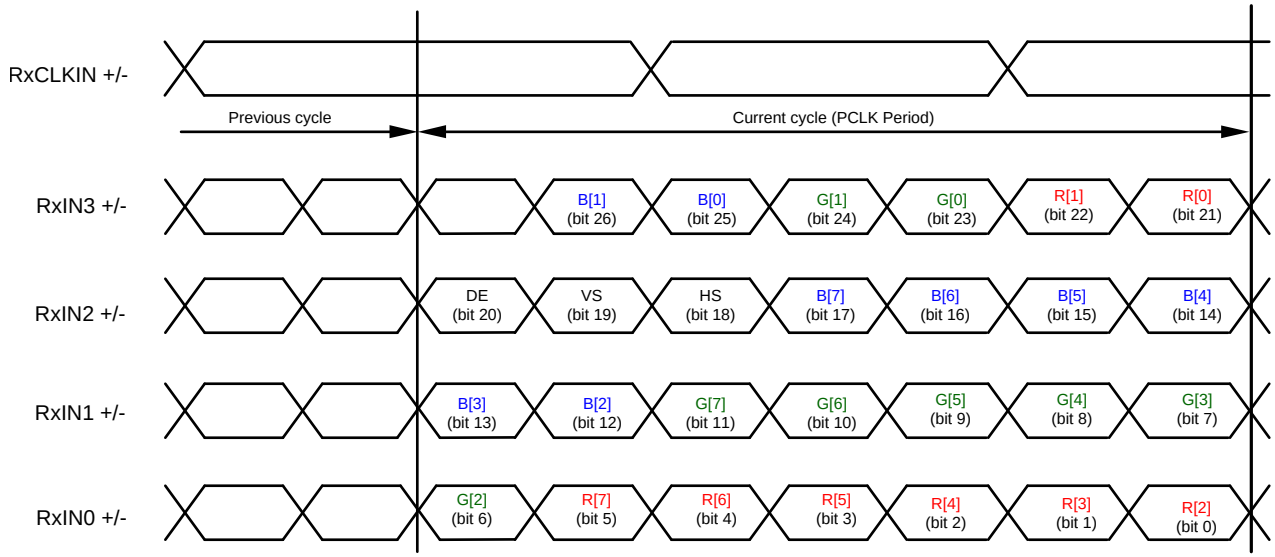


Figure 14. FPD-Link Mapping: LSBs on RxIN3 (MAPSEL=L)

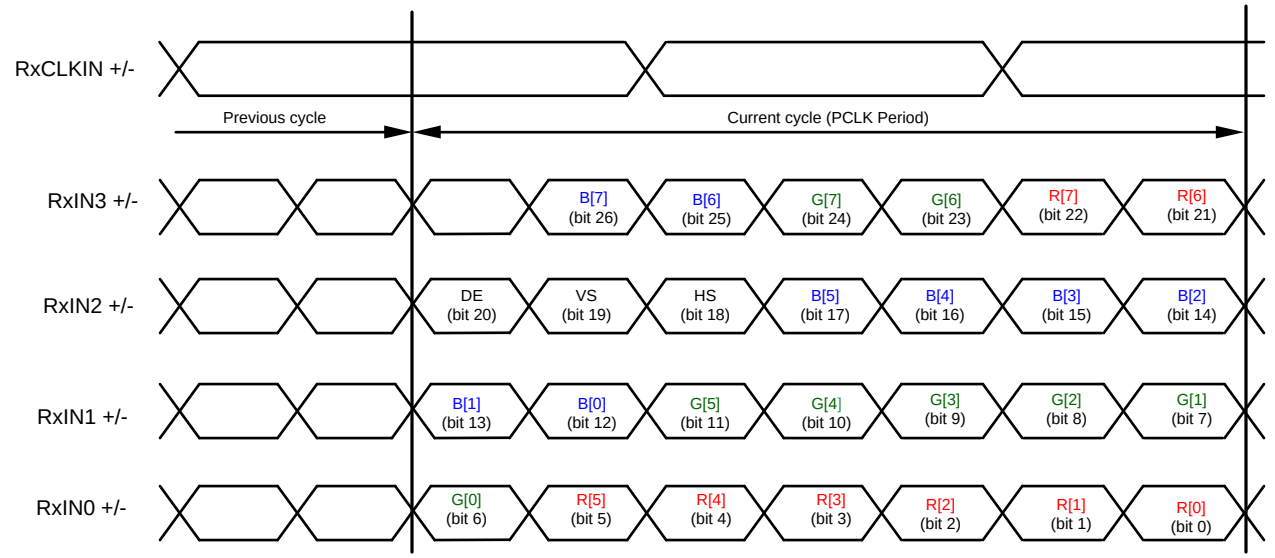


Figure 15. FPD-Link Mapping: MSBs on RxIN3 (MAPSEL=H)

VIDEO CONTROL SIGNALS

The video control signal bits embedded in the high-speed FPD-Link LVDS are subject to certain limitations relative to the video pixel clock period (PCLK). By default, the DS90UB927Q applies a minimum pulse width filter on these signals to help eliminate spurious transitions.

Normal Mode Control Signals (VS, HS, DE) have the following restrictions:

- Horizontal Sync (HS): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 5. HS can have at most two transitions per 130 PCLKs.
- Vertical Sync (VS): The video control signal pulse is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
- Data Enable Input (DE): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 5. DE can have at most two transitions per 130 PCLKs.

EMI REDUCTION FEATURES

LVCMOS V_{DDIO} OPTION

The 1.8V or 3.3V LVCMOS inputs and outputs are powered from separate VDDIO supply pins to offer compatibility with external system interface signals. Note: When configuring the V_{DDIO} power supplies, all the single-ended control input pins for device need to scale together with the same operating V_{DDIO} levels. If V_{DDIO} is selected to operate in the 3.0V to 3.6V range, V_{DDIO} must be operated within 300mV of V_{DD33}.

POWER DOWN (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through V_{DDIO}, where V_{DDIO} = 3.0V to 3.6V or V_{DD33}. To save power, disable the link when the display is not needed (PDB = LOW). Ensure that this pin is not driven HIGH before V_{DD33} and V_{DDIO} have reached final levels. When PDB is driven low, ensure that the pin is driven to 0V for at least 1.5ms before releasing or driving high. In the case where PDB is pulled up to V_{DDIO} = 3.0V to 3.6V or V_{DD33} directly, a 10kΩ pull-up resistor and a >10µF capacitor to ground are required (See Figure 29).

Toggling PDB low will POWER DOWN the device and RESET all control registers to default. During this time, PDB must be held low for a minimum period of time. See AC Electrical Characteristics for more information.

REMOTE AUTO POWER DOWN MODE

The DS90UB927Q serializer features a Remote Auto Power Down mode. This feature is enabled and disabled through the register bit 0x01[7] (Table 5). When the back channel is not detected, either due to an idle or powered-down deserializer, the serializer enters remote auto power down mode. Power dissipation of the serializer is significantly reduced in this mode. The serializer automatically attempts to resume normal operation upon detection of an active back channel from the deserializer. To complete the wake-up process and reactivate forward channel operation, the remote power-down feature must be disabled by either a local I2C host, or by an auto-ACK I2C transaction from a remote I2C host located at the deserializer. The Remote Auto Power Down Sleep/Wake cycle is shown below in Figure 16:

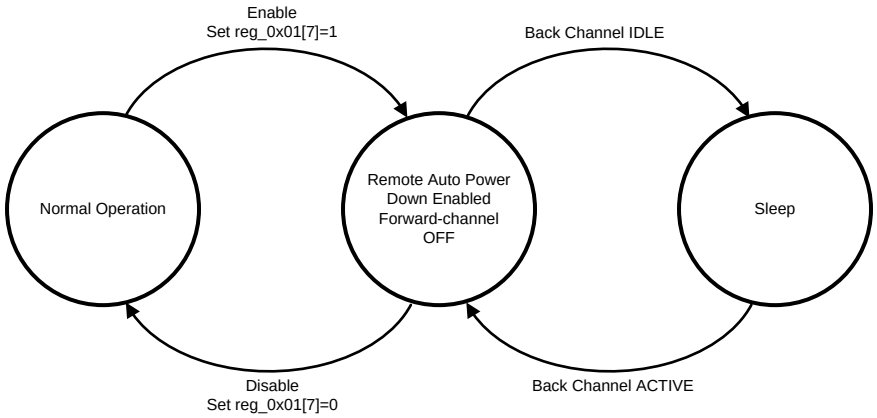


Figure 16. Remote Auto Power Down Sleep/Wake Cycle

To resume normal operation, the Remote Auto Power Down feature must be disabled in the device control register. This may be accomplished from a local I2C controller by writing reg_0x01[7]=0 (Table 5). To disable from a remote I2C controller located at the deserializer, perform the following procedure to complete the wake-up process:

1. Power up remote deserializer (back channel must be active)
2. Enable I2C PASS-THROUGH ALL by setting deserializer register reg_0x05[7]=1
3. Enable I2C AUTO ACK by setting deserializer register reg_0x03[2]=1
4. Disable Remote Auto Power Down by setting serializer register reg_0x01[7]=0
5. Disable I2C AUTO ACK by setting deserializer register reg_0x03[2]=0
6. Disable I2C PASS-THROUGH ALL by setting deserializer register reg_0x05[7]=0

INPUT RxCLKIN LOSS DETECT

The serializer can be programmed to enter a low power SLEEP state when the input clock (PCLK) is lost. A clock loss condition is detected when PCLK drops below approximately 1MHz. When a PCLK is detected again, the serializer will then lock to the incoming RxCLKIN±. Note – when RxCLKIN± is lost, the optional Serial Bus Control Registers values are still retained. See (Table 5) for more information.

SERIAL LINK FAULT DETECT

The DS90UB927Q can detect fault conditions in the FPD-Link III interconnect. If a fault condition occurs, the Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C (Table 5). The DS90UB927Q will detect any of the following conditions:

1. Cable open
2. “+” to “-” short
3. ”+” to GND short
4. ”-” to GND short
5. ”+” to battery short
6. ”+” to battery short
7. Cable is linked incorrectly (DOUT+/DOUT- connections reversed)

Note: The device will detect any of the above conditions, but does not report specifically which one has occurred.

LOW FREQUENCY OPTIMIZATION (LFMODE)

The LFMODE is set via register (Table 5) or LFMODE Pin. This mode optimizes device operation for lower input data clock ranges supported by the serializer. If LFMODE is Low (LFMODE = 0, default), the RxCLKIN± frequency is between 15MHz and 85MHz. If LFMODE is High (LFMODE = 1), the RxCLKIN± frequency is between 5 MHz and <15 MHz. Note: when the device LFMODE is changed, a PDB reset is required. When LFMODE is high (LFMODE=1), the line rate relative to the input data rate is multiplied by four. Thus, for the operating range of 5MHz to <15MHz, the line rate is 700Mbps to <2.1Gbps with an effective data payload of 175Mbps to 525Mbps. Note: for Backwards Compatibility Mode (BKWD=1), the line rate relative to the input data rate remains the same.

INTERRUPT PIN (INTB)

1. On the DS90UB927Q serializer, set register reg_0xC6[5] = 1 and 0xC6[0] = 1 (Table 5) to configure and arm the interrupt.
2. When INTB_IN on the deserializer (DS90UH926Q or DS90UB928Q) is set LOW, the INTB pin on the serializer also pulls low, indicating an interrupt condition.
3. The external controller detects INTB = LOW and reads the ISR register (Table 5) to determine the interrupt source. Reading this register also clears and resets the interrupt.

GENERAL-PURPOSE I/O

GPIO[3:0]

In normal operation, GPIO[3:0] may be used as general purpose IOs in either forward channel (inputs) or back channel (outputs) applications. GPIO modes may be configured from the registers (Table 5). GPIO[1:0] are dedicated pins and GPIO[3:2] are shared with I2S_DC and I2S_DD respectively. Note: if the DS90UB927Q is paired with a DS90UH926Q deserializer, the devices must be configured into 18-bit mode to allow usage of GPIO pins on the DS90UH927 serializer. To enable 18-bit mode, set serializer register reg_0x12[2] = 1. 18-bit mode will be auto-loaded into the deserializer from the serializer. See Table 1 for GPIO enable and configuration.

Table 1. GPIO Enable and Configuration

Description	Device	Forward Channel	Back Channel
GPIO3	DS90UB927Q	0x0F = 0x03	0x0F = 0x05
	DS90UH926/8Q	0x1F = 0x05	0x1F = 0x03
GPIO2	DS90UB927Q	0x0E = 0x30	0x0E = 0x50
	DS90UH926/8Q	0x1E = 0x50	0x1E = 0x30

Table 1. GPIO Enable and Configuration (continued)

Description	Device	Forward Channel	Back Channel
GPIO1	DS90UB927Q	0x0E = 0x03	0x0E = 0x05
	DS90UH926/8Q	0x1E = 0x05	0x1E = 0x03
GPIO0	DS90UB927Q	0x0D = 0x03	0x0D = 0x05
	DS90UH926/8Q	0x1D = 0x05	0x1D = 0x03

The input value present on GPIO[3:0] may also be read from register, or configured to local output mode (Table 5).

GPIO[8:5]

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into REG_GPIO mode. See Table 2 for GPIO enable and configuration.

Note: Local GPIO value may be configured and read either through local register access, or remote register access through the Low-Speed Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

Table 2. GPIO_REG and GPIO Local Enable and Configuration

Description	Register Configuration	Function
GPIO_REG8	0x11 = 0x01	Output, L
	0x11 = 0x09	Output, H
	0x11 = 0x03	Input, Read: 0x1D[0]
GPIO_REG7	0x10 = 0x01	Output, L
	0x10 = 0x09	Output, H
	0x10 = 0x03	Input, Read: 0x1C[7]
GPIO_REG6	0x10 = 0x01	Output, L
	0x10 = 0x09	Output, H
	0x10 = 0x03	Input, Read: 0x1C[6]
GPIO_REG5	0x0F = 0x01	Output, L
	0x0F = 0x09	Output, H
	0x0F = 0x03	Input, Read: 0x1C[5]
GPIO3	0x0F = 0x01	Output, L
	0x0F = 0x09	Output, H
	0x0F = 0x03	Input, Read: 0x1C[3]
GPIO2	0x0E = 0x01	Output, L
	0x0E = 0x09	Output, H
	0x0E = 0x03	Input, Read: 0x1C[2]
GPIO1	0x0E = 0x01	Output, L
	0x0E = 0x09	Output, H
	0x0E = 0x03	Input, Read: 0x1C[1]
GPIO0	0x0D = 0x01	Output, L
	0x0D = 0x09	Output, H
	0x0D = 0x03	Input, Read: 0x1C[0]

I2S AUDIO INTERFACE

The DS90UB927Q serializer features six I2S input pins that, when paired with a DS90UB928Q deserializer, supports surround sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1MHz and <PCLK/2 (or <13MHz). Four I2S data inputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2C_WC) input. I2S audio transport is not available in Backwards Compatibility Mode (BKWD = 1).

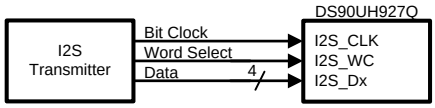


Figure 17. I2S Connection Diagram

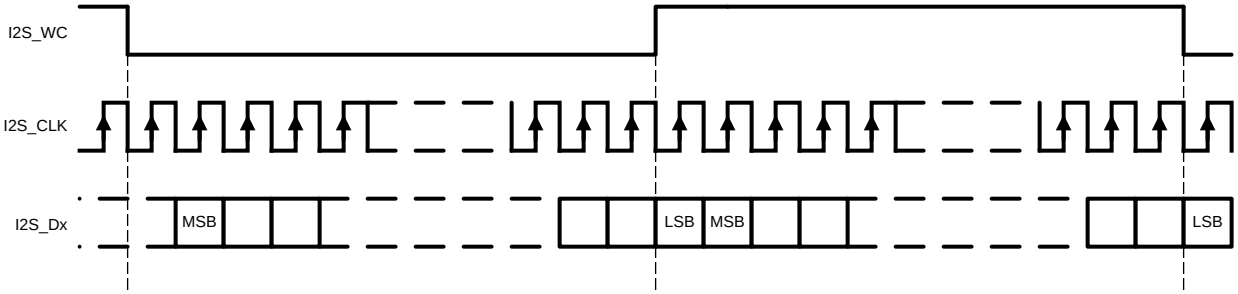


Figure 18. I2S Frame Timing Diagram

When paired with a DS90UH926Q, the DS90UB927Q I2S interface supports a single I2S data input through I2S_DA (24-bit video mode), or two I2S data inputs through I2S_DA and I2S_DB (18-bit video mode).

Table 3 covers several common I2S sample rates:

Table 3. Audio Interface Frequencies

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

I2S TRANSPORT MODES

By default, audio is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames may be disabled from control registers if Forward Channel Frame Transport of I2S data is desired. In this mode, only I2S_DA is transmitted to the DS90UB928Q deserializer. If connected to a DS90UB926Q deserializer, I2S_DA and I2S_DB are transmitted. Surround Sound Mode, which transmits all four I2S data inputs (I2S_D[A..D]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UB928Q deserializer.

I2S REPEATER

I2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated via Data Island Transport on the FPD-Link interface during the video blanking periods. If frame transport is desired, then the I2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level deserializer automatically configures downstream DS90UB927Q serializers and DS90UB928Q deserializers for surround sound transport utilizing Data Island Transport. If 4-channel operation utilizing I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (Table 5).

A DS90UB927Q serializer configured in repeater mode may also regenerate I2S audio from its I2S input pins in lieu of Data Island frames. See the Repeater Connection Diagram (Figure 21) and the I2C Control Registers (Table 5) for additional details.

REPEATER APPLICATION

The supported Repeater application provides a mechanism to extend transmission over multiple links to multiple display devices.

REPEATER CONFIGURATION

In the repeater application, this document refers to the DS90UB927Q as the Transmitter (TX), and refers to the DS90UB928Q as the Receiver (RX). Figure 19 shows the maximum configuration supported for Repeater implementations using the DS90UB925/7Q (TX), and DS90UB926/8Q (RX). Two levels of Repeaters are supported with a maximum of three Transmitters per Receiver. To ensure parallel video interface compatibility, repeater nodes should feature either the DS90UB926Q/DS90UB925Q (RX/TX) chipset or the DS90UB927Q/DS90UB928Q (RX/TX) chipset.

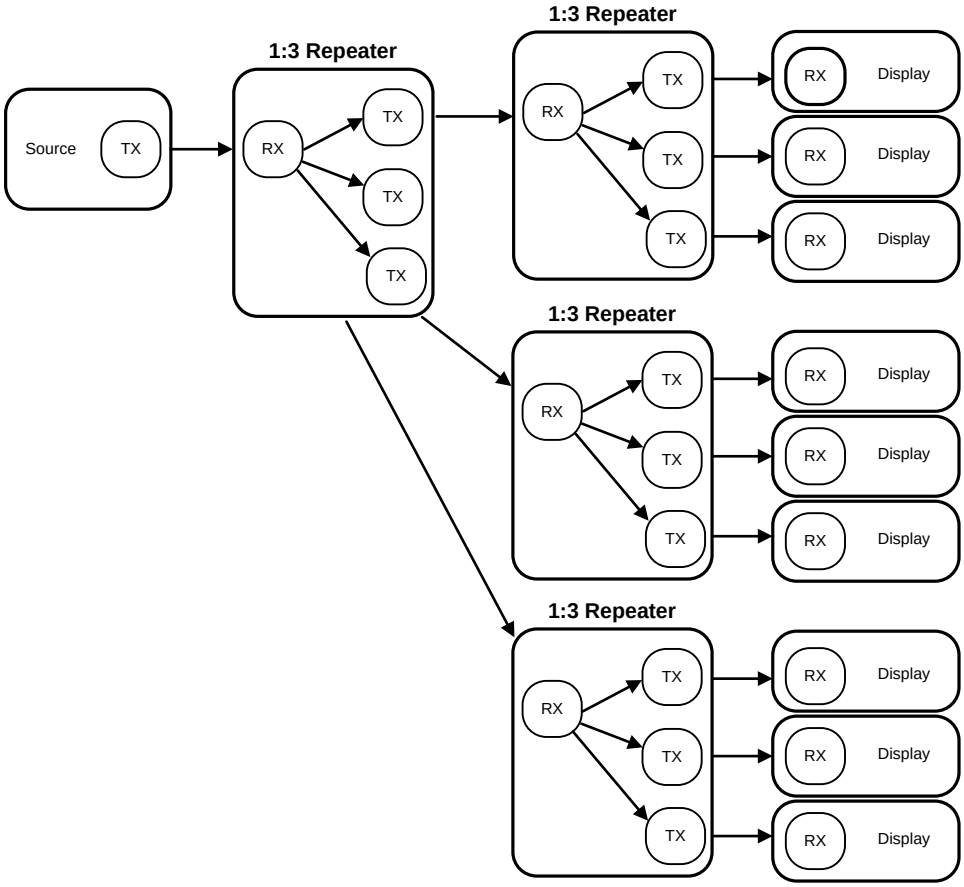


Figure 19. Maximum Repeater Application

In a repeater application, the I2C interface at each TX and RX may be configured to transparently pass I2C communications upstream or downstream to any I2C device within the system. This includes a mechanism for assigning alternate IDs (Slave Aliases) to downstream devices in the case of duplicate addresses.

At each repeater node, the FPD-Link interface fans out to up to three serializer devices, providing video, audio, and control signals and, optionally, packetized audio data (transported during video blanking intervals). Alternatively, the I2S audio interface may be used to transport digital audio data between receiver and transmitters in place of packetized audio. All audio and video data is transmitted at the output of the receiver and is received by the transmitter.

If video data is output to a local display, White Balancing and Hi-FRC dithering functions should not be used as they will block encrypted I2S audio.

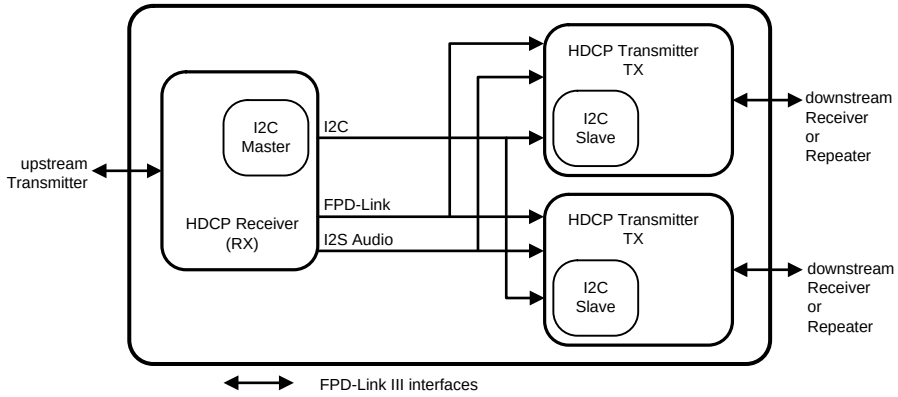


Figure 20. 1:2 Repeater Configuration

REPEATER CONNECTIONS

The Repeater requires the following connections between the Receiver and Transmitter Figure 21.

1. Video Data – Connect all FPD-Link data and clock pairs
2. I2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} or V_{DDIO} = 3.0V to 3.6V with 4.7 kΩ resistors.
3. Audio (optional) – Connect I2S_CLK, I2S_WC, and I2S_Dx signals.
4. IDx pin – Each Transmitter and Receiver must have an unique I2C address.
5. REPEAT pin — All Transmitters and Receivers must be set into Repeater Mode.
6. Interrupt pin – Connect DS90UB928Q INTB_IN pin to DS90UB927Q INTB pin. The signal must be pulled up to V_{DDIO}.

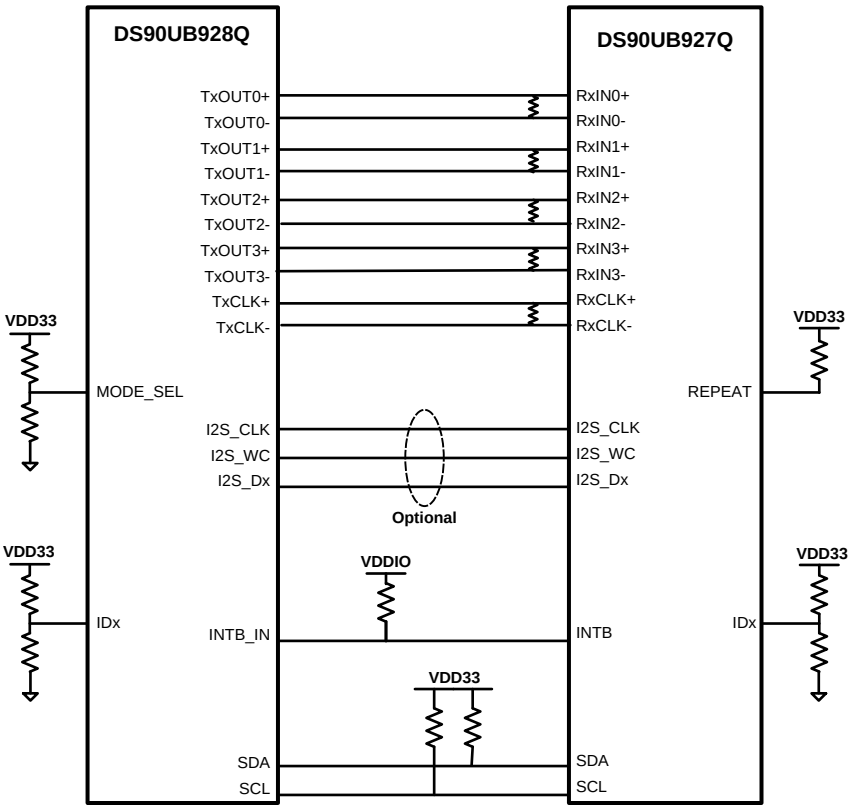


Figure 21. Repeater Connection Diagram

REPEATER FAN-OUT ELECTRICAL REQUIREMENTS

Repeater applications requiring fan-out from one DS90UB928Q deserializer to up to three DS90UB927Q serializers requires special considerations for routing and termination of the FPD-Link differential traces. Figure 22 details the requirements that must be met for each signal pair:

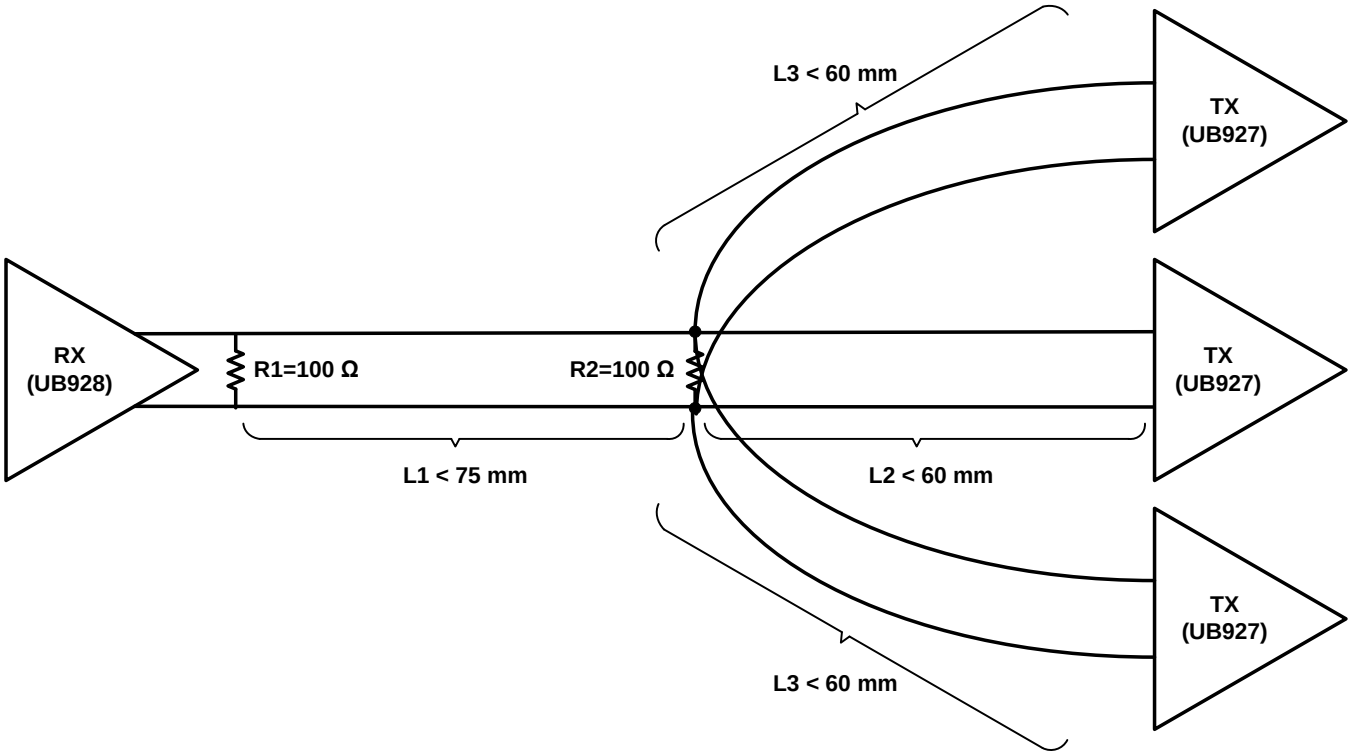


Figure 22. FPD-Link Fan-Out Electrical Requirements

BUILT IN SELF TEST (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and the low-speed back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

BIST CONFIGURATION AND STATUS

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external PCLK or the 33 MHz internal Oscillator clock (OSC) frequency. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK is valid throughout the entire duration of BIST.

See Figure 23 for the BIST mode flow diagram.

SAMPLE BIST SEQUENCE

Step 1: For the DS90UB927Q paired with a FPD-Link III Deserializer, BIST Mode is enabled via the BISTEN pin of Deserializer. The desired clock source is selected through the deserializer BISTC pin.

Step 2: The DS90UB927Q serializer is awakened through the back channel if it is not already on. An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. BIST duration is user-controlled and may be of any length.

The link returns to normal operation after the deserializer BISTEN pin is low. Figure 24 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

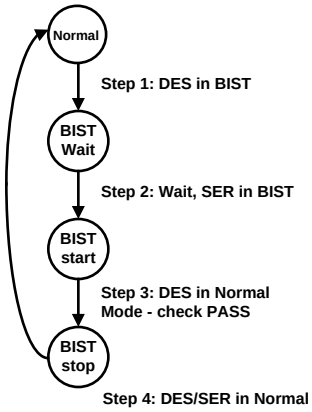


Figure 23. BIST Mode Flow Diagram

FORWARD CHANNEL AND BACK CHANNEL ERROR CHECKING

While in BIST mode, the serializer stops sampling the FPD-Link input pins and switches over to an internal all zeroes pattern. The internal all-zeroes pattern goes through scrambler, dc-balancing, etc. and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 5). CRC errors are recorded in an 8-bit register in the deserializer. The register is cleared when the serializer enters BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until cleared or the serializer enters BIST mode again.

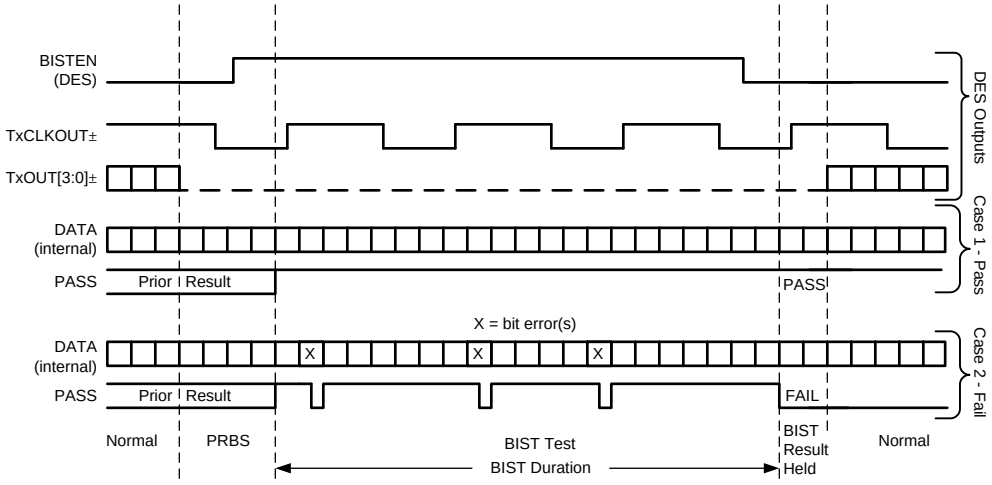


Figure 24. BIST Waveforms

INTERNAL PATTERN GENERATION

The DS90UB927Q serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied. If no clock is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to Application Note AN-2198.

PATTERN OPTIONS

The DS90UB927Q serializer pattern generator is capable of generating 17 default patterns for use in basic testing and debugging of panels. Each can be inverted using register bits (Table 5), shown below:

1. White/Black (default/inverted)
2. Black/White
3. Red/Cyan
4. Green/Magenta
5. Blue/Yellow
6. Horizontally Scaled Black to White/White to Black
7. Horizontally Scaled Black to Red/Cyan to White
8. Horizontally Scaled Black to Green/Magenta to White
9. Horizontally Scaled Black to Blue/Yellow to White
10. Vertically Scaled Black to White/White to Black
11. Vertically Scaled Black to Red/Cyan to White
12. Vertically Scaled Black to Green/Magenta to White
13. Vertically Scaled Black to Blue/Yellow to White
14. Custom Color (or its inversion) configured in PGRS
15. Black-White/White-Black Checkerboard (or custom checkerboard color, configured in PGCTL)
16. YCBR/RBCY VCOM pattern, orientation is configurable from PGCTL
17. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature

Additionally, the Pattern Generator incorporates one user-configurable full-screen 24-bit color, which is controlled by the PGRS, PGGS, and PGBS registers. This is pattern #14. One of the pattern options is statically selected in the PGCTL register when Auto-Scrolling is disabled. The PGTSC and PGTSO1-8 registers control the pattern selection and order when Auto-Scrolling is enabled.

COLOR MODES

By default, the Pattern Generator operates in 24-bit color mode, where all bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode can be activated from the configuration registers (Table 5). In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0.

VIDEO TIMING MODES

The Pattern Generator has two video timing modes – external and internal. In external timing mode, the Pattern Generator detects the video frame timing present on the DE and VS inputs. If Vertical Sync signaling is not present on VS, the Pattern Generator determines Vertical Blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the Pattern Generator uses custom video timing as configured in the control registers. The internal timing generation may also be driven by an external clock. By default, external timing mode is enabled. Internal timing or Internal timing with External Clock are enabled by the control registers (Table 5).

EXTERNAL TIMING

In external timing mode, the Pattern Generator passes the incoming DE, HS, and VS signals unmodified to the video control outputs after a two pixel clock delay. It extracts the active frame dimensions from the incoming signals in order to properly scale the brightness patterns. If the incoming video stream does not use the VS signal, the Pattern Generator determines the Vertical Blank time by detecting a long period of pixel clocks without DE asserted.

PATTERN INVERSION

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

AUTO SCROLLING

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

ADDITIONAL FEATURES

Additional pattern generator features can be accessed through the Pattern Generator Indirect Register Map. It consists of the Pattern Generator Indirect Address (PGIA reg_0x66 — Table 5) and the Pattern Generator Indirect Data (PGID reg_0x67 — Table 5). See TI application Note AN-2198.

Serial Control Bus

The DS90UB927Q may also be configured by the use of a I2C compatible serial control bus. Multiple devices may share the serial control bus (up to 10 device addresses supported). The device address is set via a resistor divider (R1 and R2 — see Figure 25 below) connected to the IDx pin.

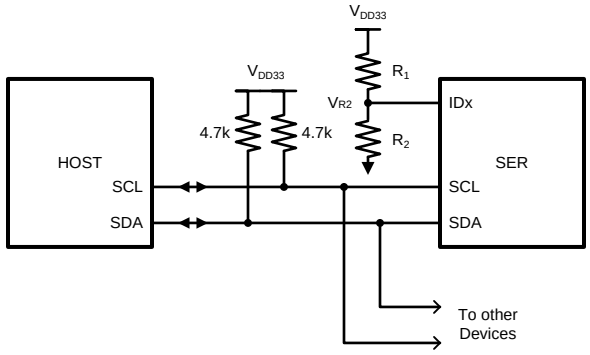


Figure 25. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD33} or V_{DDIO} = 3.0V to 3.6V. For most applications, a 4.7kΩ pull-up resistor to V_{DD33} is recommended. However, the pull-up resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDx pin configures the control interface to one of 10 possible device addresses. A pull-up resistor and a pull-down resistor may be used to set the appropriate voltage ratio between the IDx input pin (V_{R2}) and V_{DD33}, each ratio corresponding to a specific device address. See Table 5 below.

Table 4. Serial Control Bus Addresses for IDx

#	Ideal Ratio V_{R2} / V_{DD33}	Ideal V_{R2} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	Address 7'b	Address 8'b
1	0	0	Open	40.2 or >10	0x0C	0x18
2	0.306	1.011	221	97.6	0x13	0x26
3	0.350	1.154	210	113	0x14	0x28
4	0.393	1.298	196	127	0x15	0x2A
5	0.440	1.452	182	143	0x16	0x2C
6	0.483	1.594	169	158	0x17	0x2E
7	0.529	1.745	147	165	0x18	0x30
8	0.572	1.887	143	191	0x19	0x32
9	0.618	2.040	121	196	0x1A	0x34
10	0.768	2.535	90.9	301	0x1B	0x36

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 26

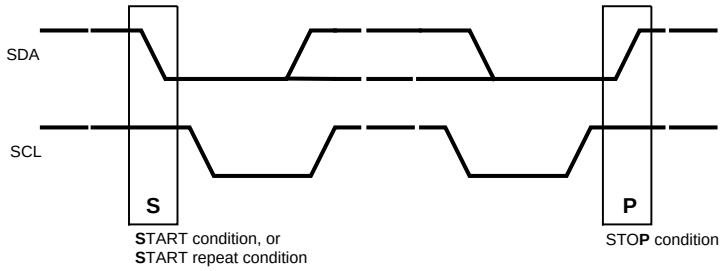


Figure 26. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 25 and a WRITE is shown in Figure 26.

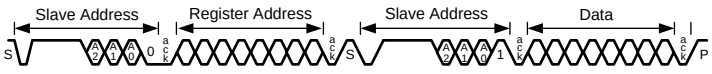


Figure 27. Serial Control Bus — READ

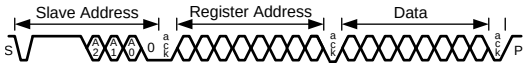


Figure 28. Serial Control Bus — WRITE

The I2C Master located at the DS90UB927Q serializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, please refer to TI Application Note SNLA131.

Table 5. Serial Control Bus Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
0	0x00	I2C Device ID	7:1	RW	IDx	Device ID	7–bit address of Serializer Note: Read-only unless bit 0 is set
			0	RW		ID Setting	I2C ID Setting 0: Device ID is from IDx pin 1: Register I2C Device ID overrides IDx pin
1	0x01	Reset	7	RW	0x00	Remote Auto Power Down	Remote Auto Power Down 0: Do not power down when no Bidirectional Control Channel link is detected (default) 1: Enable power down when no Bidirectional Control Channel link is detected
			6:2				***Reserved***.
			1	RW		Digital RESET1	Reset the entire digital block including registers This bit is self-clearing. 0: Normal operation (default) 1: Reset
			0	RW		Digital RESET0	Reset the entire digital block except registers This bit is self-clearing 0: Normal operation (default) 1: Reset

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
3	0x03	General Configuration	7	RW	0xD2	Back channel CRC Checker Enable	Back Channel Check Enable 0: Disable 1: Enable (default)
			6				***Reserved***.
			5	RW		I2C Remote Write Auto Acknowledge	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus. Note: this mode will prevent any NACK or read/write error indication from a remote device from reaching the I2C master. 0: Disable (default) 1: Enable
			4	RW		Filter Enable	HS, VS, DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 0: Filtering disable 1: Filtering enable (default)
			3	RW		I2C Pass-through	I2C Pass-Through Mode Read/Write transactions matching any entry in the DeviceAlias registers will be passed through to the remote deserializer I2C interface. 0: Pass-Through Disabled (default) 1: Pass-Through Enabled
			2				***Reserved***
			1	RW		PCLK Auto	Switch over to internal OSC in the absence of PCLK 0: Disable auto-switch 1: Enable auto-switch (default)
			0	RW		TRFB	***Reserved***

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
4	0x04	Mode Select	7	RW	0x80	Failsafe State	Input Failsafe State 0: Failsafe to High 1: Failsafe to Low (default)
			6				***Reserved***
			5	RW		CRC Error Reset	Clear back channel CRC Error Counters This bit is NOT self-clearing 0: Normal Operation (default) 1: Clear Counters
			4	RW		DE Gate RGB	DE Gates RGB Data 0: Pass RGB data independent of DE in Backward Compatibility mode and non-HDCP operation (default) 1: Gate RGB data with DE in Backward Compatibility Mode and with non-HDCP deserializers
			3	RW		BKWD ModeOverride	Backward Compatible mode set by BKWD pin or register 0: BC mode is set by BKWD pin (default) 1: BC mode is set by register bit
			2	RW		BKWD	Backward compatibility mode, device to pair with DS90UR906Q, DS90UR908Q, or DS90UR916Q 0: Normal device (default) 1: Compatible with 906/908/916
			1	RW		LFMODE Override	Frequency mode set by LFMODE pin or register 0: Frequency mode is set by LFMODE pin (default) 1: Frequency mode is set by register bit
			0	RW		LFMODE	Frequency mode select 0: High frequency mode (15MHz ≤ RxCLKIN ≤ 85MHz) (default) 1: Low frequency mode (5MHz ≤ RxCLKIN < 15 MHz)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
5	0x05	I2C Control	7:5		0x00		***Reserved***
			4:3	RW		SDA Output Delay	SDA output delay Configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns (default) 01: 280ns 10: 320ns 11: 360ns
			2	RW		Local Write Disable	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer. 0: Enable (default) 1: Disable
			1	RW		I2C Bus Timer Speedup	Speed up I2C Bus Watchdog Timer 0: Watchdog Timer expires after approximately 1s (default) 1: Watchdog Timer expires after approximately 50µs
			0	RW		I2C Bus timer Disable	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1s, the I2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL 0: Enable (default) 1: Disable
6	0x06	DES ID	7:1	RW	0x00	DES Device ID	7-bit Deserializer Device ID Configures the I2C Slave ID of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
			0				***Reserved***
7	0x07	Slave ID 0	7:1	RW	0X00	Slave Device ID 0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Device Alias ID 0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
8	0x08	Slave Alias 0	7:1	RW	0x00	Slave Device Alias ID 0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 0 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
10	0x0A	CRC Errors	7:0	R	0x00	CRC Error LSB	Number of Back Channel CRC errors – 8 least significant bits. Cleared by 0x04[5]
11	0x0B		7:0	R	0x00	CRC Error MSB	Number of Back Channel CRC errors – 8 most significant bits. Cleared by 0x04[5]
12	0x0C	General Status	7:4		0x00		***Reserved***
			3	R		BIST CRC Error	Back Channel CRC error during BIST communication with Deserializer. This bit is cleared upon loss of link, restart of BIST, or assertion of CRC ERROR RESET in register 0x04. 0: No CRC errors detected during BIST (default) 1: CRC Errors detected during BIST
			2	R		PCLK Detect	Pixel Clock Status 0: Valid PCLK not detected (default) 1: Valid PCLK detected
			1	R		DES Error	CRC error during BIST communication with Deserializer. This bit is cleared upon loss of link or assertion of 0x04[5] 0: No CRC errors detected (default) 1: CRC errors detected
			0	R		LINK Detect	LINK Detect Status 0: Cable link not detected (default) 1: Cable link detected

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
13	0x0D	GPIO0 Configuration	7:4	R	0x20	Revision ID	Revision ID: 0010: Production Device
			3	RW		GPIO0 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO0 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			1	RW		GPIO0 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPIO0 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
14	0x0E	GPIO1 and GPIO2 Configuration	7	RW	0x00	GPIO2 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			6	RW		GPIO2 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			5	RW		GPIO2 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO2 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO1 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO1 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			1	RW		GPIO1 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO1 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
15	0x0F	GPIO3 Configuration	7:4		0x00		***Reserved***
			3	RW		GPIO3 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO3 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			1	RW		GPIO3 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPIO3 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
16	0x10	GPIO_REG5 and GPIO_REG6 Configuration	7	RW	0x00	GPIO_REG6 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			6				***Reserved***
			5	RW		GPIO_REG6 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO_REG6 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO_REG5 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			2				***Reserved***
			1	RW		GPIO_REG5 Direction	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			0	RW		GPIO_REG5 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
17	0x11	GPIO_REG7 and GPIO_REG8 Configuration	7	RW	0x00	GPIO_REG8 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			6				***Reserved***
			5	RW		GPIO_REG8 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO_REG8 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO_REG7 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			2				***Reserved***
			1	RW		GPIO_REG7 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPO_REG7 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
18	0x12	Data Path Control	7:6		0x00		***Reserved***
			5	RW		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 0: DE is positive (active high, idle low) (default) 1: DE is inverted (active low, idle high)
			4	RW		I2S Repeater Regen	Regenerate I2S Data From Repeater I2S Pins 0: Repeater pass through I2S from video pins (default) 1: Repeater regenerate I2S from I2S pins
			3	RW		I2S Channel B Enable Override	I2S Channel B Override 0: Set I2S Channel B Disabled (default) 1: Set I2S Channel B Enable from reg_12[0]
			2	RW		18-bit Video Select	Video Color Depth Mode 0: Select 24-bit video mode (default) 1: Select 18-bit video mode
			1	RW		I2S Transport Select	Select I2S Transport Mode 0: Enable I2S Data Island Transport (default) 1: Enable I2S Data Forward Channel Frame Transport
			0	RW		I2S Channel B Enable	I2S Channel B Enable 0: I2S Channel B disabled (default) 1: Enable I2S Channel B

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
19	0x13	General Purpose Control	7	R	0x10	MAPSEL Mode	Returns Map Select Mode (MAPSEL) pin status
			6	RW		MAPSEL Override	FPD-Link Map Select (MAPSEL) set by input pin or register 0: Map Select is set by input pin (default) 1: Map Select is set by register bit 0x13[5]
			5	RW		MAPSEL Value	FPD-Link Map Select (MAPSEL) value when 0x13[6] is set 0: LSBs on RxIN3± (default) 1: MSBs on RxIN3±
			4				***Reserved***
			3	R		LFMODE Status	Low Frequency Mode (LFMODE) pin status 0: 15 ≤ RxCLKIN ≤ 85MHz (default) 1: 5 ≤ RxCLKIN < 15MHz
			2	R		REPEAT Status	Repeater Mode (REPEAT) pin Status 0: Non-repeater (default) 1: Repeater
			1	R		BKWD Status	Backward Compatible Mode (BKWD) Status 0: Compatible to DS90UB926/8Q (default) 1: Backward compatible to DS90UR906/8Q
			0	R		I2S_DB Status	I2S Channel B Mode (I2S_DB) Status 0: I2S_DB inactive (default) 1: I2S_DB active
20	0x14	BIST Control	7:3		0x00		***Reserved***
			2:1	RW		OSC Clock Source	Internal OSC clock select for Functional Mode or BIST. Functional Mode when PCLK is not present and 0x03[1]=1. 00: 33 MHz Oscillator (default) 01: 33 MHz Oscillator Clock Source in BIST mode 00: External Pixel Clock (default) 01: 33 MHz Oscillator Note: In LFMODE=1, the internal oscillator is 12.5MHz
			0	R		BIST Enable	BIST Control 0: Disabled (default) 1: Enabled
22	0x16	BCC Watchdog Control	7:1	RW	0xFE	Timer Value	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
			0	RW		Timer Control	Disable BCC Watchdog Timer 0: Enable BCC Watchdog Timer operation (default) 1: Disable BCC Watchdog Timer operation

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
23	0x17	I2C Control	7	RW	0x1E	I2C Pass All	Pass All 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID. (default) 1: Enable Forward Control Channel pass-through of all I2C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID.
			6:4	RW		SDA Hold Time	Internal SDA Hold Time Configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
			3:0	RW		I2C Filter Depth	Configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.
24	0x18	SCL High Time	7:0	RW	0xA1	SCL HIGH Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency.
25	0x19	SCL Low Time	7:0	RW	0xA5	SCL LOW Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency.
26	0x1A	Data Path Control 2	7	RW	0x00	Block I2S Auto Config	Block automatic I2S mode configuration (repeater only) 0: I2S mode (2-channel, 4-channel, or surround) is detected from the in-band audio signaling 1: Disable automatic detection of I2S mode
			6:1				***Reserved***
			0	RW		I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport 0: 2-channel or 4-channel I2S audio is enabled as configured in register 0x12 bits 3 and 0 (default) 1: 5.1- or 7.1-channel audio is enabled Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.
27	0x1B	BIST BC Error Count	7:0	R	0x00	BIST BC Errorr	BIST Back Channel CRC Error Counter This register stores the back-channel CRC error count during BIST Mode (saturates at 255 errors). Clears when a new BIST is initiated or by 0x04[5]

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
28	0x1C	GPIO Pin Status 1	7	R	0x00	GPIO_REG7 Pin Status	GPIO_REG7 Input Pin Status Status valid only if set to GPI (input) mode
			6	R		GPIO_REG6 Pin Status	GPIO_REG6 Input Pin Status Status valid only if set to GPI (input) mode
			5	R		GPIO_REG5 Pin Status	GPIO_REG5 Input Pin Status Status valid only if set to GPI (input) mode
			4				***Reserved***
			3	R		GPIO3 Pin Status	GPIO3 Input Pin Status Status valid only if set to GPI (input) mode
			2	R		GPIO2 Pin Status	GPIO2 Input Pin Status Status valid only if set to GPI (input) mode
			1	R		GPIO1 Pin Status	GPIO1 Input Pin Status Status valid only if set to GPI (input) mode
			0	R		GPIO0 Pin Status	GPIO0 Input Pin Status Status valid only if set to GPI (input) mode
29	0x1D	GPIO Pin Status 2	7:1		0x00		***Reserved***
			0	R		GPIO_REG8 Pin Status	GPIO_REG8 Input Pin Status Status valid only if set to GPI (input) mode
30	0x1F	Frequency Counter	7:0	RW	0x00	Frequency Counter	Frequency Counter Control Write: Measure number of pixel clock periods in written interval (40ns units) Read: Return number of pixel clock periods counted

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
32	0x20	Deserializer Capabilities	7	RW	0x00	Freeze DES CAP	Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x20 and 0x21. 0: Normal operation (default) 1: Freeze
			6:2				***Reserved***
			1	RW		HD Audio	Deserializer supports 24-bit video concurrently with HD audio This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. 0: Normal operation (default) 1: Freeze
			0	RW		FC GPIO	Deserializer supports GPIO in the Forward Channel Frame This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. 0: Normal operation (default) 1: Freeze

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select Selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. xxxx: normal/inverted 0000: Checkerboard 0001: White/Black (default) 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontal Black-White/White-Black 0111: Horizontal Black-Red/White-Cyan 1000: Horizontal Black-Green/White-Magenta 1001: Horizontal Black-Blue/White-Yellow 1010: Vertical Black-White/White— Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertical Black-Green/White-Magenta 1101: Vertical Black-Blue/White-Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: VCOM See TI App Note AN-2198.
			3				***Reserved***
			2	RW		Color Bars Pattern	Enable Color Bars 0: Color Bars disabled (default) 1: Color Bars enabled Overrides the selection from reg_0x64[7:4]
			1	RW		VCOM Pattern Reverse	Reverse order of color bands in VCOM pattern 0: Color sequence from top left is (YCBR) (default) 1: Color sequence from top left is (RBCY)
			0	RW		Pattern Generator Enable	Pattern Generator Enable 0: Disable Pattern Generator (default) 1: Enable Pattern Generator

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
101	0x65	Pattern Generator Configuration	7		0x00		***Reserved***
			6	RW		Checkerboard Scale	Scale Checkered Patterns: 0: Normal operation (each square is 1x1 pixel) (default) 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels) Setting this bit gives better visibility of the checkered patterns.
			5	RW		Custom Checkerboard	Use Custom Checkerboard Color 0: Use white and black in the Checkerboard pattern (default) 1: Use the Custom Color and black in the Checkerboard pattern
			4	RW		PG 18–bit Mode	18-bit Mode Select: 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness. (default) 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits.
			3	RW		External Clock	Select External Clock Source: 0: Selects the internal divided clock when using internal timing (default) 1: Selects the external pixel clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Timing Select	Timing Select Control: 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. (default) 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. See TI App Note AN-2198.
			1	RW		Color Invert	Enable Inverted Color Patterns: 0: Do not invert the color output. (default) 1: Invert the color output. See TI App Note AN-2198.
			0	RW		Auto Scroll	Auto Scroll Enable: 0: The Pattern Generator retains the current pattern. (default) 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. See TI App Note AN-2198.
102	0x66	PGIA	7:0	RW	0x00	PG Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
103	0x67	PGID	7:0	RW	0x00	PG Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See TI App Note AN-2198
112	0x70	Slave ID[1]	7:1	RW	0x00	Slave ID 1	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
113	0x71	Slave ID[2]	7:1	RW	0x00	Slave ID 2	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
114	0x72	Slave ID[3]	7:1	RW	0x00	Slave ID 3	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
115	0x73	Slave ID[4]	7:1	RW	0x00	Slave ID 4	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
116	0x74	Slave ID[5]	7:1	RW	0x00	Slave ID 5	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
117	0x75	Slave ID[6]	7:1	RW	0x00	Slave ID 6	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
118	0x76	Slave ID[7]	7:1	RW	0x00	Slave ID 7	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
119	0x77	Slave Alias[1]	7:1	RW	0x00	Slave Alias ID 1	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
120	0x78	Slave Alias[2]	7:1	RW	0x00	Slave Alias ID 2	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
121	0x79	Slave Alias[3]	7:1	RW	0x00	Slave Alias ID 3	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
122	0x7A	Slave Alias[4]	7:1	RW	0x00	Slave Alias ID 4	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
123	0x7B	Slave Alias[5]	7:1	RW	0x00	Slave Alias ID 5	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
124	0x7C	Slave Alias[6]	7:1	RW	0x00	Slave Alias ID 6	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
125	0x7D	Slave Alias[7]	7:1	RW	0x00	Slave Alias ID 7	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
198	0xC6	ICR	7:6		0x00		***Reserved***
			5	RW		IS_RX_INT	Interrupt on Receiver interrupt Enables interrupt on indication from the Receiver. Allows propagation of interrupts from downstream devices
			4:1				***Reserved***
199	0xC7	ISR	7:6		0x00		***Reserved***
			5	R		IS RX INT	Interrupt on Receiver interrupt Receiver has indicated an interrupt request from downstream device
			4:1				***Reserved***
			0	R		INT Enable	Global Interrupt Enable Set if any enabled interrupt is indicated
240	0xF0	TX ID	7:0	R	0x5F	ID0	First byte ID code, '_'
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code, 'U'
242	0xF2		7:0	R	0x42	ID2	Third byte of ID code. 'B'
243	0xF3		7:0	R	0x39	ID3	Forth byte of ID code: '9'
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: "2"
245	0xF5		7:0	R	0x37	ID5	Sixth byte of ID code: "7"

Applications Information

DISPLAY APPLICATION

The DS90UB927Q, in conjunction with the DS90UB928Q or DS90UH926Q, is intended for interface between a host (graphics processor) and a display, supporting 24-bit color depth (RGB888) and high definition (720p) digital video format. It can receive an 8-bit RGB stream with a pixel clock rate up to 85 MHz together with three control bits (VS, HS and DE) and four I2S audio streams.

TYPICAL APPLICATION CONNECTION

Figure 29 shows a typical application of the DS90UB927Q serializer for an 85 MHz 24-bit Color Display Application. The 5 LVDS input pairs require external 100Ω terminations. The CML outputs must have an external 0.1µF AC coupling capacitor on the high speed serial lines. The serializer has internal CML termination on its high speed outputs.

Bypass capacitors should be placed near the power supply pins. At a minimum, four (4) 4.7µF capacitors should be used for local device bypassing. Ferrite beads are placed on the two sets of supply pins (VDD33 and VDDIO) for effective noise suppression. The interface to the graphics source is LVDS. The VDDIO pins may be connected to 3.3V or 1.8V. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable.

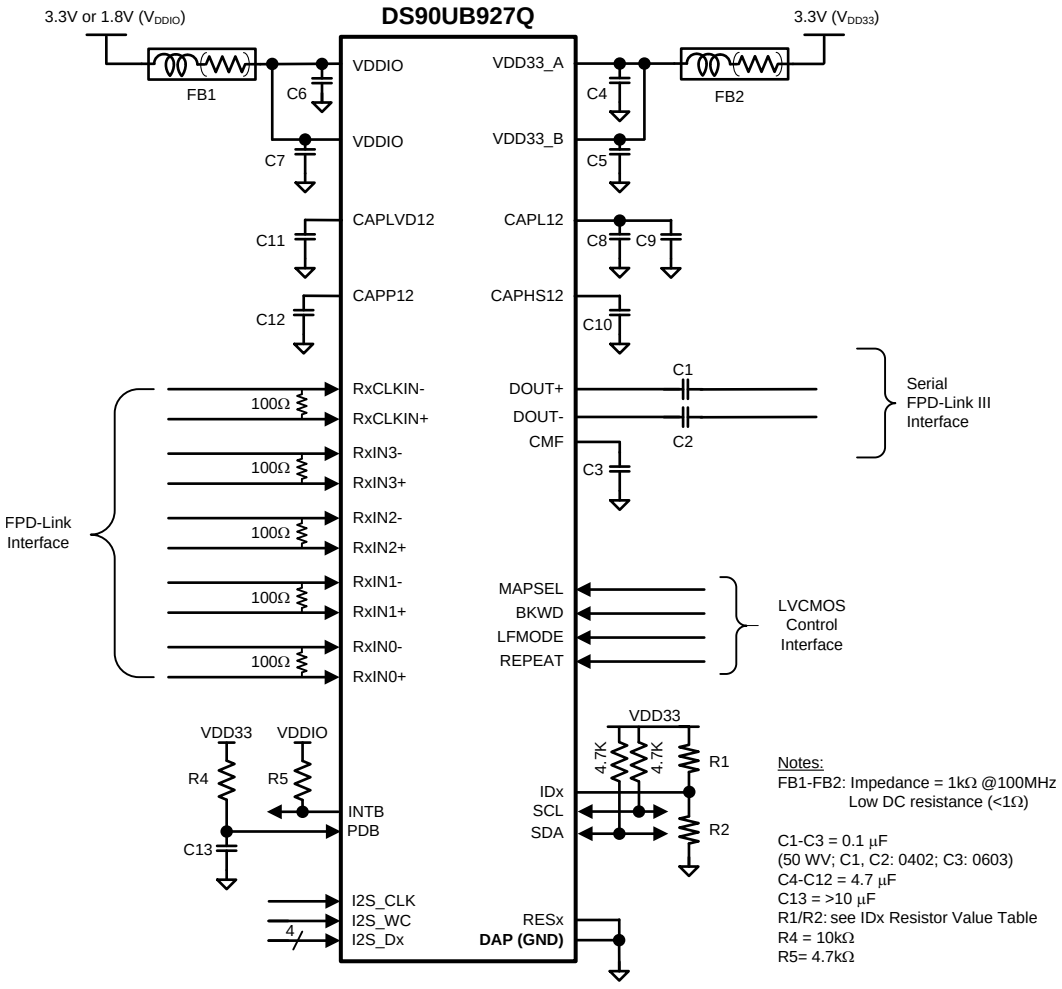


Figure 29. Typical Connection Diagram

POWER UP REQUIREMENTS AND PDB PIN

The power supply ramp (V_{DD33} and V_{DDIO}) should be faster than 1.5ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to V_{DD33}, a 10kΩ pull-up and a >10µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both V_{DD33} and V_{DDIO} has reached steady state. Pins VDD33_A and VDD33_B should both be externally connected, bypassed, and driven to the same potential (they are not internally connected).

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01µF to 10µF. Tantalum capacitors may be in the 2.2µF to 10µF range. The voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50µF to 100µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20MHz-30MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs. For DS90UB927Q, only one common ground plane is required to connect all device related ground pins.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 9 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the LLP style package, including PCB design and manufacturing requirements, is provided in TI Application Note: AN-1187.

CML INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: http://www.ti.com/lit/ml/snla187/snla187.pdf

Revision

- **October 26, 2012**
  - Initial Release

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90UB927QSQ/NOPB	ACTIVE	WQFN	RTA	40	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 105	UB927QSQ	Samples
DS90UB927QSQE/NOPB	ACTIVE	WQFN	RTA	40	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 105	UB927QSQ	Samples
DS90UB927QSQX/NOPB	ACTIVE	WQFN	RTA	40	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	UB927QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

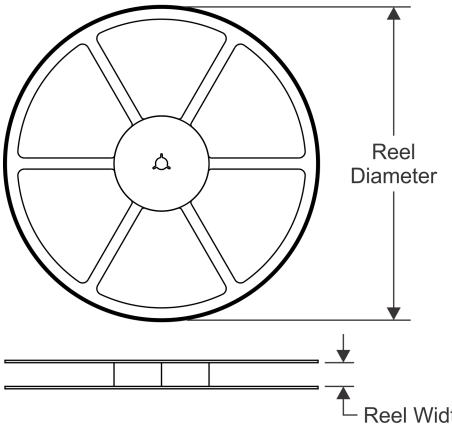
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

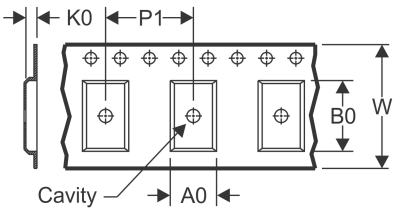
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

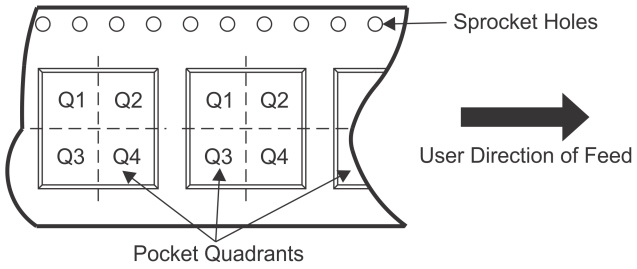


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

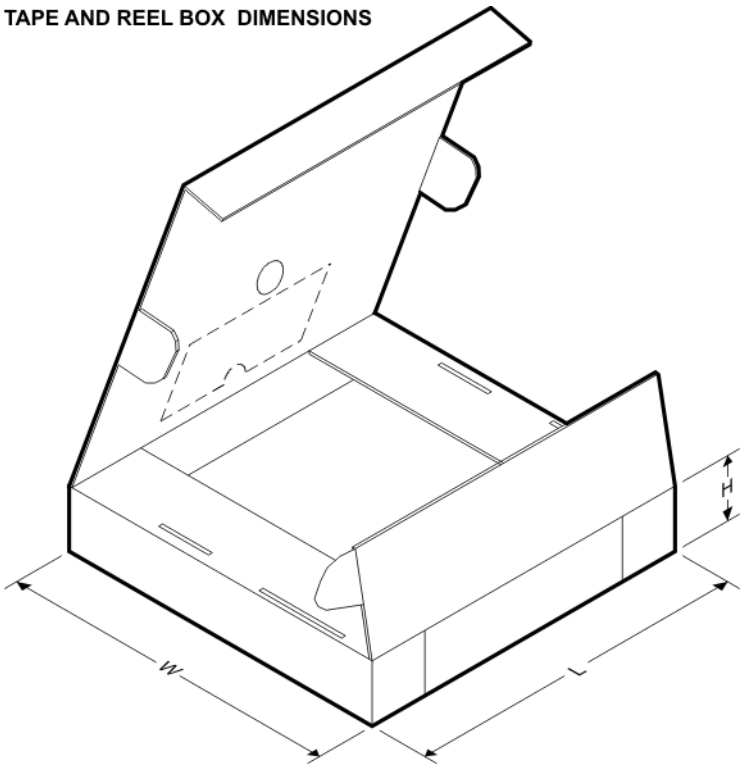
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB927QSQ/NOPB	WQFN	RTA	40	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UB927QSQE/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UB927QSQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

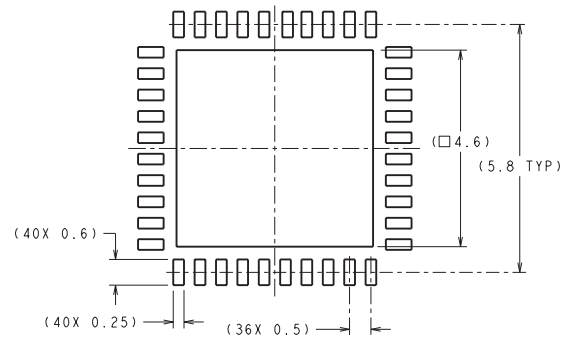
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

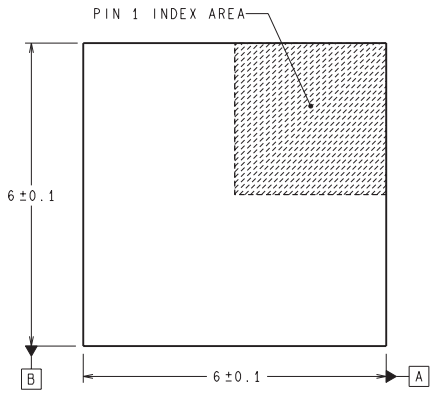
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB927QSQ/NOPB	WQFN	RTA	40	1000	367.0	367.0	38.0
DS90UB927QSQE/NOPB	WQFN	RTA	40	250	213.0	191.0	55.0
DS90UB927QSQX/NOPB	WQFN	RTA	40	2500	367.0	367.0	38.0

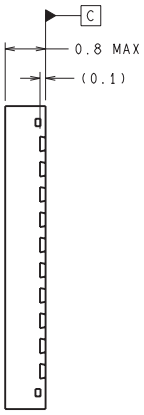
RTA0040A

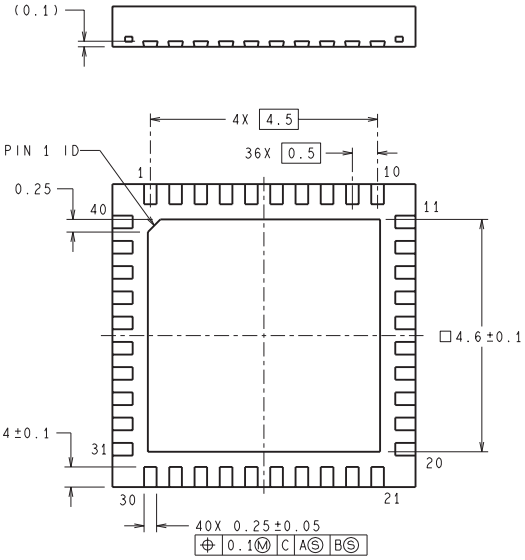


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SQA40A (Rev B)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265