DS92LV242x 10-MHz to 75-MHz, 24-Bit Channel Link II Serializer And Deserializer

1 Features

- 24-Bit Data, 3-Bit Control, 10- to 75-MHz Clock
- AC-Coupled STP Interconnect Cable up to 10 m
- Integrated Terminations on Serializer and Deserializer
- At-Speed Link BIST Mode and Reporting Pin
- Optional I^2C-Compatible Serial Control Bus
- Power-Down Mode Minimizes Power Dissipation
- 1.8-V or 3.3-V Compatible LVCMOS I/O Interface
- –40° to 85°C Temperature Range
- >8-kV HBM
- Serializer (DS92LV2421)
  - Data Scrambler for Reduced EMI
  - DC-Balance Encoder for AC Coupling
  - Selectable Output VOD and Adjustable De-emphasis
- Deserializer (DS92LV2422)
  - Fast Random Data Lock; No Reference Clock Required
  - Adjustable Input Receiver Equalization
  - LOCK (Real-Time Link Status) Reporting Pin
  - EMI Minimization on Output Parallel Bus (SSCG)
  - Output Slew Control (OS)

2 Applications

- Embedded Videos and Displays
- Medical Imaging and Factory Automation
- Office Automation (Printers and Scanners)
- Security and Video Surveillance
- General-Purpose Data Communication

3 Description

The DS92LV242x chipset translates a parallel 24–bit LVCMOS data interface into a single high-speed CML serial interface with embedded clock information. This single serial stream eliminates skew issues between clock and data, reduces connector size, and reduces interconnect cost for transferring a 24-bit or less bus over FR-4 printed-circuit board backplanes and balanced cables. In addition, the DS92LV242x chipset also features a 3-bit control bus for slow speed signals. This allows for video and display applications with up to 24 bits per pixel (RGB).

Programmable transmit de-emphasis, receive equalization, on-chip scrambling, and DC balancing enables longer distance transmission over lossy cables and backplanes. The DS92LV2422 automatically locks to incoming data without an external reference clock or special sync patterns, providing easy *plug-and-go* operation. EMI is minimized by the use of low voltage differential signaling, receiver drive strength control, and spread spectrum clocking capability.

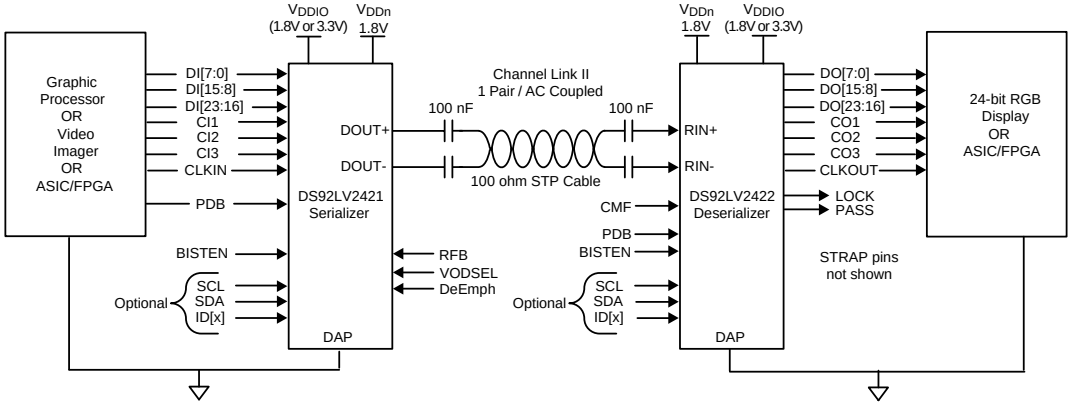
The DS92LV242x chipset is programmable though an I^2C interface as well as through pins. A built-in, at-speed BIST feature validates link integrity and may be used for system diagnostics. The DS92LV2421 is offered in a 48-pin WQFN, and the DS92LV2422 is offered in a 60-pin WQFN package. Both devices operate over the full industrial temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS92LV2421	WQFN (48)	7.00 mm × 7.00 mm
DS92LV2422	WQFN (60)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated thermal characteristic values based on latest simulation data ... 11
- Changed deserializer LVCMOS DC and supply current specification test conditions based on latest production tests ... 12
- Changed I_{OL} test condition for V_{OL} at V_{DDIO} = 3.3 V to 3 mA ... 12
- Changed max value of Deserializer V_{OL} to 0.45 V ... 12
- Changed test condition parameter for V_{OL} Serial Control Characteristic ... 13
- Changed RPU = 10 kΩ condition for the *Serial Control Bus Characteristics* of t_R and t_F ... 13
- Added notes for serializer and deserializer switching characteristics verified by characterization ... 14
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- Changed "NA" and "Disable" term in Table 5 and Table 6 to "Off" ... 28
- Changed output states to correct values based on OSS_SEL and PDB configuration in Table 7 ... 29
- Added details for Deserializer Map Select strap pin configuration ... 33
- Added clarification on the state of deserializer outputs during BIST mode operation ... 33
- Added statement to set input to low when entering BIST mode with DS90C241 or DS90UR241 ... 33
- Added note that ID[X] cannot be tied to VSS, as only four device addresses are supported ... 35
- Added RID tolerance and tablenote that RID ≠ 0 Ω to set ID[X] ... 35
- Changed statement that CONFIG settings can also by programmed via register ... 37

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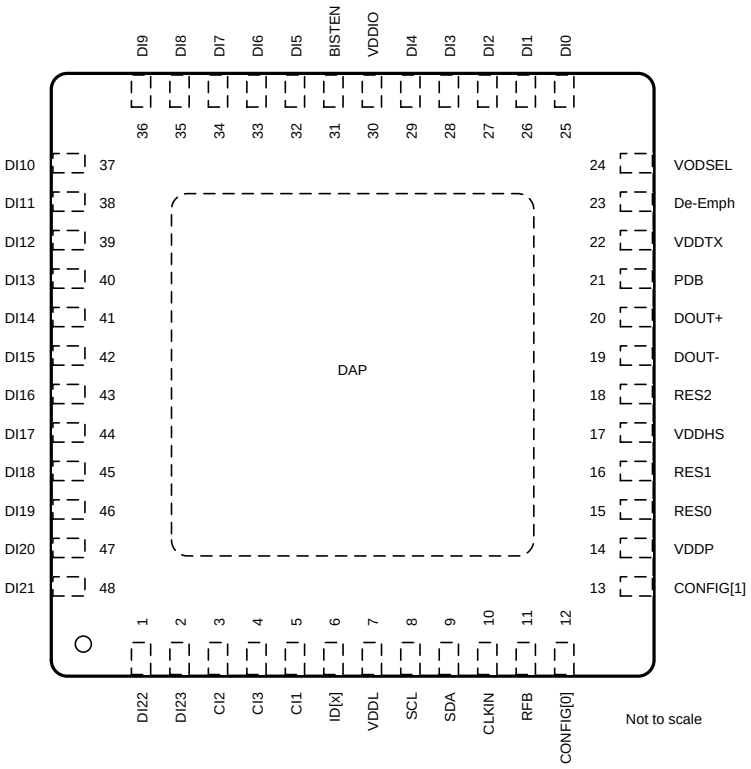
- Changed bit description to swap definition for Serializer RFB and VOD 38
- Changed bit definition for Deserializer OSS_SEL 39
- Changed definition from Reserved to MAP_SEL for Deserializer Reg 0x02[5:4] 39

Changes from Revision A (April 2013) to Revision B **Page**

- Changed layout of National Semiconductor Data Sheet to TI format 49

5 Pin Configuration and Functions

RHS Package
48-Pin WQFN
Top View



Pin Functions: DS92LV2421 (Serializer)

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
DI[7:0]	34, 33, 32, 29, 28, 27, 26, 25	I	Parallel interface data input pins, LVCMOS with pulldown. For 8-bit RED display: DI7 = R7 – MSB, DI0 = R0 – LSB.
DI[15:8]	42, 41, 40, 39, 38, 37, 36, 35	I	Parallel interface data input pins, LVCMOS with pulldown. For 8-bit GREEN display: DI15 = G7 – MSB, DI8 = G0 – LSB.
DI[23:16]	2, 1, 48, 47, 46, 45, 44, 43	I	Parallel interface data input pins, LVCMOS with pulldown. For 8-bit BLUE display: DI23 = B7 – MSB, DI16 = B0 – LSB.
CI1	5	I	Control signal input, LVCMOS with pulldown. For display or video application: CI1 = Data enable input. Control signal pulse width must be 3 clocks or longer to be transmitted when the Control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the control signal filter setting.
CI2	3	I	Control signal input, LVCMOS with pulldown. For display or video application: CI2 = Horizontal sync input. Control signal pulse width must be 3 clocks or longer to be transmitted when the control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the control signal filter setting.

(1) G = Ground, I = Input, O = Output, and P = Power
(2) 1= HIGH, 0 = LOW

Pin Functions: DS92LV2421 (Serializer) (continued)

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
CI3	4	I	Control signal input, LVCMOS with pulldown. For display or video application: CI3 = Vertical sync input. CI3 is limited to 1 transition per 130 clock cycles. Thus, the minimum pulse width allowed is 130 clock cycles wide.
CLKIN	10	I	Clock input, LVCMOS with pulldown. Latch or data strobe edge set by RFB pin.
CONTROL AND CONFIGURATION			
PDB	21	I	Power-down mode input, LVCMOS with pulldown. PDB = 1, serializer is enabled (normal operation). Refer to *Power-Up Requirements and PDB Pin*. PDB = 0, serializer is powered down. When the serializer is in the power-down state, the driver outputs (DOUT±) are both logic high, the PLL is shutdown, IDD is minimized. Control Registers are RESET.
VODSEL	24	I	Differential driver output voltage select (this can also be control by I^2C register access), LVCMOS with pulldown. VODSEL = 1, LVDS VOD is ±420 mV, 840 mV_{p-p} (typical) — long cable or de-emphasis apps. VODSEL = 0, LVDS VOD is ±280 mV, 560 mV_{p-p} (typical) — short cable (no de-emphasis), low power mode.
De-Emph	23	I	De-emphasis control (this can also be controlled by I^2C register access), analog with pullup. De-emphasis = open (float) - disabled. To enable de-emphasis, tie a resistor from this pin to GND or control through register (see Table 3).
RFB	11	I	Clock input latch or data strobe edge select (this can also be controlled by I^2C register access), LVCMOS with pulldown. RFB = 1, parallel interface data and control signals are latched on the rising clock edge. RFB = 0, parallel interface data and control signals are latched on the falling clock edge.
CONFIG[1:0]	13, 12	I	LVCMOS with pulldown. 00: Control Signal Filter DISABLED. 01: Control Signal Filter ENABLED. 10: Reverse compatibility mode to interface with the DS90UR124 or DS99R124Q-Q1. 11: Reverse compatibility mode to interface with the DS90C124.
ID[X]	6	I	I^2C serial control bus device ID address select (optional), analog. Resistor to Ground and 10-kΩ pullup to 1.8-V rail (see Table 11).
SCL	8	I	I^2C serial control bus clock input (optional), LVCMOS. SCL requires an external pullup resistor to V_{DDIO}.
SDA	9	I/O	I^2C serial control bus data input or output (optional), LVCMOS (open drain). SDA requires an external pullup resistor V_{DDIO}.
BISTEN	31	I	BIST mode (optional), LVCMOS with pulldown. BISTEN = 0, BIST is disabled (normal operation). BISTEN = 1, BIST is enabled.
RES[2:0]	18, 16, 15	I	Reserved (tie low), LVCMOS with pulldown.
CHANNEL-LINK II – CML SERIAL INTERFACE			
DOUT+	20	O	Noninverting output, CML. The output must be AC-coupled with a 0.1-µF capacitor.
DOUT–	19	O	Inverting output, CML. The output must be AC-coupled with a 0.1-µF capacitor.

Pin Functions: DS92LV2421 (Serializer) (continued)

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
POWER AND GROUND(3)			
VDDL	7	P	Logic power, 1.8 V ± 5%
VDDP	14	P	PLL power, 1.8 V ± 5%
VDDHS	17	P	TX high-speed logic power, 1.8 V ± 5%
VDDTX	22	P	Output driver power, 1.8 V ± 5%
VDDIO	30	P	LVCMOS I/O power, 1.8 V ± 5% or 3.3 V ± 10%
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 9 vias.

(3) The V_{DD} (V_{DDn} and V_{DDIO}) supply ramp must be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms, then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

NKB Package
60-Pin WQFN
Top View

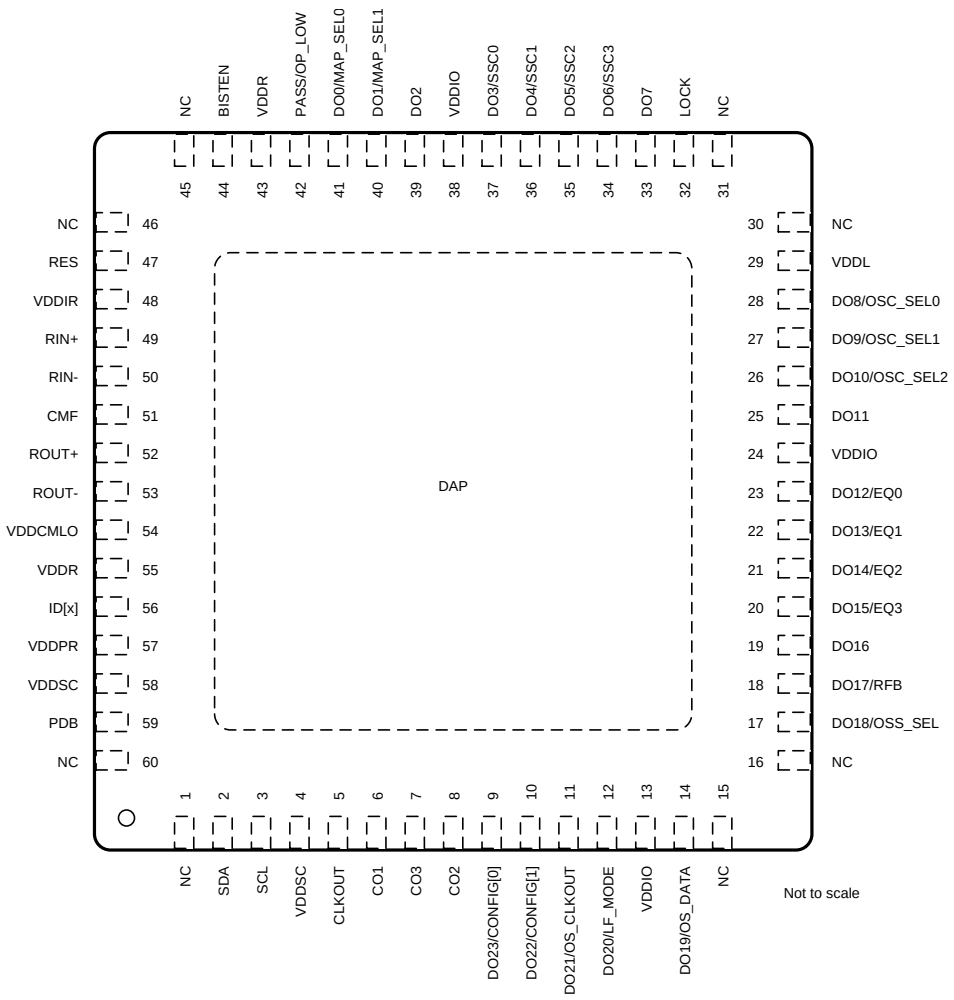


Table 1. Pin Functions: DS92LV2422 (Deserializer)

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
DO[7:0]	33, 34, 35, 36, 37, 39, 40, 41	I/O	Parallel interface data output pins, STRAP and LVCMOS. For 8-bit RED display: DO7 = R7 – MSB, DO0 = R0 – LSB. In power down (PDB = 0), outputs are controlled by the OSS_SEL (see Table 7). These pins are inputs during power-up (see *Deserializer Strap Input Pins*).
DO[15:8]	20, 21, 22, 23, 25, 26, 27, 28	I/O	Parallel interface data output pins, STRAP and LVCMOS. For 8-bit GREEN display: DO15 = G7 – MSB, DO8 = G0 – LSB. In power down (PDB = 0), outputs are controlled by the OSS_SEL (see Table 7). These pins are inputs during power-up (see *Deserializer Strap Input Pins*).
DO[23:16]	9, 10, 11, 12, 14, 17, 18, 19	I/O	Parallel interface data input pins, STRAP and LVCMOS. For 8-bit BLUE display: DO23 = B7 – MSB, DO16 = B0 – LSB. In power down (PDB = 0), outputs are controlled by the OSS_SEL (see Table 7). These pins are inputs during power-up (see *Deserializer Strap Input Pins*).
CO1	6	O	Control signal output, LVCMOS. For display or video application: CO1 = Data enable output. Control signal pulse width must be 3 clocks or longer to be transmitted when the control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the control signal filter setting. In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 7).
CO2	8	O	Control signal output, LVCMOS. For display or video application: CO2 = Horizontal sync output. Control signal pulse width must be 3 clocks or longer to be transmitted when the control signal filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the control signal filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the control signal filter setting. In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 7).
CO3	7	O	Control signal output, LVCMOS. For display or video application: CO3 = Vertical sync output. CO3 is different than CO1 and CO2 because it is limited to 1 transition per 130 clock cycles. Thus, the minimum pulse width allowed is 130 clock cycles wide. The CONFIG[1:0] pins have no effect on the CO3 signal. In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 7).
CLKOUT	5	O	Pixel clock output, LVCMOS. In power down (PDB = 0), output is controlled by the OSS_SEL pin (see Table 7). Data strobe edge set by RFB.
LOCK	32	O	LOCK status output, LVCMOS. LOCK = 1, PLL is locked, outputs are active LOCK = 0, PLL is unlocked, DO[23:0], CO1, CO2, CO3 and CLKOUT output states are controlled by OSS_SEL (see Table 7). May be used as link status or to flag when video data is active (ON/OFF).
PASS	42	O	PASS output (BIST mode), LVCMOS. PASS = 1, error free transmission. PASS = 0, one or more errors were detected in the received payload. Route to test point for monitoring, or leave open if unused.
CONTROL AND CONFIGURATION – STRAP PINS(3)			
CONFIG[1:0]	10 [DO22], 9 [DO23]	I	STRAP or LVCMOS with pulldown. 00: Control Signal Filter DISABLED. 01: Control Signal Filter ENABLED. 10: Reverse compatibility mode to interface with the DS90UR241 or DS99R241-Q1. 11: Reverse compatibility mode to interface with the DS90C241.
LF_MODE	12 [DO20]	I	SSCG low frequency mode, STRAP or LVCMOS with pulldown. Only required when SSCG is enabled, otherwise LF_MODE condition is a DON'T CARE (X). LF_MODE = 1, SSCG in low frequency mode (CLK = 10 to 20 MHz). LF_MODE = 0, SSCG in high frequency mode (CLK = 20 to 65 MHz). This can also be controlled by I^2C register access.

(1) G = Ground, I = Input, O = Output, and P = Power
(2) 1= HIGH, 0 = LOW
(3) For a high state, use a 10-kΩ pullup to V_{DDIO}; for a low state, the IO includes an internal pull down. The strap pins are read upon power-up and set device configuration. Pin number DO[23:0] listed along with shared data output name in square brackets.

Table 1. Pin Functions: DS92LV2422 (Deserializer) (continued)

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
OS_CLKOUT	11 [DO21]	I	Output CLKOUT slew select, STRAP or LVCMOS with pulldown. OS_CLKOUT = 1, increased CLKOUT slew rate. OS_CLKOUT = 0, normal CLKOUT slew rate (default). This can also be controlled by I^2C register access.
OS_DATA	14 [DO19]	I	Output DO[23:0], CO1, CO2, CO3 slew select; STRAP or LVCMOS with pulldown. OS_DATA = 1, Increased DO slew rate. OS_DATA = 0, Normal DO slew rate (default). This can also be controlled by I^2C register access.
OP_LOW	42 [PASS]	I	Outputs held low when LOCK = 1, STRAP or LVCMOS with pulldown. NOTE: Do not use any other strap options with this strap function enabled. OP_LOW = 1, all outputs are held low during power up until released by programming OP_LOW release/set register HIGH. NOTE: Before the device is powered up, the outputs are in TRI-STATE (see Figure 30 and Figure 31). OP_LOW = 0, all outputs toggle normally as soon as LOCK goes high (default). This can also be controlled by I^2C register access.
OSS_SEL	17 [DO18]	I	Output sleep state select, STRAP or LVCMOS with pulldown. OSS_SEL is used in conjunction with PDB to determine the state of the outputs in power down (see Table 7). NOTE: OSS_SEL strap cannot be used if OP_LOW = 1. This can also be controlled by I^2C register access.
RFB	18 [DO17]	I	Clock output strobe edge select, STRAP or LVCMOS with pulldown. RFB = 1, parallel interface data and control signals are strobed on the rising clock edge. RFB = 0, parallel interface data and control signals are strobed on the falling clock edge. This can also be controlled by I^2C register access.
EQ[3:0]	20 [DO15], 21 [DO14], 22 [DO13], 23 [DO12]	I	Receiver input equalization, STRAP or LVCMOS with pulldown (see Table 4). This can also be controlled by I^2C register access.
OSC_SEL[2:0]	26 [DO10], 27 [DO9], 28 [DO8]	I	Oscillator select, STRAP or LVCMOS with pulldown (see Table 8 and Table 9). This can also be controlled by I^2C register access.
SSC[3:0]	34 [DO6], 35 [DO5], 36 [DO4], 37 [DO3]	I	Spread spectrum clock generation (SSCG) range select, STRAP or LVCMOS with pulldown (see Table 5 and Table 6). This can also be controlled by I^2C register access.
MAP_SEL[1:0]	40 [D], 41 [D]	I	Bit mapping reverse compatibility or DS90UR241 options, STRAP or LVCMOS with pulldown. Pin or register control. Default setting is 00'b (see Table 10).
CONTROL AND CONFIGURATION			
PDB	59	I	Power-down mode input, LVCMOS with pulldown. PDB = 1, deserializer is enabled (normal operation). Refer to *Power-Up Requirements and PDB Pin*. PDB = 0, deserializer is in power down. When the deserializer is in the power-down state, the LVCMOS output state is determined by Table 7. Control registers are RESET.
ID[X]	56	I	I^2C serial control bus device ID Address Select (optional), analog. Resistor to ground and 10-kΩ pullup to 1.8-V rail (see Table 11).
SCL	3	I	I^2C serial control bus clock input (optional), LVCMOS. SCL requires an external pullup resistor to V_{DDIO}.
SDA	2	I/O	I^2C serial control bus data input or output (optional), LVCMOS open drain. SDA requires an external pullup resistor to V_{DDIO}.
BISTEN	44	I	BIST enable input (optional), LVCMOS with pulldown. BISTEN = 0, BIST is disabled (normal operation). BISTEN = 1, BIST is enabled.
RES	47	I	Reserved (tie low), LVCMOS with pulldown.
NC	1, 15, 16, 30, 31, 45, 46, 60	—	Not connected, leave pin open (float).

Table 1. Pin Functions: DS92LV2422 (Deserializer) (continued)

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
CHANNEL-LINK II — CML SERIAL INTERFACE			
RIN+	49	I	True input, CML. The input must be AC-coupled with a 0.1-μF capacitor.
RIN-	50	I	Inverting input, CML. The input must be AC-coupled with a 0.1-μF capacitor.
CMF	51	I	Common-mode filter, analog. VCM center-tap is a virtual ground which may be AC-coupled to ground to increase receiver common mode noise immunity. Recommended value is 4.7 μF or higher.
ROUT+	52	O	True output (receive signal after the equalizer), CML. NC if not used or connect to test point for monitor. Requires I^2C control to enable.
ROUT-	53	O	Inverting output (receive signal after the equalizer), CML. NC if not used or connect to test point for monitor. Requires I^2C control to enable.
POWER AND GROUND(4)			
VDDL	29	P	Logic power, 1.8 V ± 5%
VDDIR	48	P	Input power, 1.8 V ± 5%
VDDR	43, 55	P	RX high-speed logic power, 1.8 V ± 5%
VDDSC	4, 58	P	SSCG power, 1.8 V ± 5%
VDDPR	57	P	PLL power, 1.8 V ± 5%
VDDCMLO	54	P	RX high-speed logic power, 1.8 V ± 5%
VDDIO	13, 24, 38	P	LVCMOS I/O power, 1.8 V ± 5% or 3.3 V ± 10% (V_{DDIO})
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 9 vias.

(4) The V_{DD} (V_{DDn} and V_{DDIO}) supply ramp must be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms, then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply voltage, V_{DDn} (1.8 V)		–0.3	2.5	V
Supply voltage, V_{DDIO}		–0.3	4	V
LVCMOS I/O voltage		–0.3	VDDIO + 0.3	V
Receiver input voltage		–0.3	VDD + 0.3	V
Driver output voltage		–0.3	VDD + 0.3	V
48L RHS package	Maximum power dissipation capacity at 25°C		225	mW
	Derate above 25°C		1 / $R_{\theta JA}$	mW/°C
60L NKB package	Maximum power dissipation capacity at 25°C		525	mW
	Derate above 25°C		1 / $R_{\theta JA}$	mW/°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For soldering specifications, see product folder at www.ti.com and SNOA549.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±8000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
	Machine model (MM)		±250	
	IEC 61000-4-2 contact discharge	D_{OUT+}, D_{OUT-}	≥±8000	
		R_{IN+}, R_{IN-}	≥±8000	
	IEC 61000-4-2 air-gap discharge	D_{OUT+}, D_{OUT-}	≥±25000	
		R_{IN+}, R_{IN-}	≥±25000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DDn}	Supply voltage	1.71	1.8	1.89	V
V_{DDIO}	LVCMOS supply voltage	1.71	1.8	1.89	V
V_{DDIO}	LVCMOS supply voltage	3	3.3	3.6	V
	Clock frequency	10		75	MHz
	Supply noise(1)			50	mV_{p-p}
T_A	Operating free-air temperature	–40	25	85	°C

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC-coupled to the V_{DDn} (1.8 V) supply with amplitude = 100 mV_{p-p} measured at the device V_{DDn} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency on the serializer is less than 750 kHz. The deserializer, on the other hand, shows no error when the noise frequency is less than 400 kHz.

6.4 Thermal Information

Over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		DS92LV2421 RHS (WQFN) 48 PINS	DS92LV2422 NKB (WQFN) 60 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	30.3	26.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(2)	11.5	9.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.3	6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Based on nine thermal vias.

6.5 Electrical Characteristics – Serializer DC

Over recommended operating supply and temperature ranges (unless otherwise noted).(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS INPUT DC SPECIFICATIONS							
V_{IH}	High level input voltage	V_{DDIO} = 3 V to 3.6 V (DI[23:0], CI1,CI2,CI3, CLKIN, PDB, VODSEL, RFB, BISTEN, and CONFIG[1:0] pins)		2.2		V_{DDIO}	V
		V_{DDIO} = 1.71 V to 1.89 V (DI[23:0], CI1,CI2,CI3, CLKIN, PDB, VODSEL, RFB, BISTEN, and CONFIG[1:0] pins)		0.65 × V_{DDIO}		V_{DDIO}	
V_{IL}	Low level input voltage	V_{DDIO} = 3 V to 3.6 V (DI[23:0], CI1,CI2,CI3, CLKIN, PDB, VODSEL, RFB, BISTEN, and CONFIG[1:0] pins)		GND		0.8	V
		V_{DDIO} = 1.71 V to 1.89 V (DI[23:0], CI1,CI2,CI3, CLKIN, PDB, VODSEL, RFB, BISTEN, and CONFIG[1:0] pins)		GND		0.35 × V_{DDIO}	
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO} (DI[23:0], CI1,CI2,CI3, CLKIN, PDB, VODSEL, RFB, BISTEN, and CONFIG[1:0] pins)	V_{DDIO} = 3 V to 3.6 V	–15	±1	15	µA
			V_{DDIO} = 1.7 V to 1.89 V	–15	±1	15	
CML DRIVER DC SPECIFICATIONS							
V_{OD}	Differential output voltage	R_L = 100 Ω, de-emphasis = disabled (see Figure 2; DOUT+ and DOUT– pins)	VODSEL = 0	±205	±280	±355	mV
			VODSEL = 1	±320	±420	±520	
VOD_{p-p}	Differential output voltage (DOUT+) – (DOUT-)	R_L = 100 Ω, de-emphasis = disabled (see Figure 2; DOUT+ and DOUT– pins)	VODSEL = 0		560		mV_{p-p}
			VODSEL = 1		840		
ΔV_{OD}	Output voltage unbalance	R_L = 100 Ω, de-emphasis = disabled, VODSEL = L (DOUT+ and DOUT– pins)			1	50	mV
V_{OS}	Offset voltage (single-ended)	At TP A and B (see Figure 1), R_L = 100 Ω, de-emphasis = disabled (DOUT+ and DOUT– pins)	VODSEL = 0		1.65		V
			VODSEL = 1		1.575		
ΔV_{OS}	Offset voltage unbalance (single-ended)	At TP A and B (see Figure 1), R_L = 100 Ω, de-emphasis = disabled (DOUT+ and DOUT– pins)			1		mV
I_{OS}	Output short circuit current	DOUT± = 0 V, de-emphasis = disabled, VODSEL = 0 (DOUT+ and DOUT– pins)			–36		mA
R_{TO}	Internal output termination resistor	DOUT+ and DOUT– pins		80	100	120	Ω

(1) The electrical characteristics tables list verified specifications under the listed recommended operating conditions except as otherwise modified or specified by the electrical characteristics conditions or notes. Typical specifications are estimations only and are not verified.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = 25°C, and at the recommended operation conditions at the time of product characterization and are not verified.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH}, and V_{TL}, which are differential voltages.

Electrical Characteristics – Serializer DC (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted).(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{DDT1}	Serializer supply current (includes load current)	R_L = 100 Ω, CLKIN = 75 MHz, checker board pattern, de-emphasis = 3 kΩ, VODSEL = H (see Figure 9)	V_{DD} = 1.89 V		75	90	mA
			V_{DDIO} = 1.89 V		3	5	
I_{DDIOT1}			V_{DDIO} = 3.6 V		11	15	
I_{DDT2}	Serializer supply current (includes load current)	R_L = 100 Ω, CLKIN = 75 MHz, checker board pattern, de-emphasis = 6 kΩ, VODSEL = L (see Figure 9)	V_{DD} = 1.89 V		65	80	mA
			V_{DDIO} = 1.89 V		3	5	
I_{DDIOT2}			V_{DDIO} = 3.6 V		11	15	
I_{DDZ}	Serializer supply current power-down	PDB = 0 V, All other LVCMOS Inputs = 0 V	V_{DD} = 1.89 V		40	1000	µA
			V_{DDIO} = 1.89 V		5	10	
I_{DDIOZ}			V_{DDIO} = 3.6 V		10	20	

6.6 Electrical Characteristics – Deserializer DC

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3-V I/O LVCMOS DC SPECIFICATIONS (V_{DDIO} = 3 V TO 3.6 V)						
V_{IH}	High level input voltage	PDB and BISTEN pins	2.2		V_{DDIO}	V
V_{IL}	Low level input voltage	PDB and BISTEN pins	GND		0.8	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO} (PDB and BISTEN pins)	−15	±1	15	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA, OS_CLKOUT/DATA = L (DO[23:0], CO1, CO2, CO3, CLKOUT, LOCK, and PASS pins)	2.4	V_{DDIO}		V
V_{OL}	Low level output voltage	I_{OL} = 3 mA, OS_CLKOUT/DATA = L (DO[23:0], CO1, CO2, CO3, CLKOUT, LOCK, and PASS pins)		GND	0.4	V
I_{OS}	Output short circuit current	V_{DDIO} = 3.3 V, V_{OUT} = 0 V, OS_CLKOUT/DATA = L/H (CLKOUT pin)		36		mA
	Output short circuit current	V_{DDIO} = 3.3 V, V_{OUT} = 0 V, OS_CLKOUT/DATA = L/H (output pins)		37		
I_{OZ}	TRI-STATE output current	PDB = 0 V, OSS_SEL = 0 V, V_{OUT} = H (output pins)	−15		15	µA
1.8-V I/O LVCMOS DC SPECIFICATIONS (V_{DDIO} = 1.71 V to 1.89 V)						
V_{IH}	High level input voltage	PDB and BISTEN pins	1.235		V_{DDIO}	V
V_{IL}	Low level input voltage	PDB and BISTEN pins	GND		0.595	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO} (PDB and BISTEN pins)	−15	±1	15	µA
V_{OH}	High level output voltage	I_{OH} = –2 mA, OS_CLKOUT/DATA = L/H (DO[23:0], CO1, CO2, CO3, CLKOUT, LOCK, and PASS pins)	V_{DDIO} – 0.45	V_{DDIO}		V
V_{OL}	Low level output voltage	I_{OL} = 2 mA, OS_CLKOUT/DATA = L/H (DO[23:0], CO1, CO2, CO3, CLKOUT, LOCK, and PASS pins)	GND		0.45	V
I_{OS}	Output short circuit current	V_{DDIO} = 1.8 V, V_{OUT} = 0 V, OS_CLKOUT/DATA = L/H (CLKOUT pin)		18		mA
	Output short circuit current	V_{DDIO} = 1.8 V, V_{OUT} = 0 V, OS_CLKOUT/DATA = L/H (output pins)		18		
I_{OZ}	TRI-STATE output current	PDB = 0 V, OSS_SEL = 0 V, V_{OUT} = 0 V or V_{DDIO} (output pins)	–15		15	µA
CML RECEIVER DC SPECIFICATIONS						
V_{TH}	Differential input threshold high voltage	V_{CM} = 1.2 V, RIN+ and RIN- pins (Internal V_{BIAS})	50			mV
V_{TL}	Differential input threshold low voltage	V_{CM} = 1.2 V, RIN+ and RIN- pins (Internal V_{BIAS})	–50			mV
V_{CM}	Common mode voltage	RIN+ and RIN- pins (Internal V_{BIAS})		1.2		V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO}, RIN+ and RIN- pins	–15		15	µA
R_{TI}	Internal input termination resistor	RIN+ and RIN- pins	80	100	120	Ω
LOOP THROUGH CML DRIVER OUTPUT DC SPECIFICATIONS (EQ TEST PORT(1))						
V_{OD}	Differential output voltage	ROUT+ and ROUT- pins, R_L = 100 Ω		542		mV
V_{OS}	Offset voltage (single-ended)	ROUT+ and ROUT- pins, R_L = 100 Ω		1.4		V

(1) Specification is verified by characterization and is not tested in production.

Electrical Characteristics – Deserializer DC (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_T	Internal termination resistor	ROUT+ and ROUT- pins		80	100	120	Ω
SUPPLY CURRENT							
I_{DD1}	Deserializer supply current (includes load current)	CLKOUT = 75 MHz, checker board pattern, OS_CLKOUT/DATA = H, C_L = 4 pF (see Figure 9)	V_{DD} = 1.89 V		97	115	mA
I_{DDIO1}			V_{DDIO} = 1.89 V		40	50	
			V_{DDIO} = 3.6 V		75	85	
I_{DDZ}	Deserializer supply current power down	PDB = 0 V, All other LVCMOS Inputs = 0 V	V_{DD} = 1.89 V		100	3000	µA
I_{DDIOZ}			V_{DDIO} = 1.89 V		6	50	
			V_{DDIO} = 3.6 V		12	100	

6.7 Electrical Characteristics – DC and AC Serial Control Bus

Over 3.3-V supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high level	SDA and SCL	2.2		V_{DDIO}	V
V_{IL}	Input low level voltage	SDA and SCL	GND		0.8	V
V_{HY}	Input hysteresis			>50		mV
V_{OL}	Output low level voltage(1)	SDA, I_{OL} = 1.25 mA, V_{DDIO} = 3.3 V	0		0.4	V
I_{in}	Input current	SDA or SCL, Vin = V_{DDIO} or GND	–15		15	µA
C_{in}	Input capacitance	SDA or SCL		<5		pF

(1) Specification is verified by characterization and is not tested in production.

6.8 Timing Requirements – DC and AC Serial Control Bus

Over 3.3-V supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	SDA rise time (read)	SDA, RPU = 10 kΩ, Cb ≤ 400 pF		40		ns
t_F	SDA fall time (read)	SDA, RPU = 10 kΩ, Cb ≤ 400 pF		25		ns
$t_{SU;DAT}$	Set up time (read)			520		ns
$t_{HD;DAT}$	Hold up time (read)			55		ns
t_{SP}	Input filter			50		ns

6.9 Timing Requirements – Serializer for CLKIN

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{TCP}	Transmit input CLKIN period	10 MHz to 75 MHz (see Figure 4)	13.3	T	100	ns
t_{TCIH}	Transmit input CLKIN high time	10 MHz to 75 MHz (see Figure 4)	0.4 × T	0.5 × T	0.6 × T	ns
t_{TCIL}	Transmit input CLKIN low time	10 MHz to 75 MHz (see Figure 4)	0.4 × T	0.5 × T	0.6 × T	ns
t_{CLKT}	CLKIN input transition time	10 MHz to 75 MHz (see Figure 4)	0.5		2.4	ns
SSC_{IN}	CLKIN input	fmod (spread spectrum at 75 MHz)			35	kHz
		fdev (spread spectrum at 75 MHz)			±2%	

6.10 Timing Requirements – Serial Control Bus

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	
t_{LOW}	SCL low period	Standard mode	4.7			µs
		Fast mode	1.3			
t_{HIGH}	SCL high period	Standard mode	4			µs
		Fast mode	0.6			
$t_{HD;STA}$	Hold time for a start or a repeated start condition (see Figure 18)	Standard mode	4			µs
		Fast mode	0.6			
$t_{SU:STA}$	Set up time for a start or a repeated start condition (see Figure 18)	Standard mode	4.7			µs
		Fast mode	0.6			
$t_{HD;DAT}$	Data hold time (see Figure 18)	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
$t_{SU;DAT}$	Data set up time (see Figure 18)	Standard mode	250			ns
		Fast mode	100			
$t_{SU;STO}$	Set up time for STOP condition (see Figure 18)	Standard mode	4			µs
		Fast mode	0.6			
t_{BUF}	Bus free time (between STOP and START; see Figure 18)	Standard mode	4.7			µs
		Fast mode	1.3			
t_r	SCL and SDA rise time (see Figure 18)	Standard mode			1000	ns
		Fast mode			300	
t_f	SCL and SDA fall time (see Figure 18)	Standard mode			300	ns
		Fast mode			300	

6.11 Switching Characteristics – Serializer

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LHT}	Serializer output low-to-high transition time (see Figure 3)	R_L = 100 Ω, de-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100 Ω, de-emphasis = disabled, VODSEL = 1		200		
t_{HLT}	Serializer output high-to-low transition time (see Figure 3)	R_L = 100 Ω, de-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100 Ω, de-emphasis = disabled, VODSEL = 1		200		
t_{DIS}	Input data, setup time (see Figure 4)	DI[23:0], CI1, CI2, CI3 to CLKIN	2			ns
t_{DIH}	Input data, hold time (see Figure 4)	CLKIN to DI[23:0], CI1, CI2, CI3	2			ns
t_{XZD}	Serializer output active to OFF delay (see Figure 6)(1)			8	15	ns
t_{PLD}	Serializer PLL lock time (see Figure 5)(1)(2)(3)	R_L = 100 Ω		1.4	10	ms
t_{SD}	Serializer delay, latency (see Figure 7)(1)	R_L = 100 Ω		144 × T	145 × T	ns

(1) Specification is verified by characterization and is not tested in production.
(2) t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer, respectively, to obtain lock when exiting power-down state with an active clock.
(3) When the serializer output is at TRI-STATE the Deserializer loses PLL lock. Resynchronization and Re-lock must occur before data transfer require t_{PLD}

Switching Characteristics – Serializer (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DJIT}	Serializer output total jitter (see Figure 8)	R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 75 MHz		0.28		UI(4)
		R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 43 MHz		0.27		
		R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 10 MHz		0.35		
λ_{STXBW}	Serializer jitter transfer (function –3 dB bandwidth)	R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 75 MHz		3.3		MHz
		R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 43 MHz		2.3		
		R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 10 MHz		0.8		
δ_{STX}	Serializer jitter transfer (function peaking)	R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 75 MHz		0.86		dB
		R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 43 MHz		0.83		
		R_L = 100 Ω, de-emphasis = disabled, RANDOM pattern, CLKIN = 10 MHz		0.28		

(4) UI – Unit Interval is equivalent to one serialized data bit width (1 UI = 1 / [28 x CLK]). The UI scales with clock frequency.

6.12 Switching Characteristics – Deserializer

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{RCP}	CLK output period	t_{RCP} = t_{TCP} (CLKOUT)		13.3	T	100	ns
t_{RDC}	CLK output duty cycle	CLKOUT	SSCG = OFF, 10 to 75 MHz	40%	50%	60%	
			SSCG = ON, 10 to 20 MHz	35%	59%	65%	
			SSCG = ON, 10 to 65 MHz	40%	53%	60%	
t_{CLH}	LVCMOS low-to-high transition time (see Figure 10)	DO[23:0], CO1, CO2, CO3	V_{DDIO} = 1.8 V, C_L = 4 pF, OS_CLKOUT/DATA = L		2.1		ns
			V_{DDIO} = 3.3 V, C_L = 4 pF, OS_CLKOUT/DATA = H		2		
t_{CHL}	LVCMOS high-to-low transition time (see Figure 10)	DO[23:0], CO1, CO2, CO3	V_{DDIO} = 1.8 V, C_L = 4 pF, OS_CLKOUT/DATA = L		1.6		ns
			V_{DDIO} = 3.3 V, C_L = 4 pF, OS_CLKOUT/DATA = H		1.5		
t_{ROS}	Data valid before CLKOUT, setup time (see Figure 14)	V_{DDIO} = 1.71 to 1.89 V or 3 to 3.6 V, C_L = 4 pF (lumped load), DO[23:0], CO1, CO2, CO3		0.23 × T	0.5 × T		ns
t_{ROH}	Data valid after CLKOUT, hold time (see Figure 14)	V_{DDIO} = 1.71 to 1.89 V or 3 to 3.6 V, C_L = 4 pF (lumped load), DO[23:0], CO1, CO2, CO3		0.33 × T	0.5 × T		ns
t_{DDLT}	Deserializer lock time (see Figure 13)	CLKOUT = 10 MHz, SSC[3:0] = OFF(1)			3		ms
		CLKOUT = 75 MHz, SSC[3:0] = OFF(1)			4		
		CLKOUT = 10 MHz, SSC[3:0] = ON(1)			30		
		CLKOUT = 65 MHz, SSC[3:0] = ON(1)			6		
t_{DD}	Deserializer delay, latency (see Figure 11)	CLKOUT = 10 to 75 MHz, SSC[3:0] = OFF(2)			139 × T	140 × T	ns

(1) t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer, respectively, to obtain lock when exiting power-down state with an active clock.
(2) Specification is verified by design and is not tested in production.

Switching Characteristics – Deserializer (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DPJ}	Deserializer period jitter	SSC[3:0] = OFF (3) (2)	CLKOUT = 10 MHz		500	1000	ps
			CLKOUT = 65 MHz		550	1250	
			CLKOUT = 75 MHz		435	900	
t_{DCCJ}	Deserializer cycle-to-cycle jitter	SSC[3:0] = OFF (4) (2) (5)	CLKOUT = 10 MHz		375	900	ps
			CLKOUT = 65 MHz		500	1150	
			CLKOUT = 75 MHz		460	1000	
t_{IJT}	Deserializer input jitter tolerance (see Figure 16)	EQ = OFF, SSCG = OFF, CLKOUT = 75 MHz	jitter freq < 2 MHz		0.9		UI (6)
			jitter freq > 6 MHz		0.5		
BIST MODE							
t_{PASS}	BIST PASS valid time (see Figure 17)	BISTEN = 1			1	10	µs
SSCG MODE							
f_{DEV}	Spread spectrum clocking deviation frequency	CLKOUT = 10 to 65 MHz, SSC[3:0] = ON		±0.5%		±2%	
f_{MOD}	Spread spectrum clocking modulation frequency	CLKOUT = 10 to 65 MHz, SSC[3:0] = ON		8		100	kHz

(3) t_{DPJ} is the maximum amount the period is allowed to deviate over many samples.
(4) Specification is verified by characterization and is not tested in production.
(5) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.
(6) UI – Unit Interval is equivalent to one serialized data bit width (1 UI = 1 / [28 x CLK]). The UI scales with clock frequency.

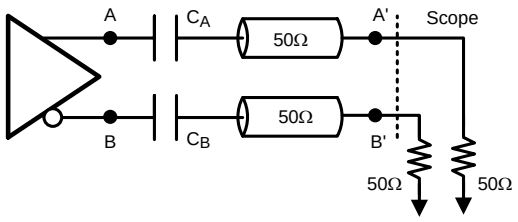


Figure 1. Serializer Test Circuit

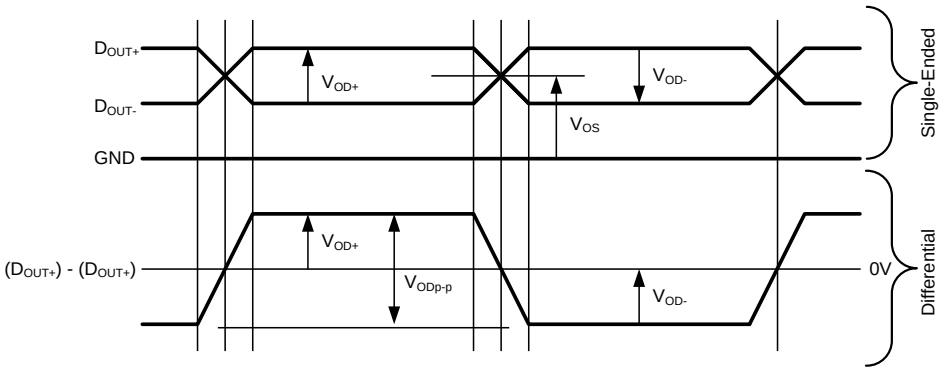


Figure 2. Serializer Output Waveforms

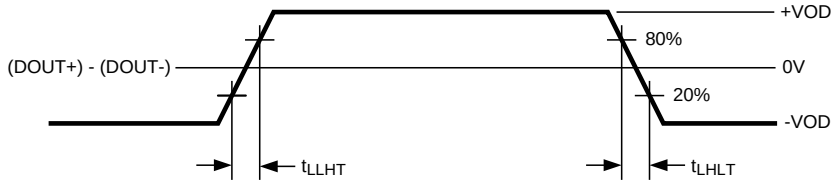


Figure 3. Serializer Output Transition Times

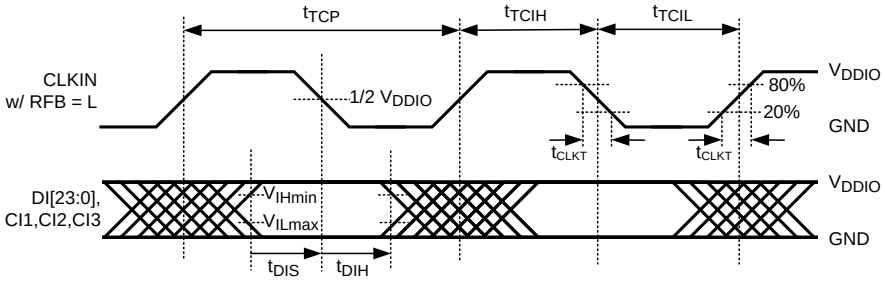


Figure 4. Serializer Input CLKIN Waveform and Set and Hold Times

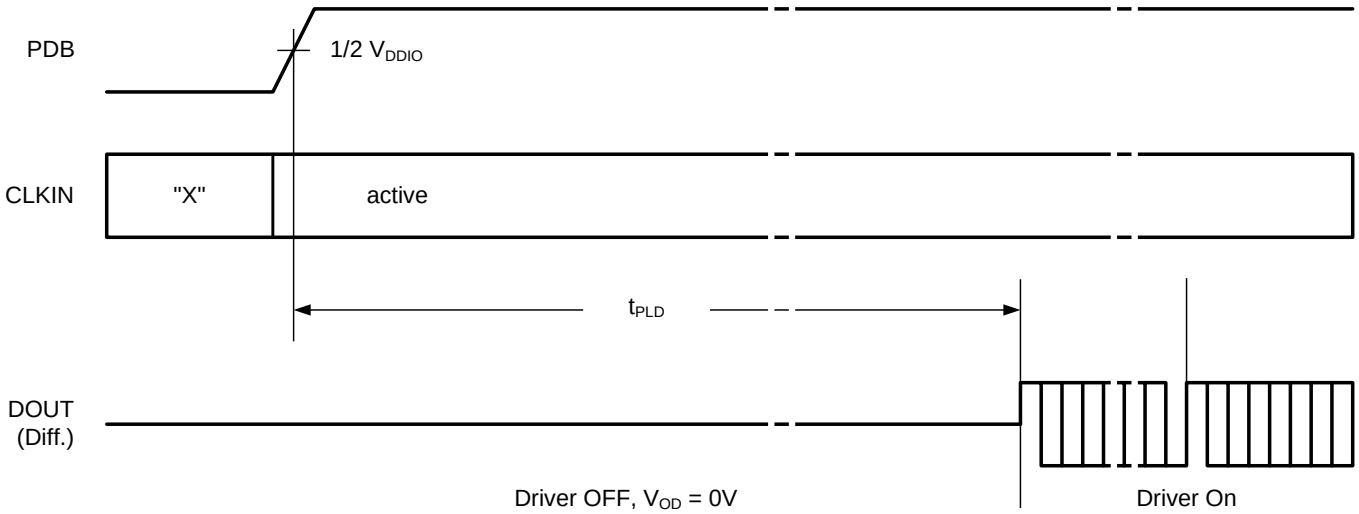


Figure 5. Serializer Lock Time

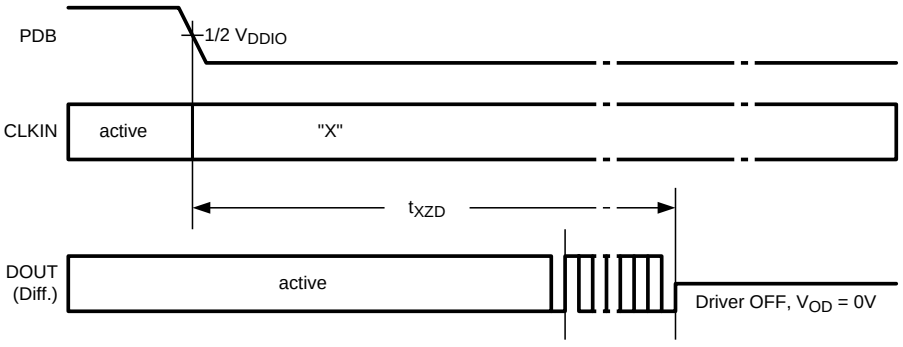


Figure 6. Serializer Disable Time

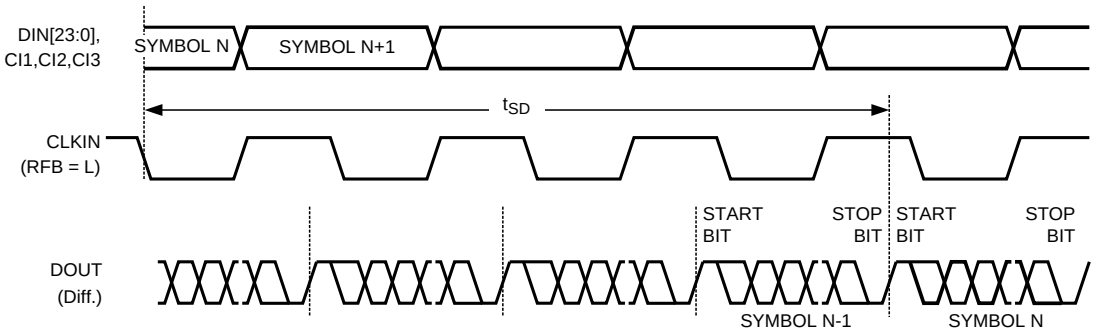


Figure 7. Serializer Latency Delay

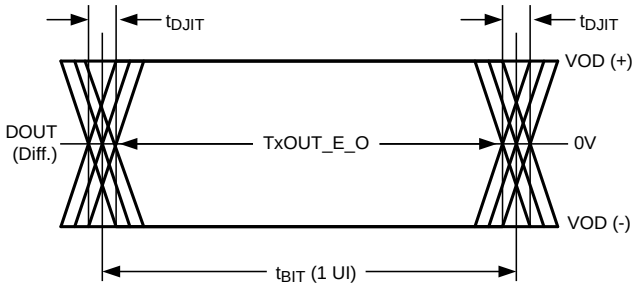


Figure 8. Serializer Output Jitter

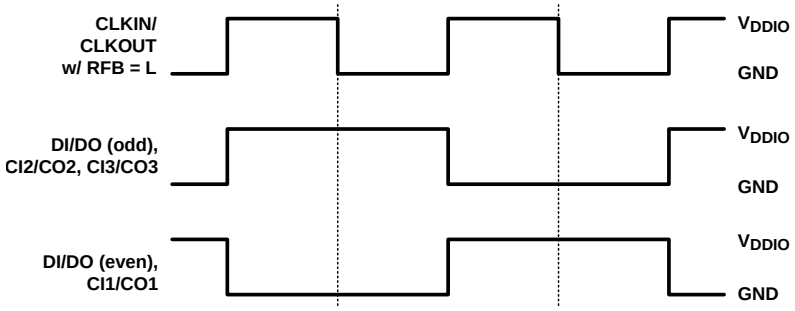


Figure 9. Checkerboard Data Pattern

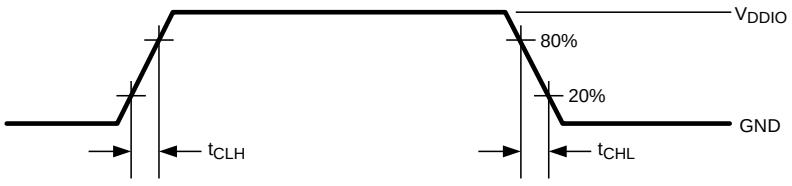


Figure 10. Deserializer LVCMOS Transition Times

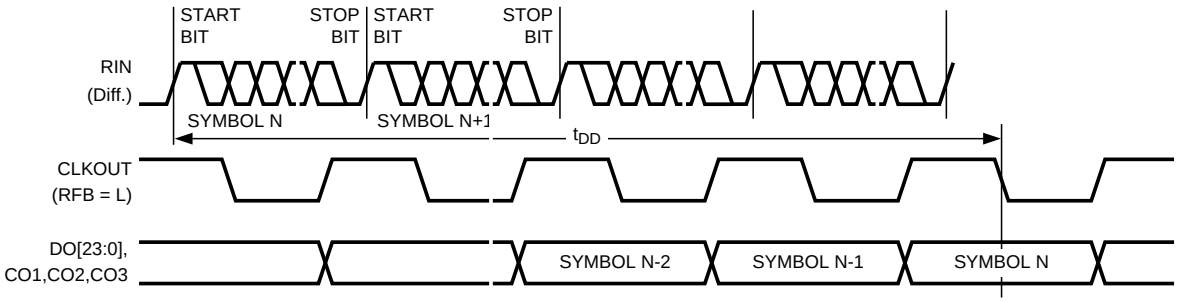


Figure 11. Deserializer Delay – Latency

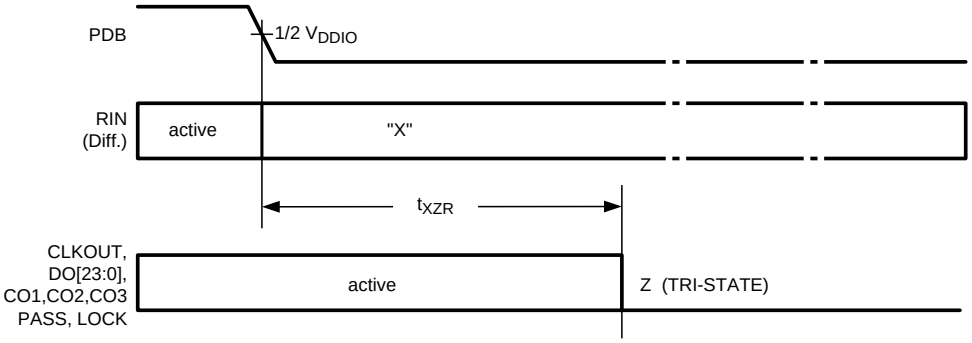


Figure 12. Deserializer Disable Time (OSS_SEL = 0)

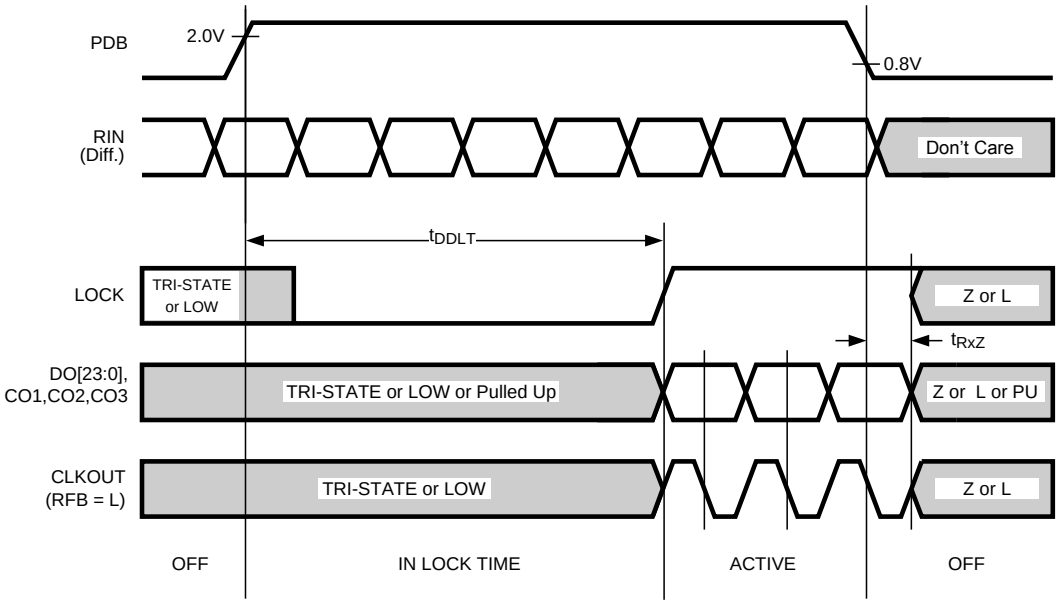


Figure 13. Deserializer PLL Lock Times and PDB Tri-State Delay

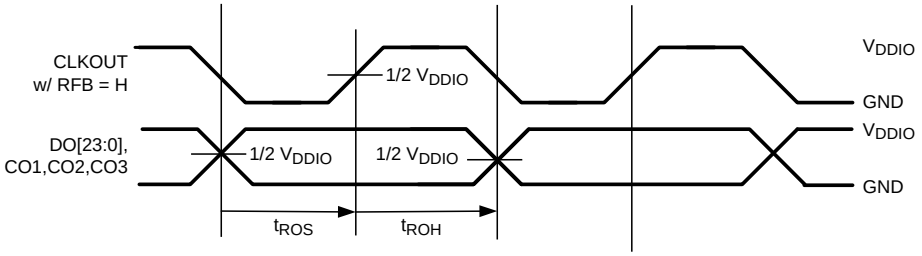


Figure 14. Deserializer Output Data Valid (Setup and Hold) Times With SSCG = Off

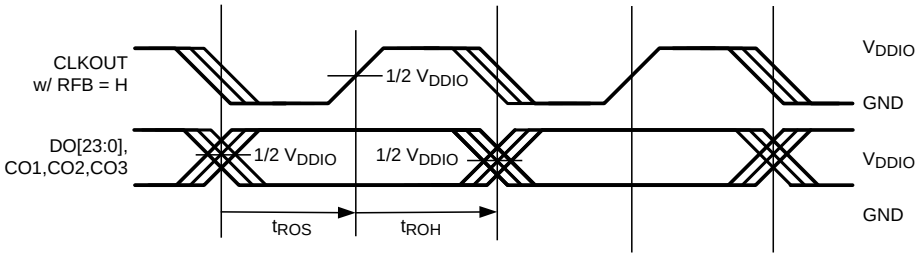
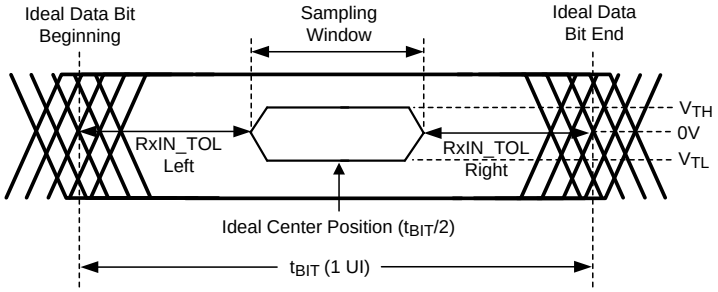


Figure 15. Deserializer Output Data Valid (Setup And Hold) Times With SSCG = On



t_{RJIT} = RxIN_TOL (Left + Right)

Sampling Window = 1 UI - t_{RJIT}

Figure 16. Receiver Input Jitter Tolerance

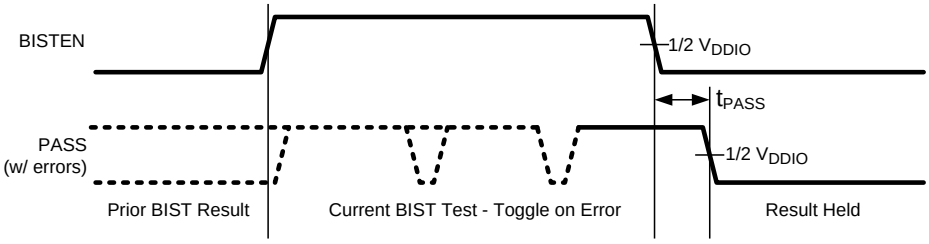


Figure 17. BIST Pass Waveform

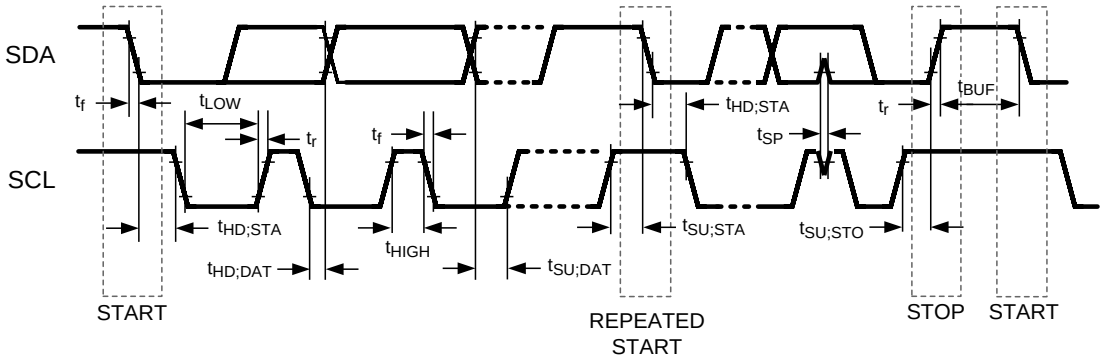


Figure 18. Serial Control Bus Timing Diagram

6.13 Typical Characteristics

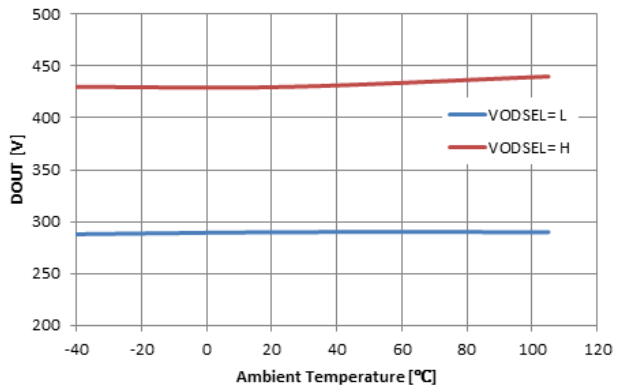


Figure 19. Differential Output Voltage vs Ambient Temperature

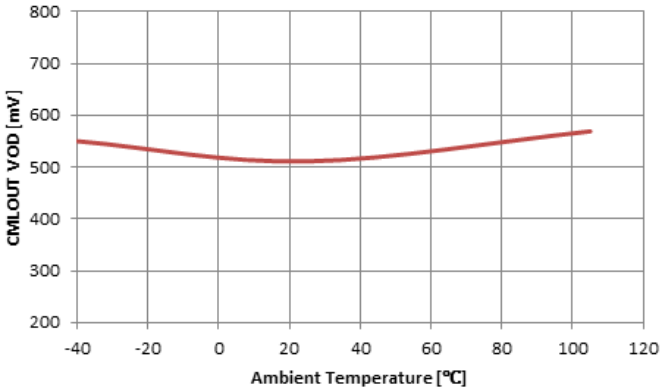


Figure 20. ROUT (CMLOUT) VOD vs Ambient Temperature

7 Detailed Description

7.1 Overview

The DS92LV242x chipset transmits and receives 24 bits of data and 3 control signals over a single serial CML pair operating at 280 Mbps to 2.1 Gbps. The serial stream also contains an embedded clock, video control signals, and the DC-balance information which enhances signal quality and supports AC coupling.

The deserializer can attain lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic *plug and lock* performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating, and then deserializing the incoming data stream, providing a parallel LVCMOS video bus to the display, ASIC, or FPGA.

The DS92LV242x chipset can operate in 24-bit color depth (with DE, HS, VS encoded within the serial data stream). In 18-bit color applications, the three video control signals may be sent encoded within the serial bit stream (restrictions apply, see *Video Control Signal Filter – Serializer and Deserializer*) along with six additional general-purpose signals.

7.2 Functional Block Diagrams

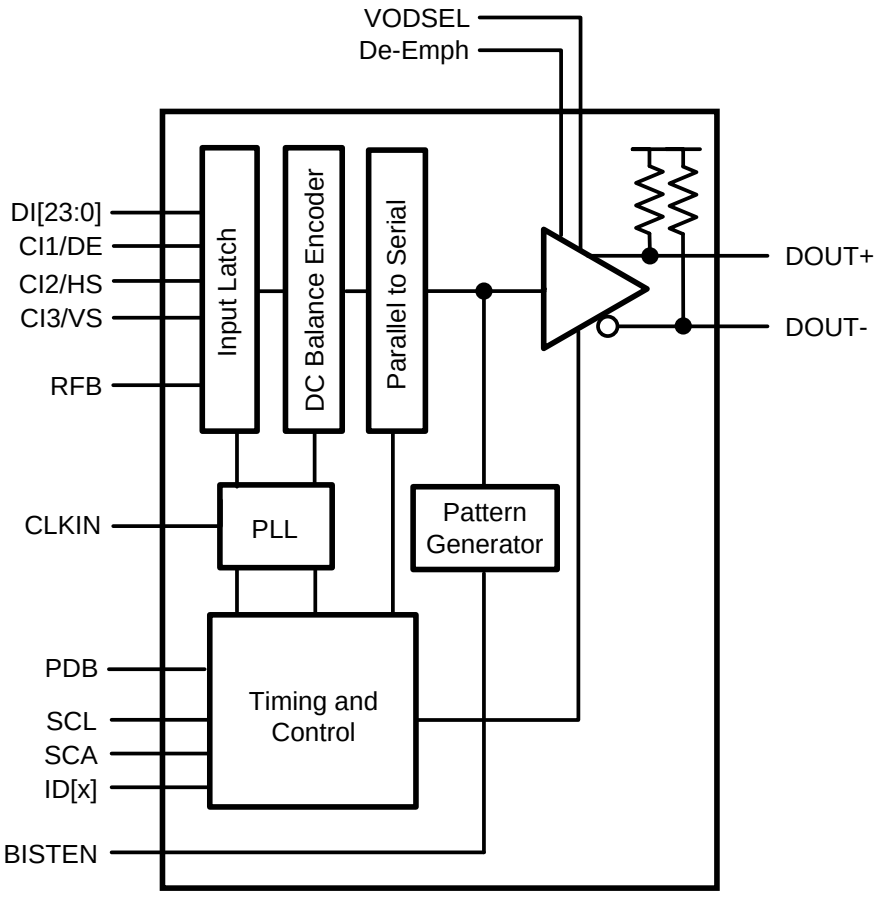


Figure 21. DS92LV2421 – Serializer

Functional Block Diagrams (continued)

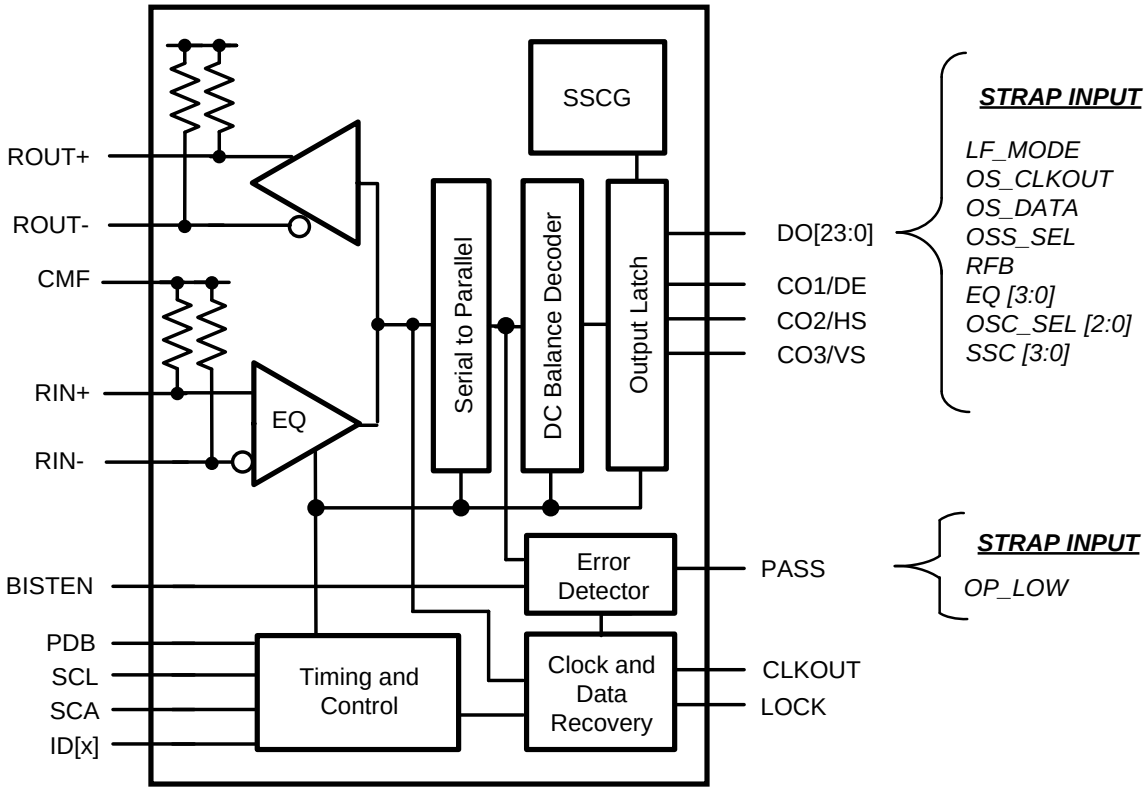


Figure 22. DS92LV2422 – Deserializer

7.3 Feature Description

7.3.1 Data Transfer

The DS92LV242x chipset transmits and receives a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always high and C0 is always low. The b[23:0] contains the scrambled LVCMOS data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream and can also contain encoded control (VS, HS, DE). Both DCA and DCB coding schemes are generated by the serializer and decoded by the deserializer automatically. Figure 23 illustrates the serial stream per clock cycle.

NOTE

Figure 23 only illustrates the bits but does not actually represent the bit location as the bits are scrambled and balanced continuously.

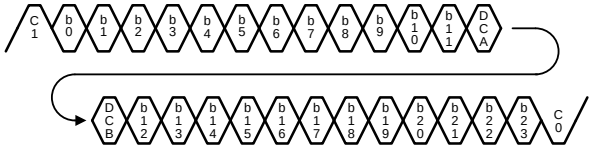


Figure 23. Channel Link II Serial Stream (DS92LV242x)

Feature Description (continued)

7.3.2 Video Control Signal Filter – Serializer and Deserializer

When operating the devices in normal mode, the video control signals (DE, HS, VS) have the following restrictions:

- Normal mode with control signal filter enabled:
  - DE and HS: Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 CLK cycles or longer.
- Normal mode with control signal filter disabled:
  - DE and HS: Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS: Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video control signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals (see Figure 24).

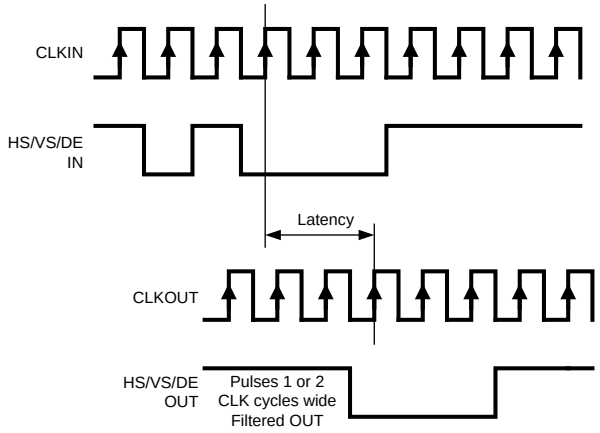


Figure 24. Video Control Signal Filter Waveform

7.3.3 Serializer Functional Description

The serializer converts a wide parallel input bus to a single serial output data stream and also acts as a signal generator for the chipset Built In Self Test (BIST) mode. The device can be configured through external pins or through the optional serial control bus. The serializer features enhance signal quality on the link by supporting: a selectable VOD level, a selectable de-emphasis signal conditioning, and Channel Link II data coding that provides randomization, scrambling, and DC balancing of the data. The serializer includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and system spread spectrum clock support. The serializer features power-saving features with a sleep mode, auto stop clock feature, and optional LVCMOS (1.8 V) parallel bus compatibility (see also *Optional Serial Bus Control* and *Built-In Self Test (BIST)*).

7.3.3.1 EMI Reduction Features

7.3.3.1.1 Data Randomization and Scrambling

Channel Link II serializers and deserializers feature a three-step encoding process that enables the use of AC-coupled interconnects and also helps to manage EMI. The serializer first passes the parallel data through a scrambler which randomizes the data. The randomized data is then DC-balanced. The DC-balanced and randomized data then goes through a bit-shuffling circuit and is transmitted out on the serial line. This encoding process helps to prevent static data patterns on the serial stream. The resulting frequency content of the serial stream ranges from the parallel clock frequency to the serial Nyquist rate. For example, if the serializer and deserializer chip set is operating at a parallel clock frequency of 75 MHz, the resulting frequency content of serial stream ranges from 75 MHz to 1.05 GHz (75 MHz × 28 bits / 2 = 2.1 GHz / 2 = 1.05 GHz).

Feature Description (continued)

7.3.3.1.2 Serializer Spread Spectrum Compatibility

The serializer CLKIN is capable of tracking spread spectrum clocking (SSC) from a host source. The CLKIN accepts spread spectrum tracking up to 35-kHz modulation and ±0.5, ±1, or ±2% deviations (center spread). The maximum conditions for the CLKIN input are: a modulation frequency of 35 kHz and amplitude deviations of ±2% (4% total).

7.3.3.2 Signal Quality Enhancers

7.3.3.2.1 Serializer VOD Select (VODSEL)

The serializer differential output voltage may be increased by setting the VODSEL pin high. When VODSEL is low, the DC VOD is at the standard (default) level. When VODSEL is high, the VOD is increased in level. The increased VOD is useful in extremely high noise environments and also on extra long cable length applications. When using de-emphasis, TI recommends setting VODSEL = H to avoid excessive signal attenuation, especially with the larger de-emphasis settings. This feature may be controlled by the external pin or by register.

Table 2. Differential Output Voltage

INPUT	EFFECT	
VODSEL	VOD (mV)	VOD (mV_{p-p})
H	±420	840
L	±280	560

7.3.3.2.2 Serializer De-Emphasis (De-Emph)

The de-emphasis pin controls the amount of de-emphasis beginning one full bit time after a logic transition that the serializer drives. This is useful to counteract loading effects of long or lossy cables. This pin must be left open for standard switching currents (no de-emphasis) or if controlled by register. De-emphasis is selected by connecting a resistor on this pin to ground, with R value between 0.5 kΩ to 1 MΩ, or by register setting. When using de-emphasis, TI recommends to set VODSEL = H.

Table 3. De-Emphasis Resistor Value

RESISTOR VALUE (kΩ)	DE-EMPHASIS SETTING
Open	Disabled
0.6	–12 dB
1	–9 dB
2	–6 dB
5	–3 dB

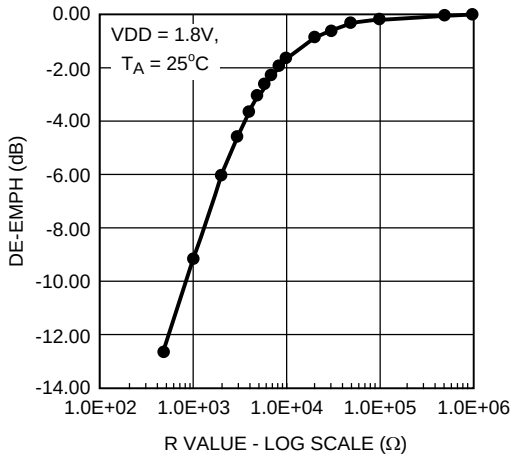


Figure 25. De-Emphasis vs R Value

7.3.3.3 Power-Saving Features

7.3.3.3.1 Serializer Power-Down Feature (PDB)

The serializer has a PDB input pin to enable or power down the device. This pin is controlled by the host and is used to save power, disabling the link when it is not needed. In power-down mode, the high-speed driver outputs are both pulled to VDD and present a 0-V VOD state.

NOTE

In power down, the optional serial bus control registers are RESET.

7.3.3.3.2 Serializer Stop Clock Feature

The serializer enters a low power SLEEP state when the CLKIN is stopped. A STOP condition is detected when the input clock frequency is less than 3 MHz. The clock must be held at a static low or high state. When the CLKIN starts again, the serializer locks to the valid input clock and then transmits the serial data to the deserializer.

NOTE

In STOP CLOCK SLEEP, the optional serial bus control register values are RETAINED.

7.3.3.3.3 1.8-V or 3.3-V VDDIO Operation

The serializer parallel bus and serial bus interface can operate with 1.8-V or 3.3-V levels (V_{DDIO}) for host compatibility. The 1.8-V levels offer lower noise (EMI) and also system power savings.

7.3.3.3.4 Deserializer Power-Down Feature (PDB)

The deserializer has a PDB input pin to enable or power down the device. This pin can be controlled by the system to save power, disabling the deserializer when the display is not needed. An auto-detect mode is also available. In this mode, the PDB pin is tied high and the deserializer enters power down when the serial stream stops. When the serial stream starts up again, the deserializer locks to the input stream and assert the LOCK pin and output valid data. In power-down mode, the data and CLKOUT output states are determined by the OSS_SEL status.

NOTE

In power down, the optional serial bus control registers are RESET.

7.3.3.3.5 Deserializer Stop Stream SLEEP Feature

The deserializer enters a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the deserializer then locks to the incoming signal and recover the data.

NOTE

In STOP STREAM SLEEP, the optional serial bus control registers values are RETAINED.

7.3.3.4 Serializer Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the data is latched on. If RFB is high, input data is latched on the rising edge of the CLKIN. If RFB is low, input data is latched on the falling edge of the CLKIN. Serializer and deserializer may be set differently. This feature may be controlled by the external pin or by register.

7.3.3.5 Optional Serial Bus Control

See *Optional Serial Bus Control*.

7.3.3.6 Optional BIST Mode

See *Built-In Self Test (BIST)*.

7.3.4 Deserializer Functional Description

The deserializer converts a single input serial data stream to a wide parallel output bus and also provides a signal check for the chipset Built-In Self Test (BIST) mode. The device can be configured through external pins and strap pins or through the optional serial control bus. The deserializer features enhance signal quality on the link by supporting an equalizer input and Channel Link II data coding that provides randomization, scrambling, and DC balancing of the data. The deserializer includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and output spread spectrum clock generation (SSCG) support. The deserializer features power-saving features with a power-down mode and optional LVCMOS (1.8 V) interface compatibility.

7.3.4.1 Signal Quality Enhancers

7.3.4.1.1 Deserializer Input Equalizer Gain (EQ)

The deserializer can enable receiver input equalization of the serial stream to increase the eye opening to the deserializer input.

NOTE

This function cannot be seen at the RxIN± input but can be observed at the serial test port (ROUT±) enabled through the serial bus control registers. The equalization feature may be controlled by the external pin or by register.

Table 4. Receiver Equalization Configuration Table

INPUTS				EFFECT
EQ3	EQ2	EQ1	EQ0	
L	L	L	H	≈1.5 dB
L	L	H	H	≈3 dB
L	H	L	H	≈4.5 dB
L	H	H	H	≈6 dB
H	L	L	H	≈7.5 dB
H	L	H	H	≈9 dB
H	H	L	H	≈10.5 dB
H	H	H	H	≈12 dB
X	X	X	L	OFF (1)

(1) Default Setting is EQ = Off

7.3.4.2 EMI Reduction Features

7.3.4.2.1 Deserializer Output Slew Rate Select (OS_CLKOUT/OS_DATA)

The parallel bus outputs (DO[23:0], CO[3:1], and CLKOUT) of the deserializer feature a selectable output slew. The DATA (DO[23:0], CO[3:1]) are controlled by strap pin or register bit OS_DATA. The CLKOUT is controlled by strap pin or register bit OS_CLKOUT. When the OS_CLKOUT/DATA = H, the maximum slew rate is selected. When the OS_PCLK/DATA = L, the minimum slew rate is selected. Use the higher slew rate setting when driving longer traces or a heavier capacitive load.

7.3.4.2.2 Deserializer Common-Mode Filter Pin (CMF) (Optional)

The deserializer provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high-noise environments for additional noise rejection capability. A 4.7-µF capacitor may be connected from this pin to Ground.

7.3.4.2.3 Deserializer SSCG Generation (Optional)

The deserializer provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This aids to lower system EMI. Output SSCG deviations of ±2% (4% total) at up to 100-kHz modulations are available (see Table 5). This feature may be controlled by external strap pins or by register.

NOTE

The device supports SSCG function with CLKOUT = 10 MHz to 65 MHz. When the CLKOUT = 65 MHz to 75 MHz, it is required to disable the SSCG function (SSC[3:0] = 0000).

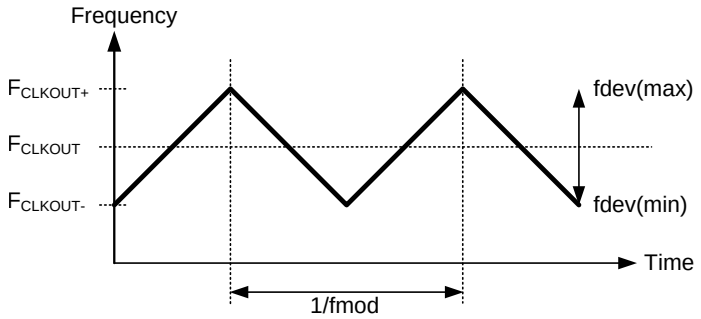


Figure 26. SSCG Waveform

Table 5. SSCG Configuration (LF_MODE = L) – Deserializer Output

SSC[3:0] INPUTS LF_MODE = L (20 - 65 MHz)				RESULT	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	CLK/2168
L	L	H	L	±1	
L	L	H	H	±1.5	
L	H	L	L	±2	
L	H	L	H	±0.5	CLK/1300
L	H	H	L	±1	
L	H	H	H	±1.5	
H	L	L	L	±2	
H	L	L	H	±0.5	CLK/868
H	L	H	L	±1	
H	L	H	H	±1.5	
H	H	L	L	±2	
H	H	L	H	±0.5	CLK/650
H	H	H	L	±1	
H	H	H	H	±1.5	

Table 6. SSCG Configuration (LF_MODE = H) – Deserializer Output

SSC[3:0] INPUTS LF_MODE = H (10 - 20 MHz)				RESULT	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	CLK/620
L	L	H	L	±1	
L	L	H	H	±1.5	
L	H	L	L	±2	
L	H	L	H	±0.5	CLK/370
L	H	H	L	±1	
L	H	H	H	±1.5	
H	L	L	L	±2	
H	L	L	H	±0.5	CLK/258
H	L	H	L	±1	
H	L	H	H	±1.5	
H	H	L	L	±2	
H	H	L	H	±0.5	CLK/192
H	H	H	L	±1	
H	H	H	H	±1.5	

7.3.4.2.4 1.8-V or 3.3-V VDDIO Operation

The deserializer parallel bus and serial bus interface can operate with 1.8-V or 3.3-V levels (V_{DDIO}) for target (display) compatibility. The 1.8-V levels offer a lower noise (EMI) and also system power savings.

7.3.4.3 Deserializer Clock-Data Recovery Status Flag (LOCK) And Output State Select (OSS_SEL)

When PDB is driven high, the CDR PLL begins locking to the serial input and LOCK goes from TRI-STATE to low (depending on the value of the OSS_SEL setting). After the DS92LV2422 completes its lock sequence to the input serial data, the LOCK output is driven high, indicating valid data and clock recovered from the serial input is available on the parallel bus and clock outputs. The CLKOUT output is held at its current state at the change from OSC_CLK (if this is enabled through OSC_SEL) to the recovered clock (or vice versa).

If there is a loss of clock from the input serial stream, LOCK is driven low and the state of the outputs are based on the OSS_SEL setting (strap pin configuration or register).

7.3.4.4 Deserializer Oscillator Output (Optional)

The deserializer provides an optional clock output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin or by register (see Table 8 and Table 9).

Table 7. OSS_SEL and PDB Configuration (Deserializer Outputs)

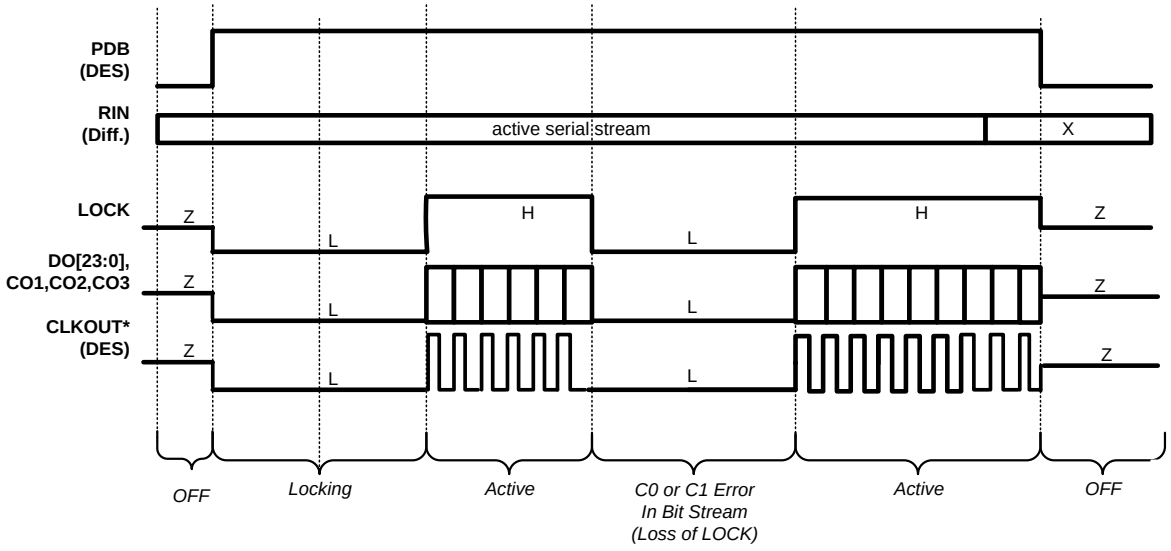
INPUTS			OUTPUTS			
SERIAL INPUT	PDB	OSS_SEL	CLKOUT	DO[23:0], CO1, CO2, CO3	LOCK	PASS
X	L	L	Z	Z	Z	Z
X	L	H	Z	Z	Z	Z
Static	H	L	L	L	L	L
Static	H	H	Z	Z(1)	L	L
Active	H	X	Active	Active	H	H

(1) If DO[23:0], CO[3:1] pin is strapped high, the output is pulled up.

Table 8. OSC (Oscillator) Mode — Deserializer Output

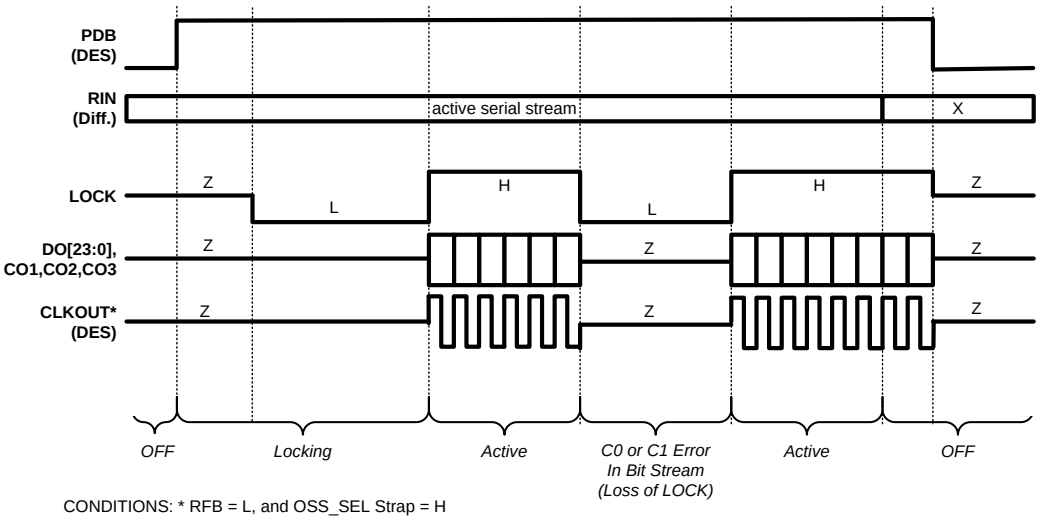
INPUTS	OUTPUTS			
EMBEDDED CLK	CLKOUT	DO[23:0], CO1, CO2, CO3	LOCK	PASS
See (1)	OSC Output	L	L	H
Present	Toggling	Active	H	H

(1) Absent and OSC_SEL ≠ 000.



CONDITIONS: * RFB = L, and OSS_SEL Strap = L

Figure 27. Deserializer Outputs With Output State Select Low (OSS_SEL = L)



CONDITIONS: * RFB = L, and OSS_SEL Strap = H

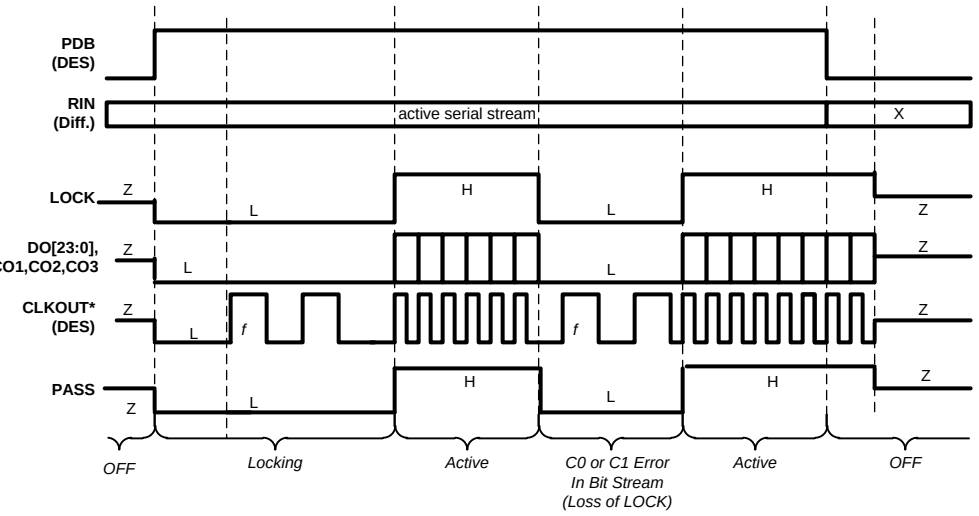
Figure 28. Deserializer Outputs With Output State Select High (OSS_SEL = H)

Table 9. OSC_SEL (Oscillator) Configuration

OSC_SEL[2:0] INPUTS			CLKOUT OSCILLATOR FREQUENCY
OSC_SEL2	OSC_SEL1	OSC_SEL0	
L	L	L	Off – Feature Disabled – Default

Table 9. OSC_SEL (Oscillator) Configuration (continued)

OSC_SEL[2:0] INPUTS			CLKOUT OSCILLATOR FREQUENCY
OSC_SEL2	OSC_SEL1	OSC_SEL0	
L	L	H	50 MHz ± 40%
L	H	L	25 MHz ± 40%
L	H	H	16.7 MHz ± 40%
H	L	L	12.5 MHz ± 40%
H	L	H	10 MHz ± 40%
H	H	L	8.3 MHz ± 40%
H	H	H	6.3 MHz ± 40%



CONDITIONS: * RFB = L, OSS_SEL = H , and OSC_SEL not equal to 000.

Figure 29. Deserializer Outputs With Output State High and CLKOUT Oscillator Option Enabled

7.3.4.5 Deserializer OP_LOW (Optional)

The OP_LOW feature is used to hold the LVCMOS outputs (except for the LOCK output) at a low state. The user must toggle the OP_LOW set / reset register bit to release the outputs to the normal toggling state.

NOTE

The release of the outputs can only occur when LOCK is high. When the OP_LOW feature is enabled, anytime LOCK = low, the LVCMOS outputs toggle to a low state again. The OP_LOW strap pin feature is assigned to output PASS pin 42.

Restrictions on other straps:

1. Other straps must not be used to keep the data and clock outputs at a true low state. Other features must be selected through I^2C.
2. The OSS_SEL function is not available when OP_LOW is enabled (tied high).

Outputs DO[23:0], CO[3:1], and CLKOUT are in TRI-STATE before PDB toggles high, because the OP_LOW strap value has not been recognized until the DS92LV2422 powers up. Figure 30 shows the user controlled release of OP_LOW and automatic reset of OP_LOW set on the falling edge of LOCK. Figure 31 shows the user controlled release of OP_LOW and manual reset of OP_LOW set.

NOTE

Manual reset of OP_LOW can only occur when LOCK is high.

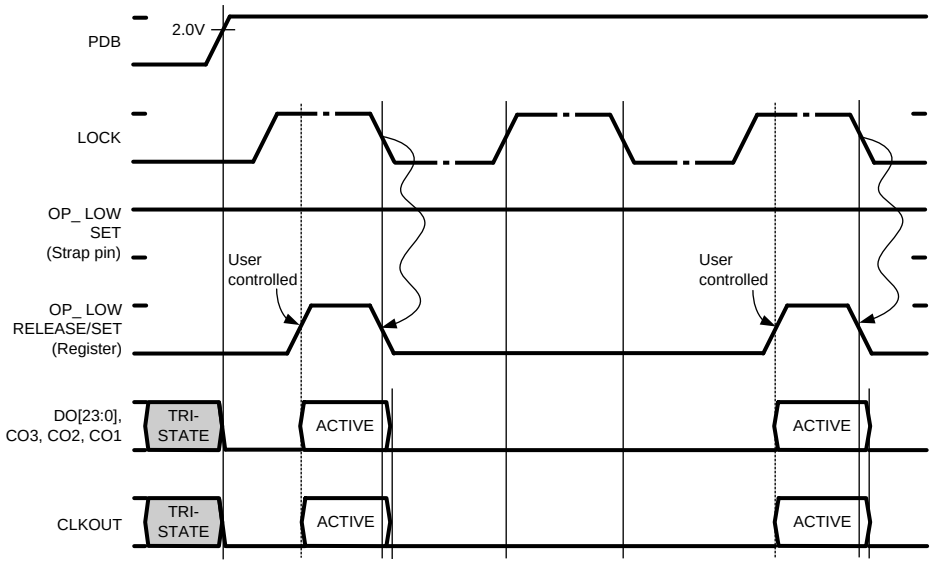


Figure 30. OP_LOW Auto Set

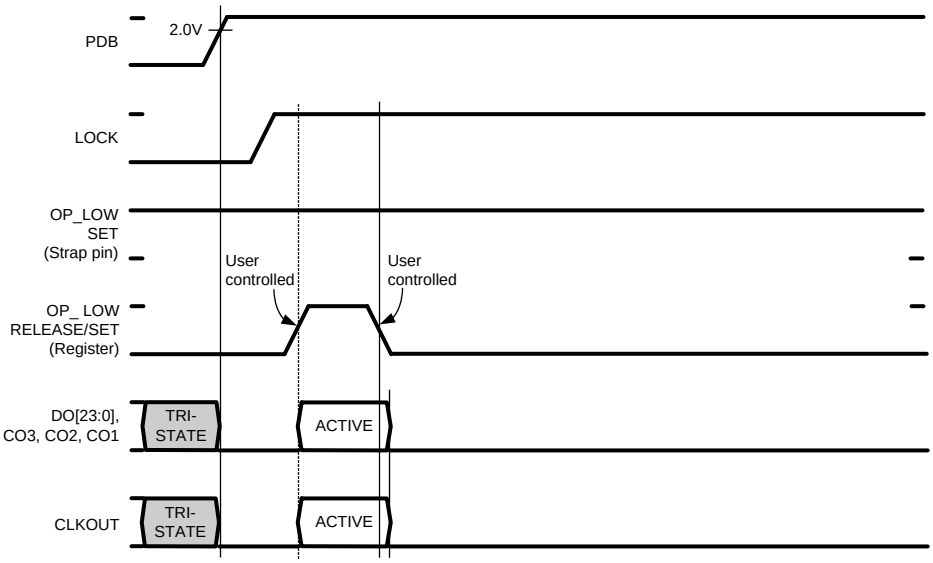


Figure 31. OP_LOW Manual Set or Reset

7.3.4.6 Deserializer Clock Edge Select (RFB)

The RFB pin determines the edge that the data is strobed on. If RFB is high, output data is strobed on the rising edge of CLKOUT. If RFB is low, data is strobed on the falling edge of CLKOUT. This allows for inter-operability with downstream devices. The deserializer output does not need to use the same edge as the serializer input. This feature may be controlled by the external pin or by register.

7.3.4.7 Deserializer Control Signal Filter (Optional)

The deserializer provides an optional control signal (C3, C2, C1) filter that monitors the three control signals and eliminates any pulses or glitches that are 1 or 2 CLKOUT periods wide. Control signals must be 3 parallel clock periods wide (in its high or low state, regardless of which state is active). This is set by the CONFIG[1:0] strap option or by I^2C register control.

7.3.4.8 Deserializer Low Frequency Optimization (LF_Mode)

This feature may be controlled by the external pin or by register.

7.3.4.9 Deserializer Map Select

This feature may be controlled by the external pin or by register.

Table 10. Map Select Configuration

INPUTS		EFFECT
MAP_SEL1	MAP_SEL0	
L	L	Bit 4, Bit 5 on LSB DEFAULT
L	H	LSB 0 or 1
H	H or L	LSB 0

7.3.4.10 Deserializer Strap Input Pins

Configuration of the device may be done through configuration input pins and the strap input pins, or through the serial control bus. The strap input pins share select parallel bus output pins. They are used to load in configuration values during the initial power-up sequence of the device. Only a pullup on the pin is required when a high is desired. By default, the pad has an internal pulldown and bias low by itself. The recommended value of the pullup is 10 kΩ to V_{DDIO}; open (NC) for low, because no pulldown is required (internal pulldown). If using the serial control bus, no pullups are required.

7.3.4.11 Optional Serial Bus Control

See *Optional Serial Bus Control*.

7.3.4.12 Optional BIST Mode

See *Built-In Self Test (BIST)*.

7.3.5 Built-In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test, and for system diagnostics. In BIST mode, only an input clock is required along with control to the serializer and deserializer BISTEN input pins. The serializer outputs a test pattern (PRBS-7) and drives the link at speed. The deserializer detects the PRBS-7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or power down). A high on PASS indicates NO ERRORS were detected. A low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. During the BIST duration, the deserializer data outputs toggle with a checkerboard pattern.

Inter-operability is supported between this Channel Link II device and all Channel Link II generations (Gen 1, 2, 3). See *Sample BIST Sequence* for entering BIST mode and control.

7.3.5.1 Sample BIST Sequence

See Figure 32 for the BIST mode flow diagram.

Step 1: Place the DS92LV2421 serializer in BIST Mode by setting serializer BISTEN = H. For the DS92LV2421 serializer or DS99R421-Q1 FPD-Link II serializer, BIST Mode is enabled through the BISTEN pin. For the DS90C241 serializer or DS90UR241 serializer, BIST mode is entered by setting all the input data of the device to a low state. A CLKIN is required for BIST. When the deserializer detects the BIST mode pattern and command (DCA and DCB code), the data and control signal outputs are shut off.

Step 2: Place the DS92LV2422 deserializer in BIST mode by setting BISTEN = H. The deserializer is now in BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin switches low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To stop BIST mode, the deserializer BISTEN pin is set low. The deserializer stops checking the data, and the final test result is held on the PASS pin. If the test ran error free, the PASS output is high. If there was one or more errors detected, the PASS output is low. The PASS output state is held until a new BIST is run, the device is RESET, or powered down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the serializer BISTEN input is set low. The Link returns to normal operation.

Figure 33 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error-free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission and so forth), thus they may be introduced by greatly extending the cable length, faulting the interconnect, or reducing signal condition enhancements (de-emphasis, VODSEL, or Rx equalization).

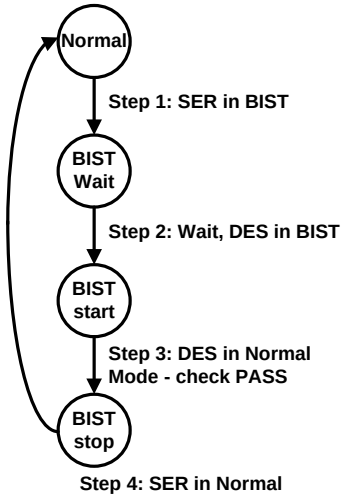


Figure 32. BIST Mode Flow Diagram

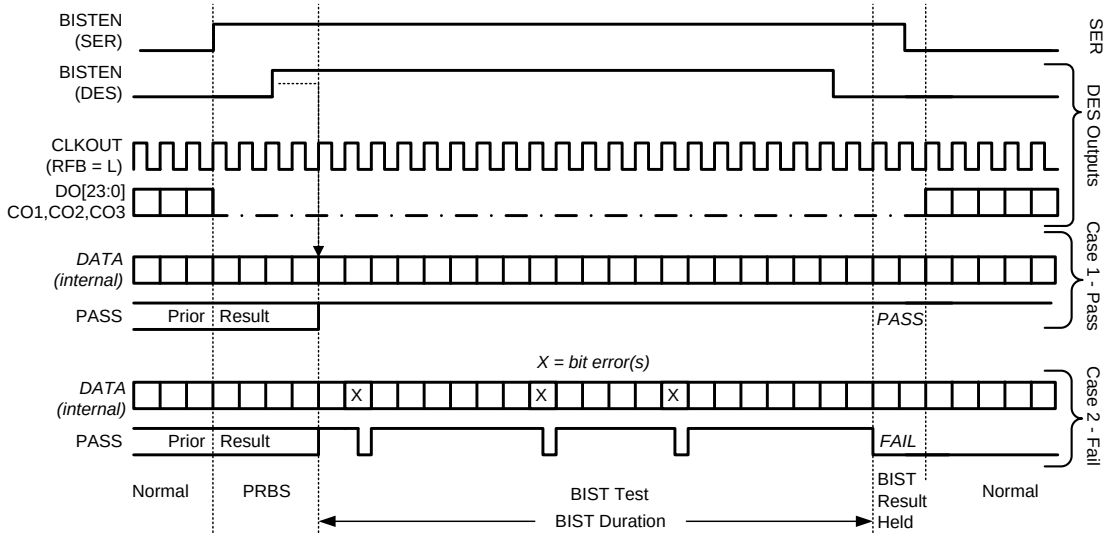


Figure 33. BIST Waveforms

7.3.5.2 BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST Test Result (PASS)

The BER is less than or equal to one over the product of 24 times the CLKOUT rate times the test duration. If we assume a 65-MHz clock, a 10-minute (600 seconds) test, and a PASS, the BER is ≤ 1.07 X 10E-12.

BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. If the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin switches low. The combination of the LOCK and At-Speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

7.3.6 Optional Serial Bus Control

The serializer and deserializer may also be configured by the use of a serial control bus that is I^2C protocol-compatible. By default, the I^2C Reg 0x00 = 0x00, and all configuration is set by control or strap pins. Writing reg 0x00 = 0x01 enables or allows configuration by registers; this overrides the control or strap pins. Multiple devices may share the serial control bus, because multiple addresses are supported (see Figure 34).

The serial bus is comprised of three pins. The SCL is a serial bus clock input. The SDA is the serial bus data input or output signal. Both SCL and SDA signals require an external pullup resistor to V_{DDIO}. For most applications, a 4.7-kΩ pullup resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled high or driven low.

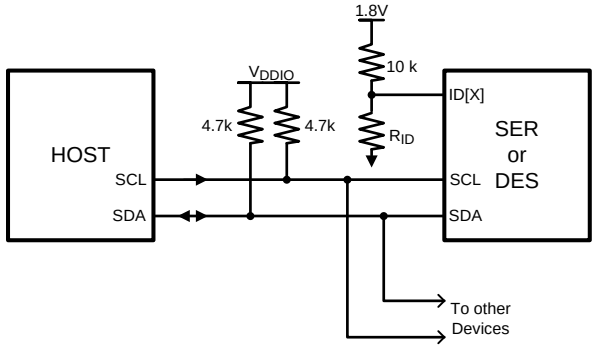


Figure 34. Serial Control Bus Connection

The third pin is the ID[X] pin. This pin sets one of four possible device addresses. Two different connections are possible:

- The pin may be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-kΩ resistor.
- The pin may be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-kΩ resistor and pulled down to ground with a recommended value RID resistor. This creates a voltage divider that sets the other three possible addresses.

See Table 11 for the serializer and Table 12 for the deserializer. Do not tie ID[X] directly to VSS.

Table 11. ID[X] Resistor Value – DS92LV2421 (Serializer)

RESISTOR RID kΩ(1) (5% TOL)	ADDRESS 7'b	ADDRESS 8'b 0 APPENDED (WRITE)
0.47	7b' 110 1001 (h'69)	8b' 1101 0010 (h'D2)
2.7	7b' 110 1010 (h'6A)	8b' 1101 0100 (h'D4)
8.2	7b' 110 1011 (h'6B)	8b' 1101 0110 (h'D6)
Open	7b' 110 1110 (h'6E)	8b' 1101 1100 (h'DC)

(1) RID ≠ 0 Ω. Do not connect directly to VSS (GND). This is not a valid address.

Table 12. ID[X] Resistor Value – DS92LV2422 Deserializer

RESISTOR RID kΩ(1) (5% TOL)	ADDRESS 7'b	ADDRESS 8'b 0 APPENDED (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

(1) RID ≠ 0 Ω. Do not connect directly to VSS (GND). This is not a valid address.

The serial bus protocol is controlled by START, START-repeated, and STOP phases. A START occurs when SCL transitions low while SDA is high. A STOP occurs when SDA transition high while SCL is also high (see Figure 35).

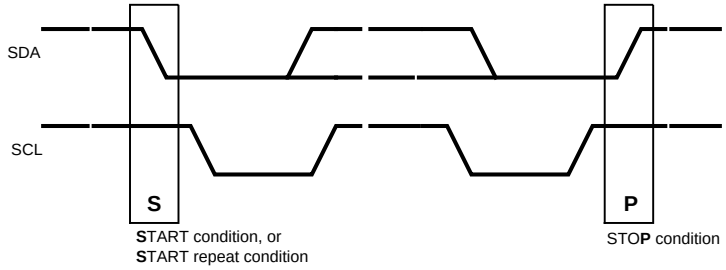


Figure 35. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match the slave address of a device, it Not-acknowledges (NACKs) the master by letting SDA be pulled high. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a start condition or a repeated start condition. All communication on the bus ends with a stop condition. A READ is shown in Figure 36 and a WRITE is shown in Figure 37.

NOTE

During initial power-up, a delay of 10 ms is required before the I^2C will respond.

If the serial bus is not required, the three pins may be left open (NC).

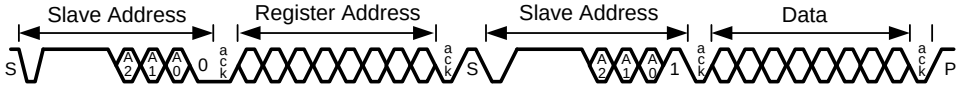


Figure 36. Serial Control Bus — READ

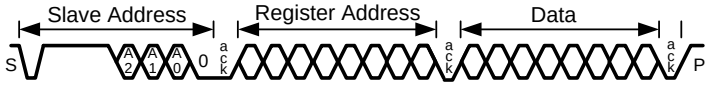


Figure 37. Serial Control Bus — WRITE

7.4 Device Functional Modes

7.4.1 Serializer and Deserializer Operating Modes and Reverse Compatibility (CONFIG[1:0])

The DS92LV242x chipset is compatible with other single serial lane Channel Link II or FPD-Link II devices. Configuration modes are provided for reverse compatibility with the DS90C241 / DS90C124 chipset (FPD-Link II Generation 1) and also the DS90UR241 / DS90UR124 chipset (FPD-Link II Generation 2) by setting the respective mode with the CONFIG[1:0] pins on the serializer or deserializer as shown in Table 13 and Table 14. This selection also determines whether the control signal filter feature is enabled or disabled in the normal mode. This feature may be controlled by pin or by register.

Table 13. DS92LV2421 Serializer Modes

CONFIG1	CONFIG0	MODE	COMPATIBLE DESERIALIZER DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS92LV2422, DS92LV2412, DS92LV0422, DS92LV0412
L	H	Normal Mode, Control Signal Filter enabled	DS92LV2422, DS92LV2412, DS92LV0422, DS92LV0412
H	L	Reverse Compatibility Mode (FPD-Link II, GEN2)	DS90UR124, DS99R124Q-Q1
H	H	Reverse Compatibility Mode (FPD-Link II, GEN1)	DS90C124

Table 14. DS92LV2422 Deserializer Modes

CONFIG1	CONFIG0	MODE	COMPATIBLE SERIALIZER DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS92LV2421, DS92LV2411, DS92LV0421, DS92LV0411
L	H	Normal Mode, Control Signal Filter enabled	DS92LV2421, DS92LV2411, DS92LV0421, DS92LV0411
H	L	Reverse Compatibility Mode (FPD-Link II, GEN2)	DS90UR241, DS99R421-Q1
H	H	Reverse Compatibility Mode (FPD-Link II, GEN1)	DS90C241

7.5 Register Maps

Table 15. SERIALIZER — Serial Bus Control Registers

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
0	0	Serializer Config 1	7	R/W	0	***Reserved***	***Reserved***
			6	R/W	0	***Reserved***	***Reserved***
			5	R/W	0	VODSEL	0: Low 1: High
			4	R/W	0	RFB	0: Data latched on Falling edge of CLKIN 1: Data latched on Rising edge of CLKIN
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: DS90UR124, DS99R124Q-Q1 Reverse-Compatibility Mode (FPD-Link II, GEN2) 11: DS90C124 Reverse-Compatibility Mode (FPD-Link II, GEN1)
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: Normal Mode 1: Sleep Mode – Register settings retained.
			0	R/W	0	REG	0: Configurations set from control pins 1: Configuration set from registers (except I^2C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1101000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1101 001 (h'69) 7b '1101 010 (h'6A) 7b '1101 011 (h'6B) 7b '1101 110 (h'6E) All other addresses are ***reserved***.
2	2	De-Emphasis Control	7:5	R/W	000	De-Emphasis Setting	000: set by external resistor 001: –1 dB 010: –2 dB 011: –3.3 dB 100: –5 dB 101: –6.7 dB 110: –9 dB 111: –12 dB
			4	R/W	0	De-Emphasis EN	0: De-emphasis enabled 1: De-emphasis disabled
			3:0	R/W	000	***Reserved***	***Reserved***

Table 16. DESERIALIZER — Serial Bus Control Registers

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
0	0	Deserializer Config 1	7	R/W	0	LF_MODE	0: 20 to 65 MHz SSCG Operation 1: 10 to 20 MHz SSCG Operation
			6	R/W	0	OS_CLKOUT	0: Normal CLKOUT Slew Rate 1: Increased CLKOUT Slew Rate
			5	R/W	0	OS_DATA	0: Normal DATA Slew Rate 1: Increased DATA Slew Rate
			4	R/W	0	RFB	0: Data strobed on Falling edge of CLKOUT 1: Data strobed on Rising edge of CLKOUT
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: DS90UR241, DS99R241-Q1 Reverse-Compatibility Mode (FPD-Link II, GEN2) 11: DS90C241 Reverse-Compatibility Mode (FPD-Link II, GEN1)
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: Normal Mode 1: Sleep Mode – Register settings retained.
			0	R/W	0	REG Control	0: Configurations set from control pins or strap pins 1: Configurations set from registers (except I^2C_ID)
1	1	Slave ID	7	R/W	0	REG ID	0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1110 001 (h'71) 7b '1110 010 (h'72) 7b '1110 011 (h'73) 7b '1110 110 (h'76) All other addresses are ***Reserved***.
2	2	Deserializer Features 1	7	R/W	0	OP_LOW	0: Set outputs state LOW (except LOCK) 1: Release output LOW state, outputs toggling normally Note: This register only works during LOCK = 1
			6	R/W	0	OSS_SEL	Output Sleep State Select 0: CLKOUT, DO[23:0], CO1, CO2, CO3 = L, LOCK = Normal, PASS = H 1: CLKOUT, DO[23:0], CO1, CO2, CO3 = Tri-State, LOCK = Normal, PASS = H
			5:4	R/W	00	MAP_SEL	Special for Reverse-Compatibility Mode 00: Bit 4, 5 on LSB 01: LSB zero if all data is zero; one if any data is one 10: LSB zero 11: LSB zero
			3	R/W	0	OP_LOW Strap Bypass	0: Strap will determine whether OP_LOW feature is ON or OFF 1: Turns OFF OP_LOW feature
			2:0	R/W	00	OSC_SEL	000: Disable 001: 50 MHz ± 40% 010: 25 MHz ± 40% 011: 16.7 MHz ± 40% 100: 12.5 MHz ± 40% 101: 10 MHz ± 40% 110: 8.3 MHz ± 40% 111: 6.3 MHz ± 40%

Table 16. DESERIALIZER — Serial Bus Control Registers (continued)

ADD (DEC)	ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT (BIN)	FUNCTION	DESCRIPTION
3	3	Deserializer Features 2	7:5	R/W	000	EQ Gain	000: ≈1.625 dB 001: ≈3.25 dB 010: ≈4.87 dB 011: ≈6.5 dB 100: ≈8.125 dB 101: ≈9.75 dB 110: ≈11.375 dB 111: ≈13 dB
			4	R/W	0	EQ Enable	0: EQ = disable 1: EQ = enable
			3:0	R/W	0000	SSC	If LF_MODE = 0, then: 000: SSCG disable 0001: fdev = ±0.5%, fmod = CLK/2168 0010: fdev = ±1.0%, fmod = CLK/2168 0011: fdev = ±1.5%, fmod = CLK/2168 0100: fdev = ±2.0%, fmod = CLK/2168 0101: fdev = ±0.5%, fmod = CLK/1300 0110: fdev = ±1.0%, fmod = CLK/1300 0111: fdev = ±1.5%, fmod = CLK/1300 1000: fdev = ±2.0%, fmod = CLK/1300 1001: fdev = ±0.5%, fmod = CLK/868 1010: fdev = ±1.0%, fmod = CLK/868 1011: fdev = ±1.5%, fmod = CLK/868 1100: fdev = ±2.0%, fmod = CLK/868 1101: fdev = ±0.5%, fmod = CLK/650 1110: fdev = ±1.0%, fmod = CLK/650 1111: fdev = ±1.5%, fmod = CLK/650 If LF_MODE = 1, then: 000: SSCG disable 0001: fdev = ±0.5%, fmod = CLK/620 0010: fdev = ±1.0%, fmod = CLK/620 0011: fdev = ±1.5%, fmod = CLK/620 0100: fdev = ±2.0%, fmod = CLK/620 0101: fdev = ±0.5%, fmod = CLK/370 0110: fdev = ±1.0%, fmod = CLK/370 0111: fdev = ±1.5%, fmod = CLK/370 1000: fdev = ±2.0%, fmod = CLK/370 1001: fdev = ±0.5%, fmod = CLK/258 1010: fdev = ±1.0%, fmod = CLK/258 1011: fdev = ±1.5%, fmod = CLK/258 1100: fdev = ±2.0%, fmod = CLK/258 1101: fdev = ±0.5%, fmod = CLK/192 1110: fdev = ±1.0%, fmod = CLK/192 1111: fdev = ±1.5%, fmod = CLK/192
4	4	ROUT Config	7	R/W	0	Repeater Enable	0: Output ROUT± = disable 1: Output ROUT± = enable
			6:0	R/W	0000000	***Reserved***	***Reserved***

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Display Application

The DS92LV242x chipset is intended for interface between a host (graphics processor) and a display. It supports a 24-bit color depth (RGB888) and up to 1024 x 768 display formats. In a RGB888 application, 24 color bits (D[23:0]), Pixel Clock (CLKIN), and three control bits (C1, C2, C3) are supported across the serial link with CLKIN rates from 10 to 75 MHz. The chipset may also be used in 18-bit color applications. In this application, three to six general-purpose signals may also be sent from host to display.

The deserializer is expected to be placed close to its target device. The interconnect between the deserializer and the target device is typically in the 1 to 3 inch separation range. The input capacitance of the target device is expected to be in the 5 pF to 10 pF range. Take care of the CLKOUT output trace, as this signal is edge sensitive and strobes the data. It is also assumed that the fanout of the deserializer is one. If additional loads need to be driven, a logic buffer or mux device is recommended.

8.1.2 Live Link Insertion

The serializer and deserializer devices support live pluggable applications. The automatic receiver lock to random data *plug and go* hot insertion capability allows the DS92LV2422 to attain lock to the active data stream during a live insertion event.

8.1.3 Alternate Color / Data Mapping

Color Mapped Data Pin names are provided to specify a recommended mapping for 24-bit color applications. Seven [7] is assumed to be the MSB, and Zero [0] is assumed to be the LSB. While this is recommended, it is not required. When connecting to earlier generations of FPD-Link II serializer and deserializer devices, a color mapping review is recommended to ensure the correct connectivity is obtained. Table 17 provides examples for interfacing to 18-bit applications with or without the video control signals embedded. The DS92LV2422 deserializer provides additional flexibility with the MAP_SEL feature as well.

Table 17. Alternate Color and Data Mapping

18-BIT RGB	18-BIT RGB	24-BIT RGB	2421 PIN NAME	2422 PIN NAME	24-BIT RGB	18-BIT RGB	18-BIT RGB
LSB R0	GP0	R0	DI0	DO0	R0	GP0	LSB R0
R1	GP1	R1	DI1	DO1	R1	GP1	R1
R2	R0	R2	DI2	DO2	R2	R0	R2
R3	R1	R3	DI3	DO3	R3	R1	R3
R4	R2	R4	DI4	DO4	R4	R2	R4
MSB R5	R3	R5	DI5	DO5	R5	R3	MSB R5
LSB G0	R4	R6	DI6	DO6	R6	R4	LSB G0
G1	R5	R7	DI7	DO7	R7	R5	G1
G2	GP2	G0	DI8	DO8	G0	GP2	G2
G3	GP3	G1	DI9	DO9	G1	GP3	G3
G4	G0	G2	DI10	DO10	G2	G0	G4
MSB G5	G1	G3	DI11	DO11	G3	G1	MSB G5
LSB B0	G2	G4	DI12	DO12	G4	G2	LSB0
B1	G3	G5	DI13	DO13	G5	G3	B1

Application Information (continued)

Table 17. Alternate Color and Data Mapping (continued)

18-BIT RGB	18-BIT RGB	24-BIT RGB	2421 PIN NAME	2422 PIN NAME	24-BIT RGB	18-BIT RGB	18-BIT RGB
B2	G4	G6	DI14	DO14	G6	G4	B2
B3	G5	G7	DI15	DO15	G7	G5	B3
B4	GP4	B0	DI16	DO16	B0	GP4	B4
MSB B5	GP5	B1	DI17	DO17	B1	GP5	MSB B5
HS	B0	B2	DI18	DO18	B2	B0	HS
VS	B1	B3	DI19	DO19	B3	B1	VS
DE	B2	B4	DI20	DO20	B4	B2	DE
GP0	B3	B5	DI21	DO21	B5	B3	GP0
GP1	B4	B6	DI22	DO22	B6	B4	GP1
GP2	B5	B7	DI23	DO23	B7	B5	GP2
GND	HS	HS	CI1	CO1	HS	HS	GND
GND	VS	VS	CI2	CO2	VS	VS	GND
GND	DE	DE	CI3	CO3	DE	DE	GND
Scenario 3 (1)	**Scenario 2 (2)**	**Scenario 1 (3)**	**2421 Pin Name**	**2422 Pin Name**	**Scenario 1 (3)**	**Scenario 2 (2)**	**Scenario 3 (1)**

(1) Scenario 3 supports an 18-bit RGB color mapping, 3 un-embedded video control signals, and up to three general-purpose signals.
(2) Scenario 2 supports an 18-bit RGB color mapping, 3 embedded video control signals, and up to six general-purpose signals.
(3) Scenario 1 supports the 24-bit RGB color mapping, along with the 3 embedded video control signals. This is the native mode for the chipset.

8.2 Typical Applications

8.2.1 DS92LV2421 Typical Connection

Figure 38 shows a typical application of the DS92LV2421 serializer in pin control mode for a 24-bit application. The LVDS outputs require 100-nF AC-coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1-µF capacitors and a 4.7-µF capacitor must be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. In this application, the RFB pin is tied low to latch data on the falling edge of the CLKIN. The application assumes connection to the companion deserializer (DS92LV2422), and therefore the configuration pins CONFIG[1:0] are also both tied low. In this example, the cable is long, and therefore the VODSEL pin is tied high and a De-Emphasis value is selected by the resistor R1. The interface to the host is with 1.8-V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8-V rail. The optional serial bus control is not used in this example, thus the SCL, SDA, and ID[X] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

Typical Applications (continued)

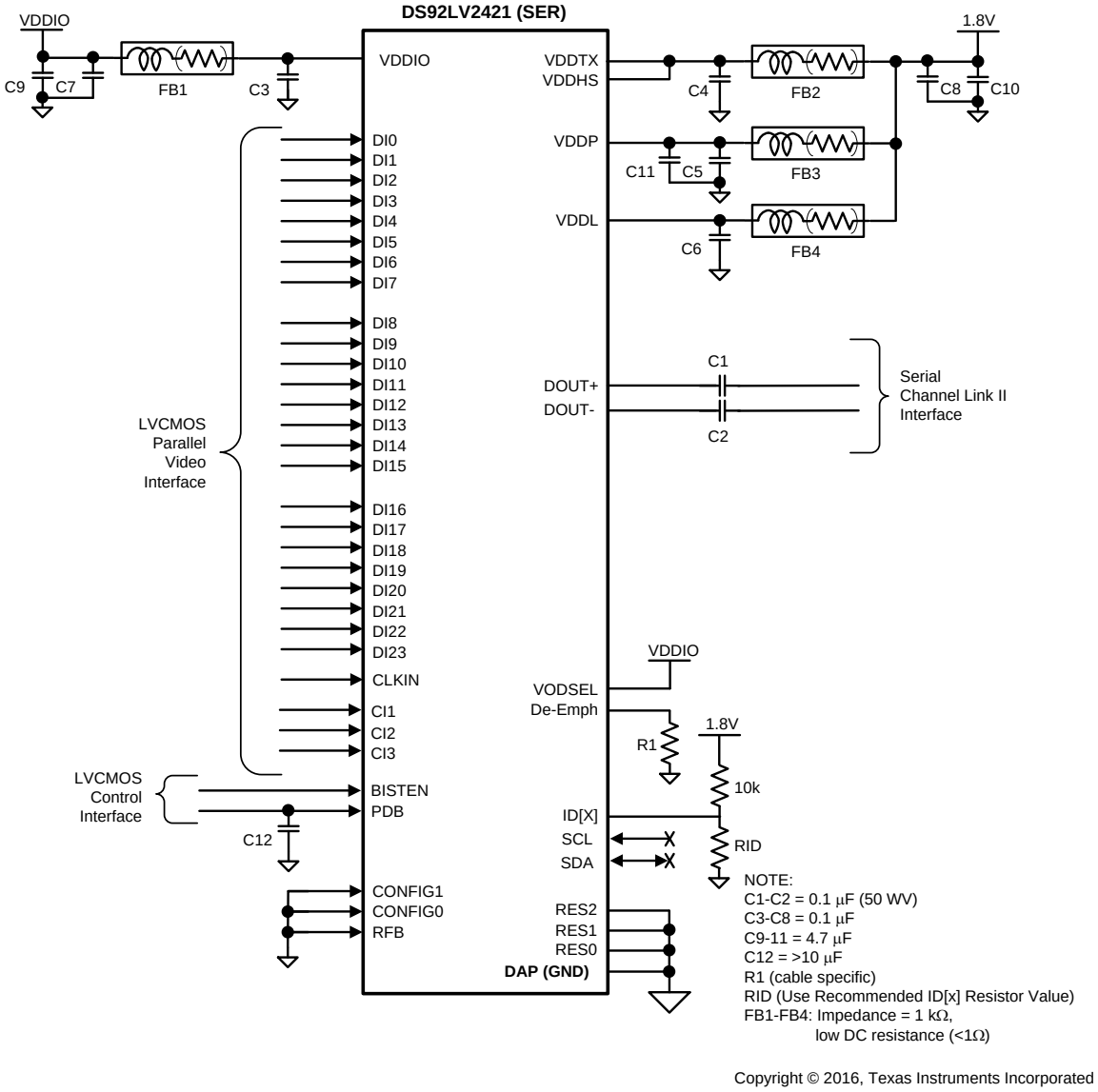


Figure 38. DS92LV2421 Typical Connection Diagram – Pin Control

8.2.1.1 Design Requirements

For this example, Table 18 lists the design parameters.

Table 18. Design Parameters

PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V to 3.3 V
VDDL, VDDP, VDDHS, VDDTX	1.8 V
AC-Coupling Capacitor for DOUT±	100 nF

8.2.1.2 Detailed Design Procedure

The DOUT± outputs require 100-nF AC-coupling capacitors to the line. The power supply filter capacitors are placed near the power supply pins. A smaller capacitance capacitor must be located closer to the power supply pins.

The VODSEL pin is tied to VDDIO for the long cable application. The de-emphasis pin may connect a resistor to ground. Refer to Table 3. The PDB and BISTEN pins are assumed to be controlled by a microprocessor. The PDB must remain in a low state until all power supply voltages reach the final voltage. The RFB pin is tied low to latch data on the falling edge of the PCLK and tied high for the rising clock edge. The CONFIG[1:0] pins are set depending on operating modes and backward compatibility. The SCL, SDA, and ID[X] pins are left open when these serial bus control pins are unused. The RES[2:0] pins and DAP must be tied to ground.

8.2.1.3 Application Curve

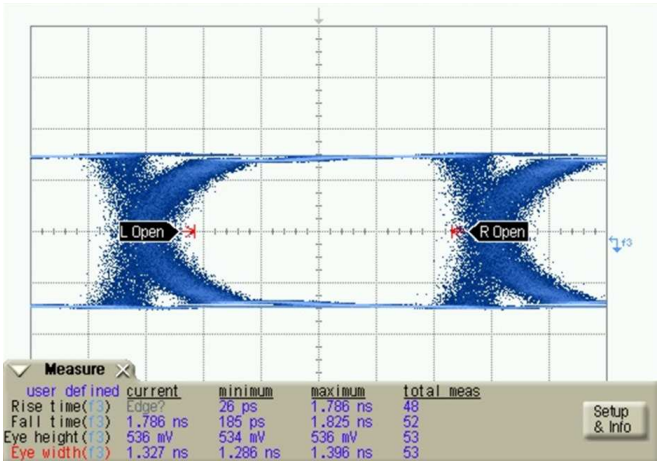


Figure 39. Eye Diagram at CLK = 20 MHz

8.2.2 DS92LV2422 Typical Connection

Figure 40 shows a typical application of the DS92LV2422 deserializer in pin or strap control mode for a 24-bit application. The LVDS inputs use 100-nF coupling capacitors to the line, and the receiver provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, seven 0.1-µF capacitors and two 4.7-µF capacitors must be used for local device bypassing. System General Purpose Output (GPO) signals control the PDB and the BISTEN pins. In this application, the RFB pin is tied low to strobe the data on the falling edge of the CLKOUT.

Because the device is in pin or strap control mode, four 10-kΩ pullup resistors are used on the parallel output bus to select the desired device features. CONFIG[1:0] is set to 01'b for normal mode with control signal filter enabled, and this is accomplished with the strap pullup on DO23. The receiver input equalizer is also enabled and set to provide 7.5 dB of gain, and this is accomplished with EQ[3:0] set to 1001'b with strap pullups on DO12 and DO15. To reduce parallel bus EMI, the SSCG feature is enabled and set to fmod = CLK/2168 and ±1% with SSC[3:0] set to 0010'b and a strap pullup on DO4. The desired features are set with the use of the four pullup resistors.

The interface to the target display is with 3.3-V LVCMOS levels, thus the VDDIO pin is connected to the 3.3-V rail. The optional serial bus control is not used in this example, thus the SCL, SDA and ID[X] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

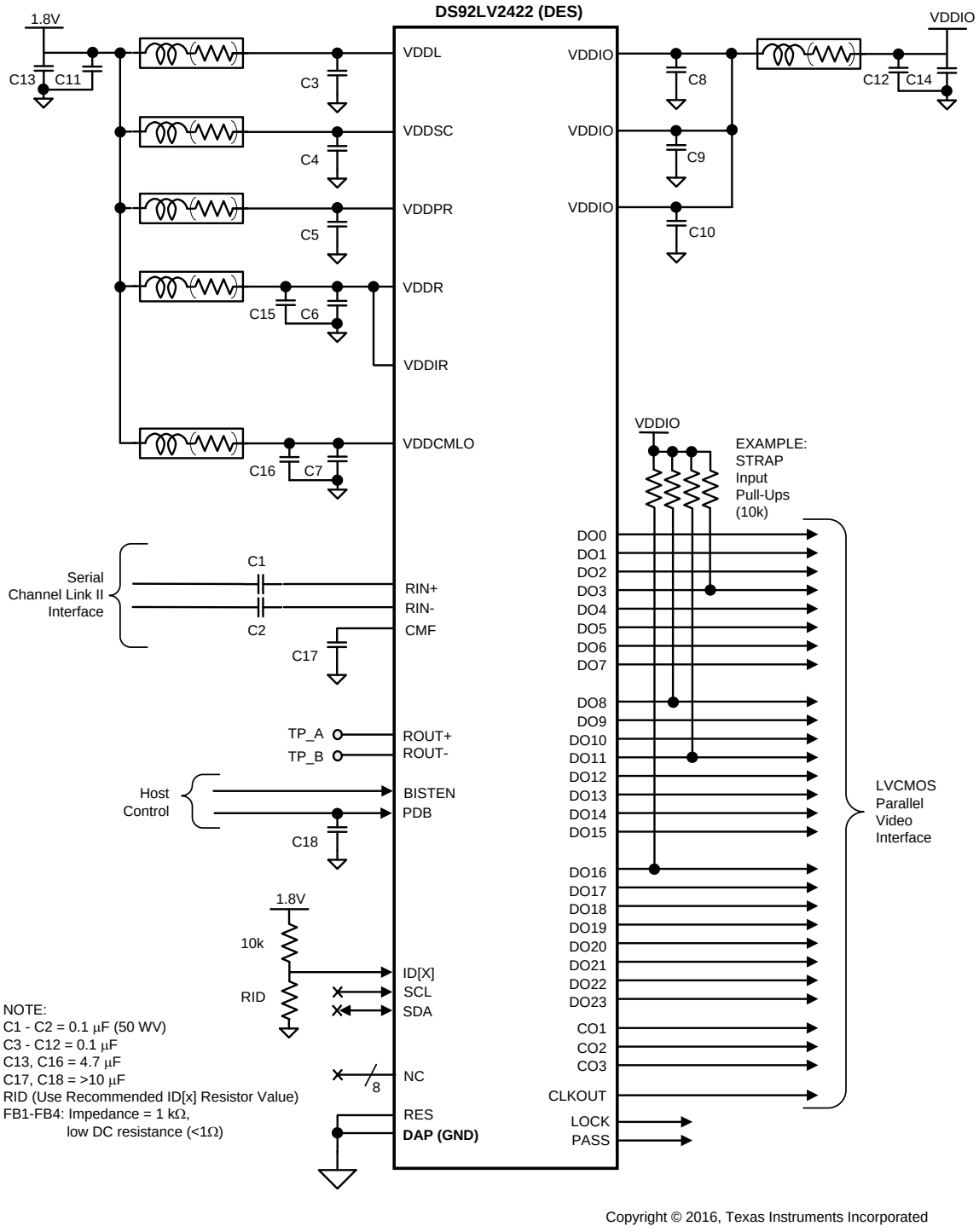


Figure 40. DS92LV2422 Typical Connection Diagram — Pin Control

8.2.2.1 Design Requirements

For this example, Table 19 lists the design parameters.

Table 19. Design Parameters

PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V to 3.3 V
VDDL, VDDSC, VDDPR, VDDR, VDDIR, VDDCMLO	1.8 V
AC-Coupling Capacitor for DOUT±	100 nF

8.2.2.2 Detailed Design Procedure

The RIN± inputs require 100-nF AC-coupling capacitors to the line. The power supply filter capacitors are placed near the power supply pins. A smaller capacitance capacitor must be placed closer to the power supply pins.

The device has 22 control and configuration pins that are called strap pins. These pins include an internal pulldown. For a high state, use a 10-kΩ resistor pullup to VDDIO.

The PDB and BISTEN pins are assumed to be controlled by a microprocessor. The PDB has to be in a low state until all power supply voltages reach the final voltage. The SCL, SDA, and ID[X] pins are left open when these serial bus control pins are unused.

The RES pin and DAP must be tied to ground.

8.2.2.3 Application Curves

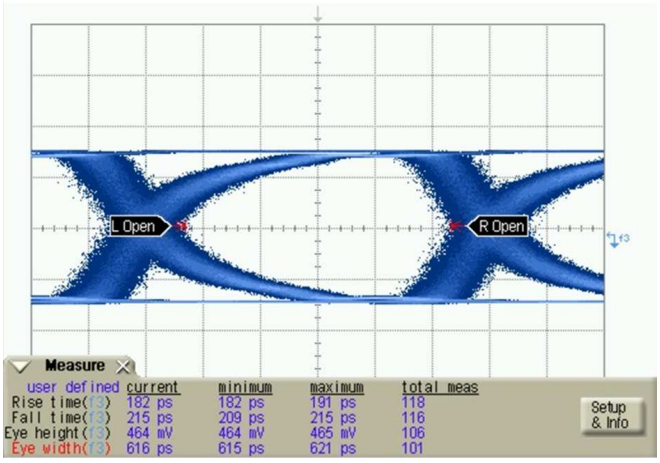


Figure 41. Eye Diagram at CLK = 45 MHz

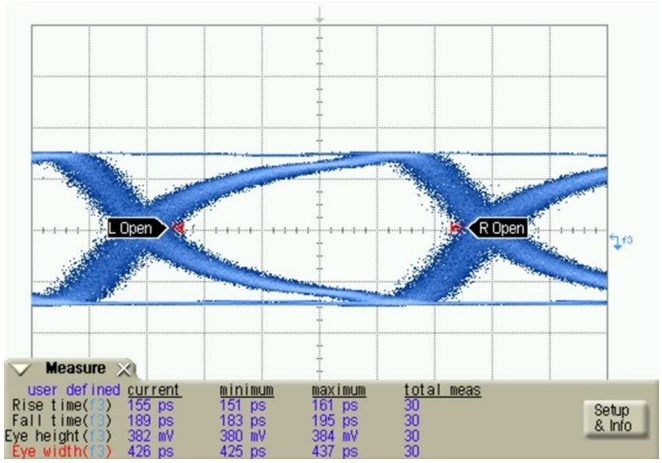


Figure 42. Eye Diagram at CLK = 65 MHz

9 Power Supply Recommendations

9.1 Power-Up Requirements and PDB Pin

The VDD (VDDn and VDDIO) supply ramp must be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms, then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to VDDIO, TI recommends using a 10-kΩ pullup and a 22-µF capacitor to GND to delay the PDB input signal.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power or ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies and makes the value and placement of external bypass capacitors less critical. External bypass capacitors must include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2 µF to 10 µF range. Voltage rating of the tantalum capacitors must be at least 5x the power supply voltage being used.

Surface-mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 µF to 100 µF range and smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane, with vias on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Place LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100 Ω are typically recommended for LVDS interconnects. The closely coupled lines help to ensure that coupled noise appears as common mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

10.1.1 WQFN (LLP) Stencil Guidelines

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP (WQFN) package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown below:

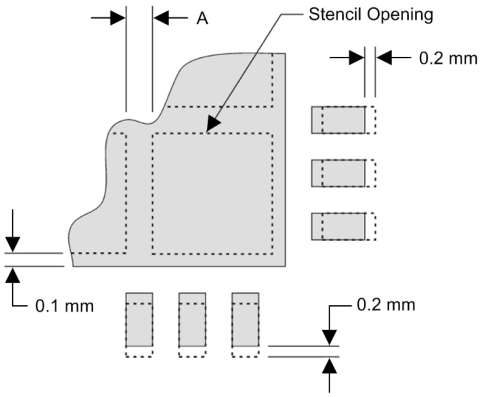


Figure 43. No Pullback LLP, Single Row Reference Diagram

Layout Guidelines (continued)

Table 20. No Pullback LLP Stencil Aperture Summary for DS92LV2421 and DS92LV2422

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS92LV2421	48	SQA48A	0.25 × 0.6	0.5	5.1 × 5.1	0.25 × 0.7	1.1 × 1.1	16	0.2
DS92LV2422	60	SQA60B	0.25 × 0.8	0.5	7.2 × 7.2	0.25 × 0.9	1.16 × 1.16	25	0.3

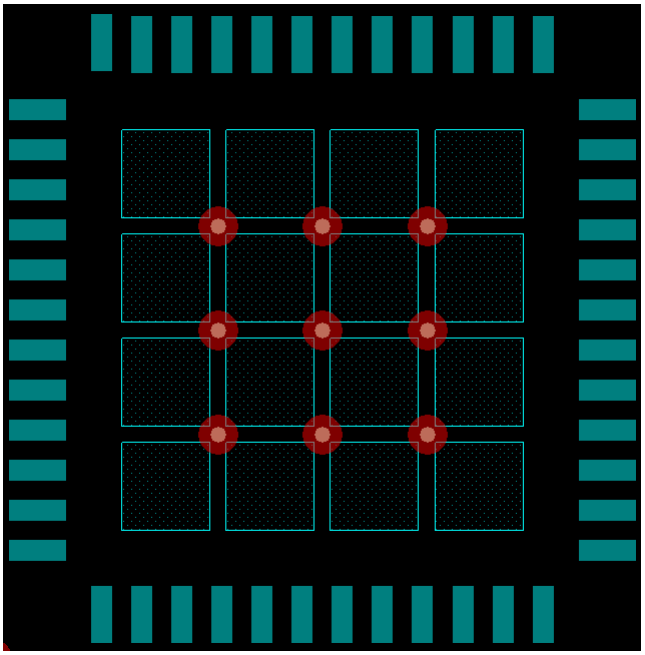


Figure 44. 48-Pin WQFN Stencil Example of Via and Opening Placement

Information on the WQFN style package is provided in *Leadless Leadframe Package (LLP) Application Report* (SNOA401).

10.1.2 Transmission Media

The serializer and deserializer chipset is intended to be used in a point-to-point configuration through a PCB trace or through twisted pair cable. The serializer and deserializer provide internal terminations for a clean signaling environment. The interconnect for CML must present a differential impedance of 100 Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

10.1.3 LVDS Interconnect Guidelines

See AN-1108 *Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and AN-905 *Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S, 2S, 3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of vias
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual, available in PDF format from the TI web site at: www.ti.com/lvds.

10.2 Layout Example

The following PCB layout examples are derived from the layout design of the LV24EVK01 Evaluation Module. These graphics and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the serializer and deserializer pair.

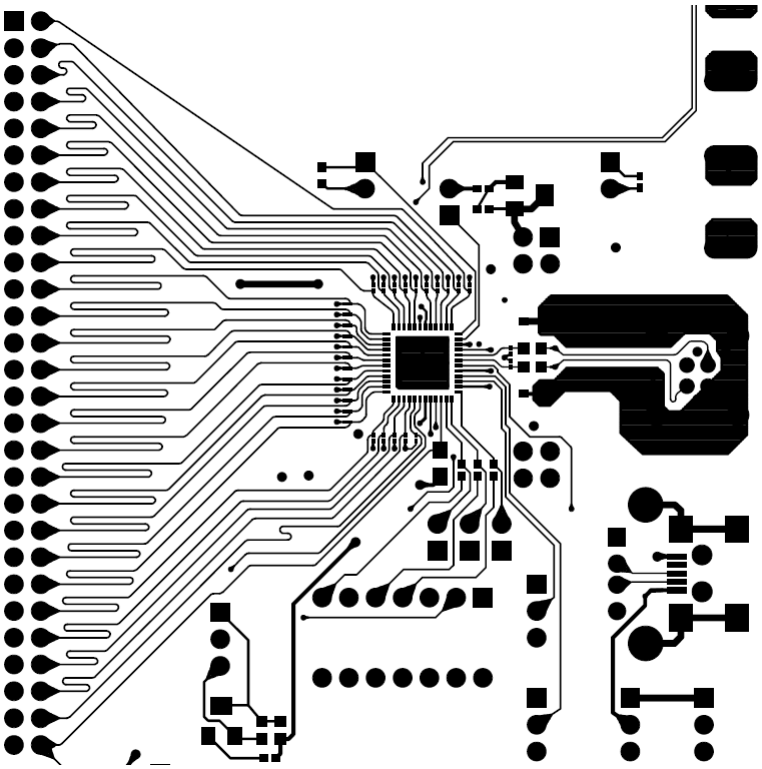


Figure 45. DS92LV2421 Serializer Example Layout

Layout Example (continued)

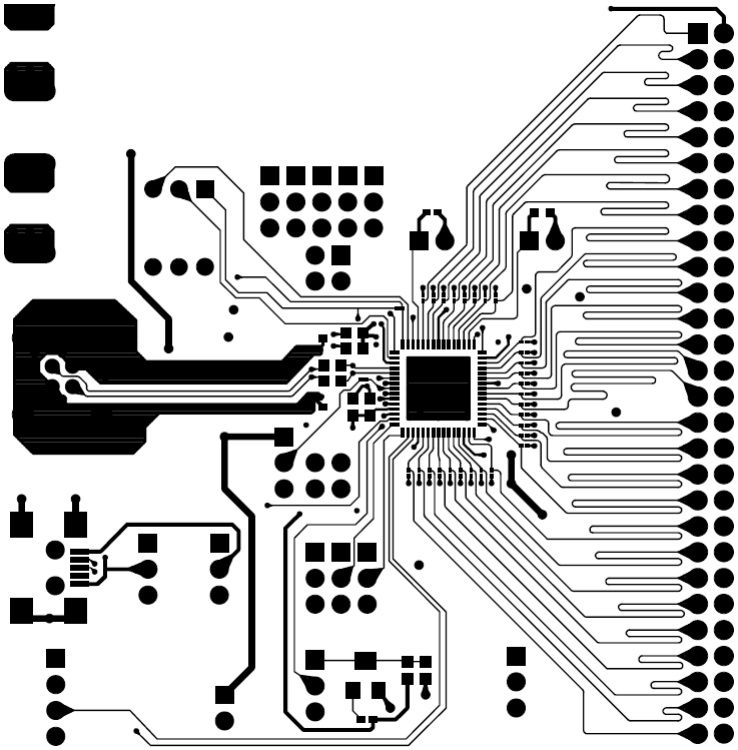


Figure 46. DS92LV2422 Deserializer Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

For development support see the following:

LVDS Owner's Manual, www.ti.com/lvds

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Absolute Maximum Ratings for Soldering*, SNOA549
- *Leadless Leadframe Package (LLP) Application Report*, SNOA401
- AN-1108 *Channel-Link PCB and Interconnect Design-In Guidelines*, SNLA008
- AN-905 *Transmission Line RAPIDESIGNER Operation and Applications Guide*, SNLA035

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 21. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DS92LV2421	Click here	Click here	Click here	Click here	Click here
DS92LV2422	Click here	Click here	Click here	Click here	Click here

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS92LV2421SQ/NOPB	ACTIVE	WQFN	RHS	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LV2421SQ	Samples
DS92LV2421SQE/NOPB	ACTIVE	WQFN	RHS	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LV2421SQ	Samples
DS92LV2421SQX/NOPB	ACTIVE	WQFN	RHS	48	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LV2421SQ	Samples
DS92LV2422SQ/NOPB	ACTIVE	WQFN	NKB	60	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LV2422SQ	Samples
DS92LV2422SQE/NOPB	ACTIVE	WQFN	NKB	60	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LV2422SQ	Samples
DS92LV2422SQX/NOPB	ACTIVE	WQFN	NKB	60	2000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LV2422SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

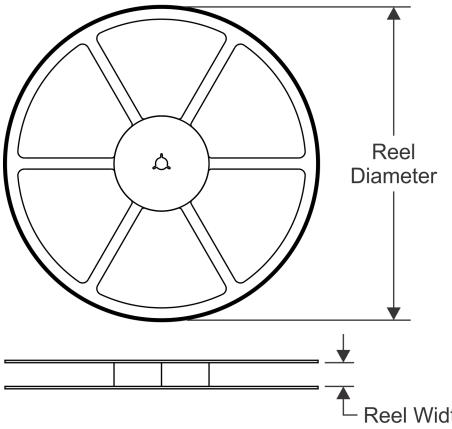
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

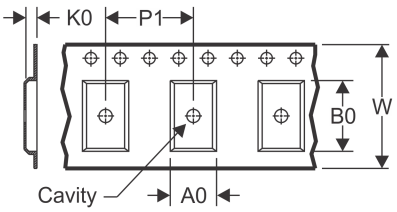
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

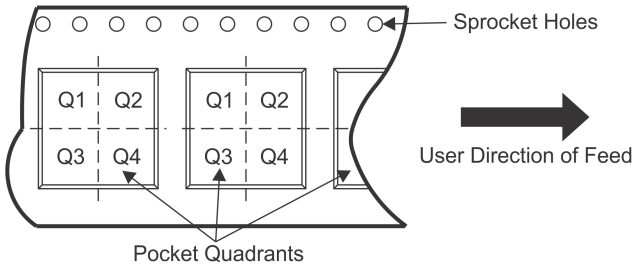


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

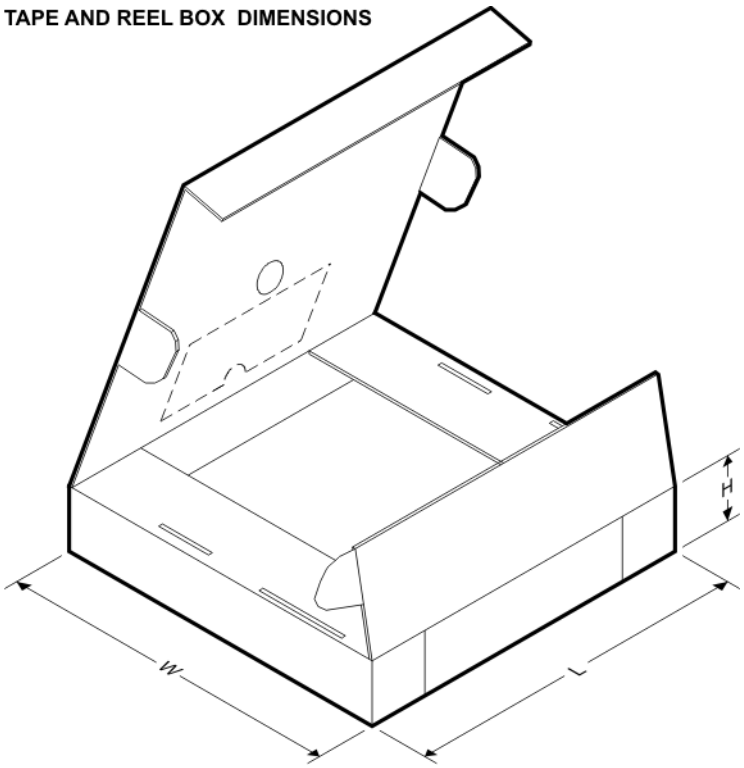
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV2421SQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV2421SQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV2421SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV2422SQ/NOPB	WQFN	NKB	60	1000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS92LV2422SQE/NOPB	WQFN	NKB	60	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS92LV2422SQX/NOPB	WQFN	NKB	60	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

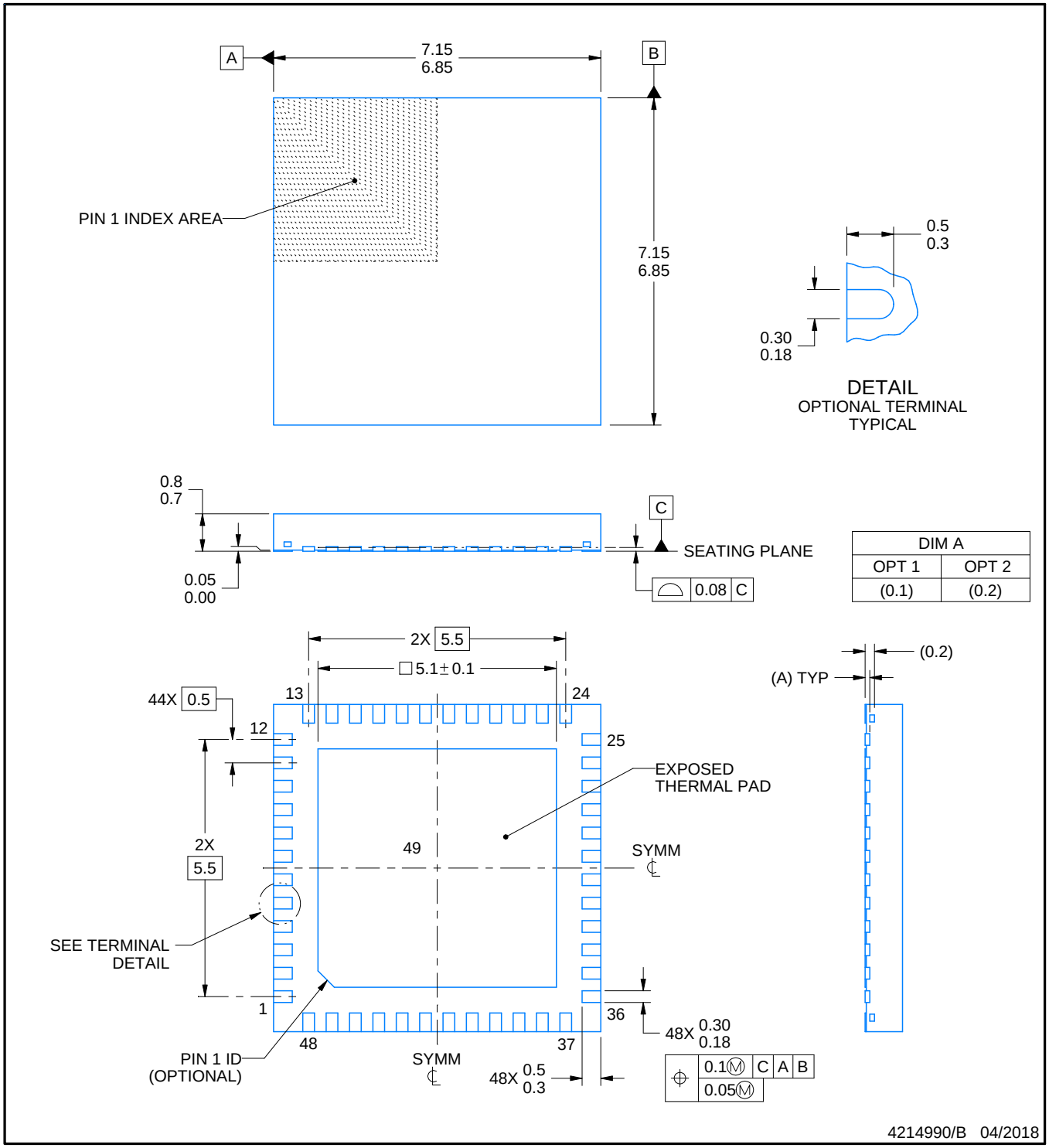
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV2421SQ/NOPB	WQFN	RHS	48	1000	367.0	367.0	38.0
DS92LV2421SQE/NOPB	WQFN	RHS	48	250	210.0	185.0	35.0
DS92LV2421SQX/NOPB	WQFN	RHS	48	2500	367.0	367.0	38.0
DS92LV2422SQ/NOPB	WQFN	NKB	60	1000	367.0	367.0	38.0
DS92LV2422SQE/NOPB	WQFN	NKB	60	250	210.0	185.0	35.0
DS92LV2422SQX/NOPB	WQFN	NKB	60	2000	367.0	367.0	38.0

PACKAGE OUTLINE

RHS0048A

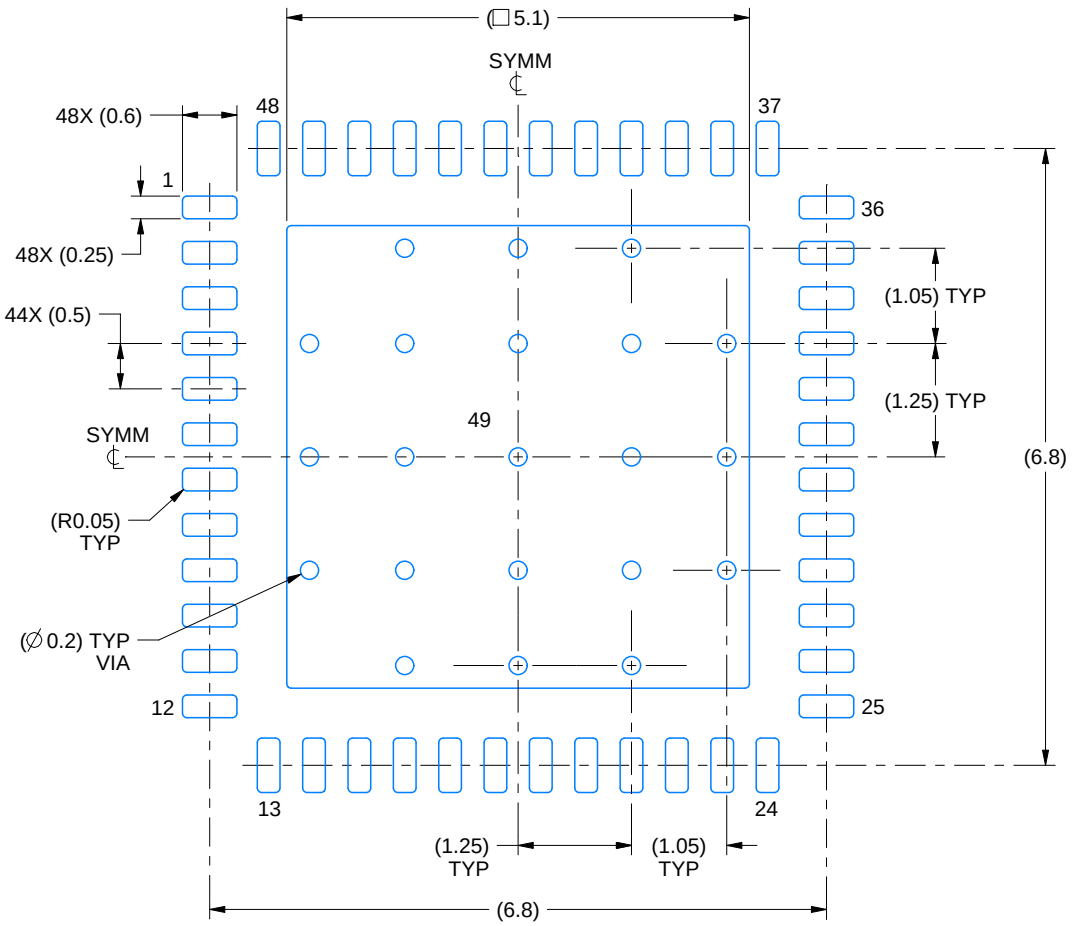
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

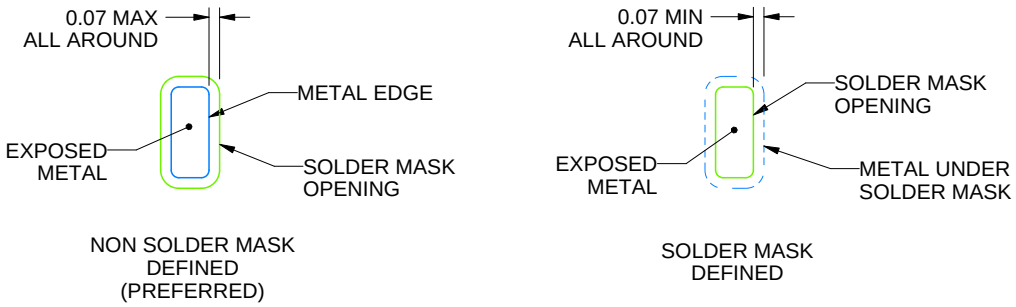


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

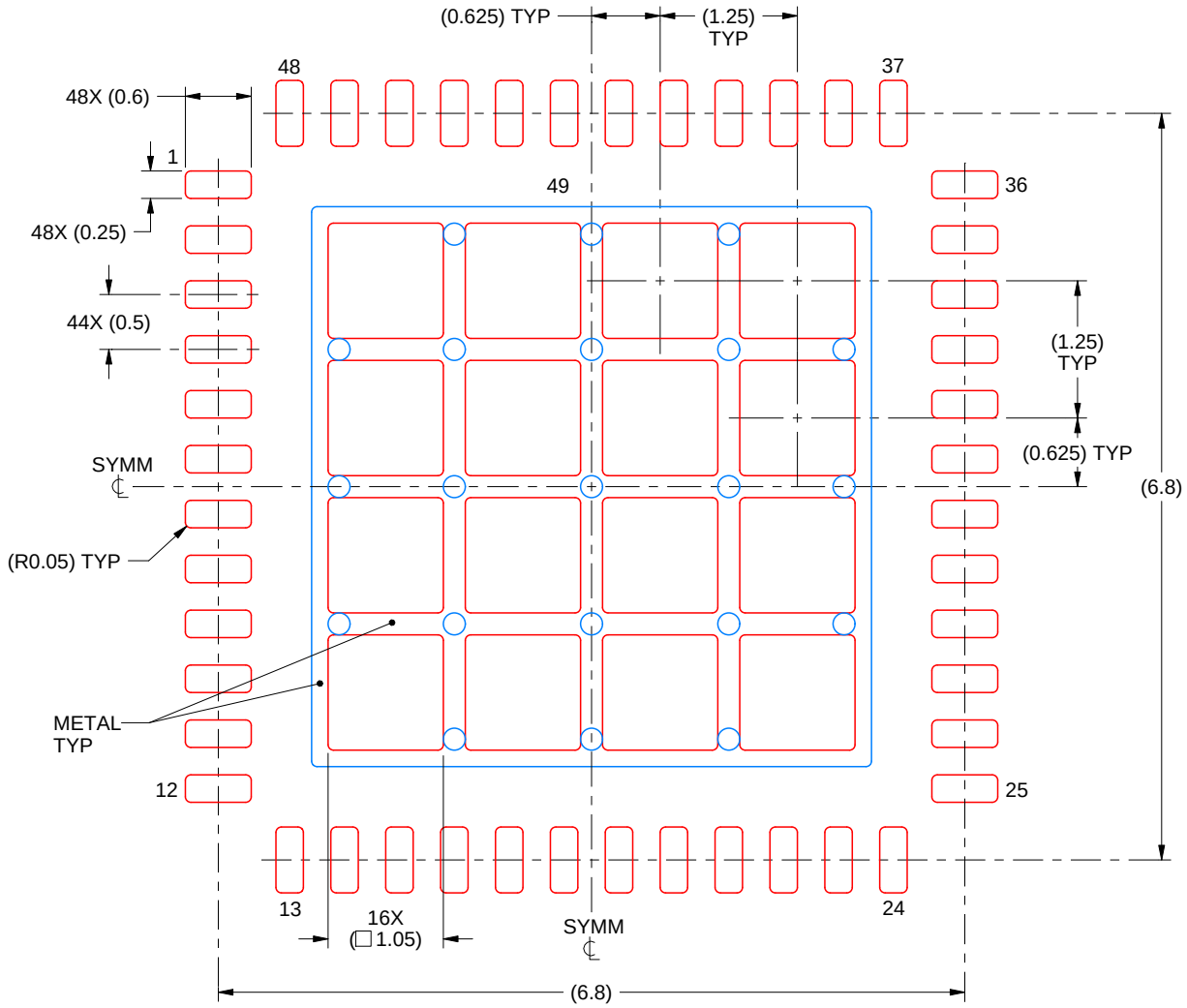


SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

NOTES: (continued)

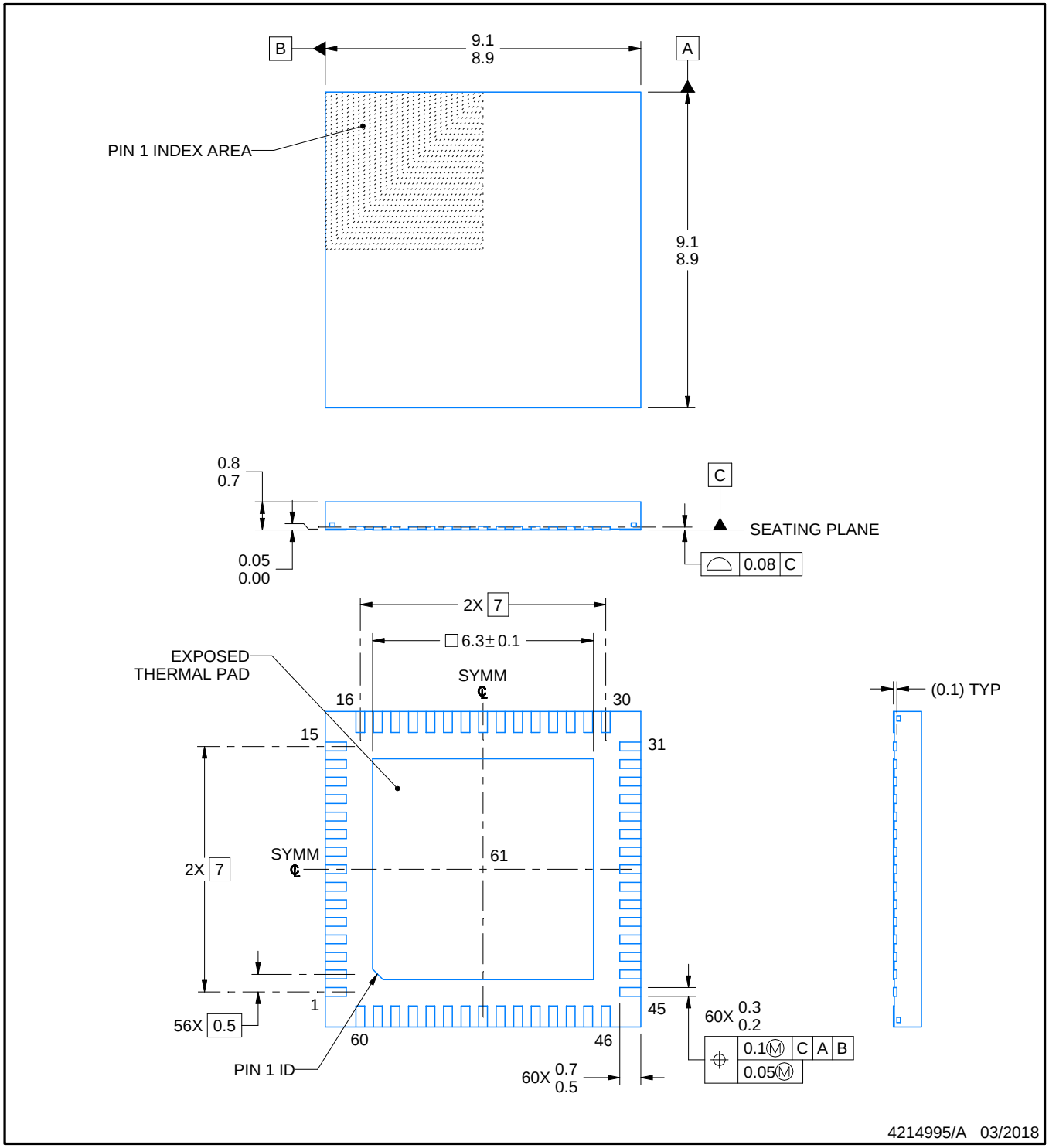
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

NKB0060B

PACKAGE OUTLINE

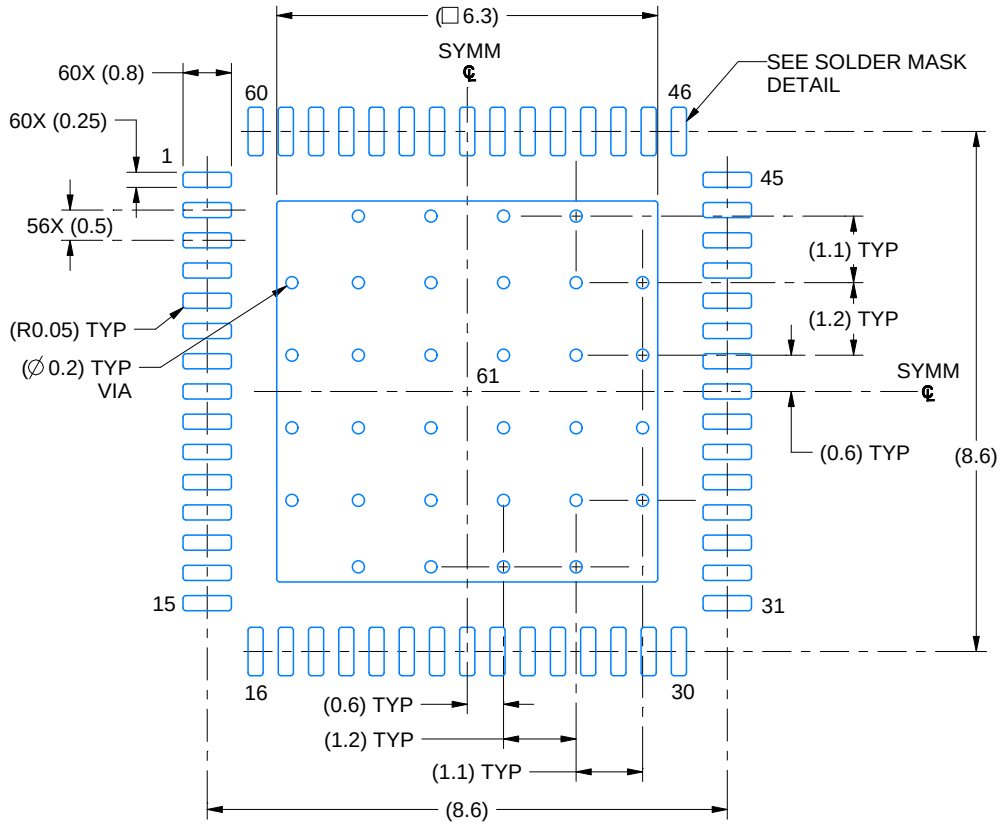
VQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

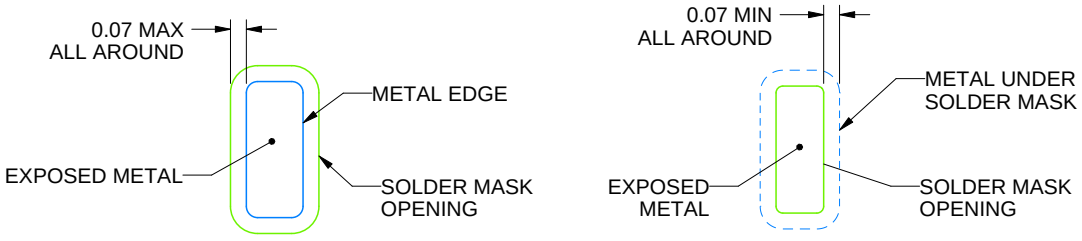


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

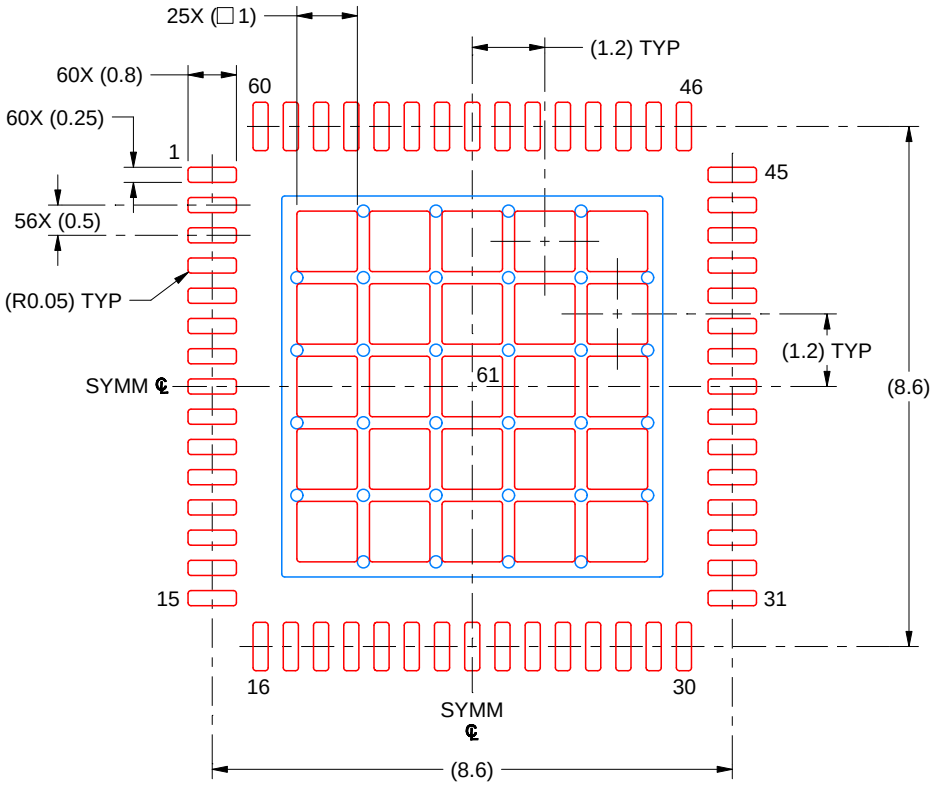


SOLDER MASK DETAILS

4214995/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

EXPOSED PAD 61
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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