DS96F172MQML/DS96F174MQML EIA-485/EIA-422 Quad Differential Drivers

Check for Samples: DS96F172MQML, DS96F174MQML

FEATURES

- **Meets EIA-485 and EIA-422 Standards**
- **Monotonic Differential Output Switching**
- **TRI-STATE Outputs**
- **Designed for Multipoint bus Transmission**
- **Common Mode Output Voltage Range: −7.0V to +12V**
- **Operates from Single +5.0V Supply**
- **Reduced Power Consumption**
- **Thermal Shutdown Protection**
- **DS96F172 and DS96F174 are Lead and Function Compatible with the SN75172/174 or the AM26LS31/MC3487**

DESCRIPTION

The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA-485 Standards. The DS96F172 and the DS96F174 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F172 and DS96F174 to operate at higher speeds while minimizing power consumption.

The DS96F172 and the DS96F174 have TRI-STATE outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

Connection Diagrams

16-Lead CDIP Package (see Package Number NFE0016A)

DS96F172 (Top View)

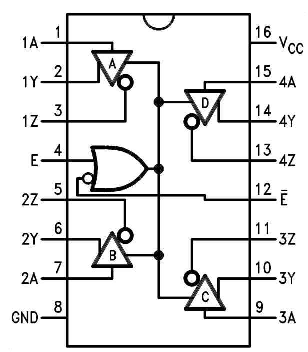


Figure 1.

DS96F174 (Top View)

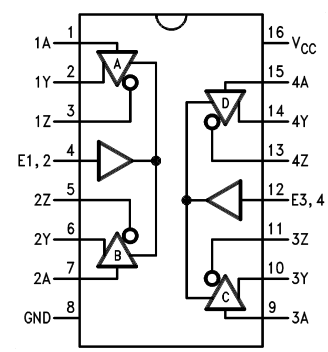


Figure 2.

20-Lead LCCC Package (see Package Number NAJ0020A)

NC = No connection

DS96F172 (Top View)

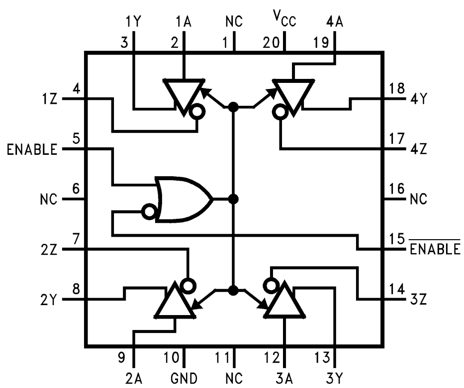


Figure 3.

DS96F174 (Top View)

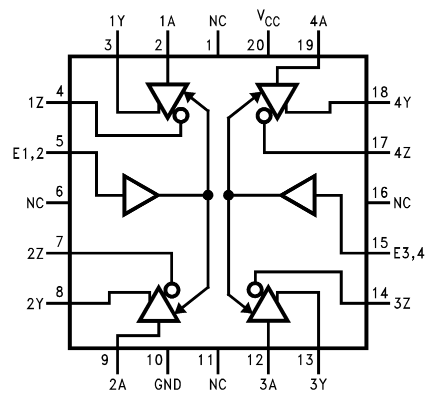


Figure 4.

Logic Diagrams

DS96F172

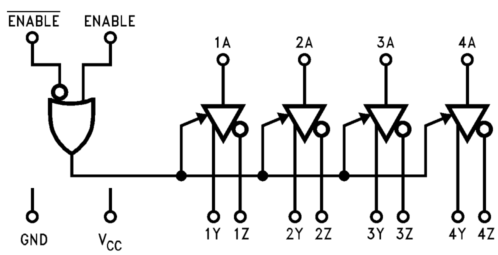


Figure 5.

DS96F174

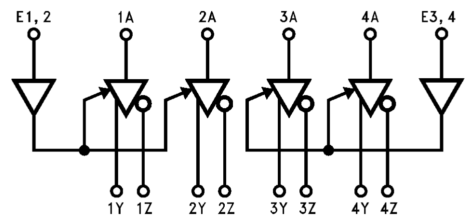


Figure 6.

Function Tables (Each Driver)

Table 1. DS96F172[1]

Input	Enable		Outputs	
A	**E**	**$\overline{E}$**	**Y**	**Z**
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

Table 2. DS96F174[1]

Input	Enable	Outputs	
A	**E**	**Y**	**Z**
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

Storage Temperature Range (T_{Stg})	−65°C ≤ T_A ≤ +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation at 25°C[2]	
LCCC package	2,000 mW
CDIP package	1,800 mW
Ceramic Flatpack package	1,000 mW
Supply Voltage	7.0V
Enable Input Voltage	5.5V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Above T_A = 25°C, derate LCCC package 13.3, CDIP package 12.5, Ceramic flatpack package 7.1 mW/°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Common Mode Output Voltage (V_{OC})	−7.0	+12.0	V
Output Current High (I_{OH})		−60	mA
Output Current Low (I_{OL})		60	mA
Operating Temperature (T_A)	−55	+125	°C

Quality Conformance Inspection

Table 3. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS96F172/DS96F174 Electrical Characteristics AC/DC Parameters(1)

The following conditions apply, unless otherwise specified.
DC: V_{CC} = 5.5V
AC: V_{CC} = 5.0V

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
V_{IL}	Logical 0 Input Voltage				0.8	V	1
					0.7	V	2, 3
V_{IH}	Logical 1 Input Voltage			2.0		V	1, 2, 3
V_{IC}	Input Clamp Voltage	I = -18mA		-1.5		V	1, 2, 3
V_{OD1}	Differential Output Voltage	I_O = 0mA			6.0	V	1, 2, 3
V_{OD2}	Differential Output Voltage	V_{CC} = 4.5V, R_L = 54Ω Figure 7		1.5		V	1, 2
			See(2)	1.2		V	3
V_{OD2}	Differential Output Voltage	V_{CC} = 4.5V, R_L = 100Ω Figure 7		2.0		V	1, 2, 3
ΔV_{OD1}	Change In Magnitude of V_{OD2}	V_{CC} = 4.5V, R_L = 54Ω	See(3)	-200	200	mV	1, 2
			See(2)(3)	-400	400	mV	3
ΔV_{OD2}	Change In Magnitude of V_{OD2}	V_{CC} = 4.5V, R_L = 100Ω	See(3)	-200	200	mV	1, 2
			See(2)(3)	-400	400	mV	3
V_{OC}	Common Mode Output Voltage	R_L = 54Ω Figure 7			3.0	V	1, 2, 3
V_{OC}	Common Mode Output Voltage	R_L = 100Ω Figure 7			3.0	V	1, 2, 3
ΔV_{OC}	Change in Magnitude of V_{OC}	V_{CC} = 4.5V, R_L = 54Ω Figure 7	See(3)	-200	200	mV	1, 2, 3
ΔV_{OC}	Change in Magnitude of V_{OC}	V_{CC} = 4.5V, R_L = 100Ω Figure 7	See(4)	-200	200	mV	1, 2, 3
I_O	Output Current With Power Off	V_{CC} = 0V, V_O = -7V to 12V		-50	50	µA	1, 2, 3

(1) All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.
(2) −55°C limit exceeds EIA standard RS−485 specification
(3) $\Delta|V_{OD}|$ is the change in magnitude of V_{OD}, that occurs when the input is changed between high and low levels.
(4) $\Delta|V_{OC}|$ is the change in magnitude of the V_{OC} that occurs when the input is changed between high and low levels.

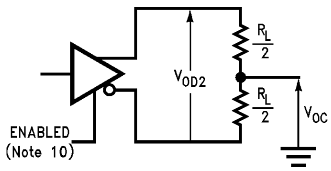
DS96F172/DS96F174 Electrical Characteristics AC/DC Parameters[1] (continued)

The following conditions apply, unless otherwise specified.
DC: V_{CC} = 5.5V
AC: V_{CC} = 5.0V

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
I_{OZ}	High Impedance State Output Current	V_O = -7V to 12V		-50	50	µA	1, 2, 3
I_{IH}	Logical 1 Input Current	V_I = 2.4V			20	µA	1, 2, 3
I_{IL}	Logical 0 Input Current	V_I = 0.4V		-50		µA	1, 2, 3
I_{CC}	Supply Current	Outputs Enabled			50	mA	1, 2, 3
I_{CCX}	Supply Current	Outputs Disabled			30	mA	1, 2, 3
I_{OS1}	Short Circuit Output Current	V_O = -7V	See[5]	-250		mA	1, 2, 3
I_{OS2}	Short Circuit Output Current	V_O = 0V	See[5]	-150		mA	1, 2, 3
I_{OS3}	Short Circuit Output Current	$V_O = V_{CC}$	See[5]		150	mA	1, 2, 3
I_{OS4}	Short Circuit Output Current	V_O = 12V	See[5]		250	mA	1, 2, 3
t_{PLH}	Propagation Delay Lo to Hi level	R_L = 27Ω, C_L = 15pF Figure 10			25	ns	10, 11
					16	ns	9
t_{PHL}	Propagation Delay Hi to Low Level	R_L = 27Ω, C_L = 15pF Figure 10			25	ns	10, 11
					16	ns	9
SKEW	Output to Output Delay Time	R_L = 60Ω			10	ns	10, 11
					4	ns	9
t_{LZ}	Output Disable Time From Low Level	R_L = 110Ω, C_L = 50pF Figure 12			40	ns	10, 11
					25	ns	9
t_{HZ}	Output Disable Time From High Level	R_L = 110Ω, C_L = 50pF Figure 11			80	ns	10, 11
					30	ns	9
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, C_L = 50pF Figure 12			100	ns	10, 11
					40	ns	9
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, C_L = 50pF Figure 10			40	ns	10, 11
					32	ns	9
t_{DD}	Differential Output Delay Time	R_L = 60Ω, C_L = 15pF Figure 9			30	ns	10, 11
					22	ns	9
t_{TD}	Differential Output Transition Time	R_L = 60Ω, C_L = 15pF Figure 9			40	ns	10, 11
					22	ns	9

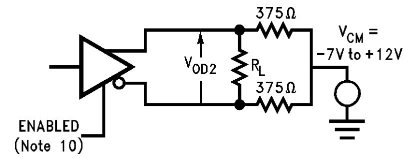
(5) 0.2µF cap is connected between the output and Gnd to reduce oscillation.

PARAMETER MEASUREMENT INFORMATION



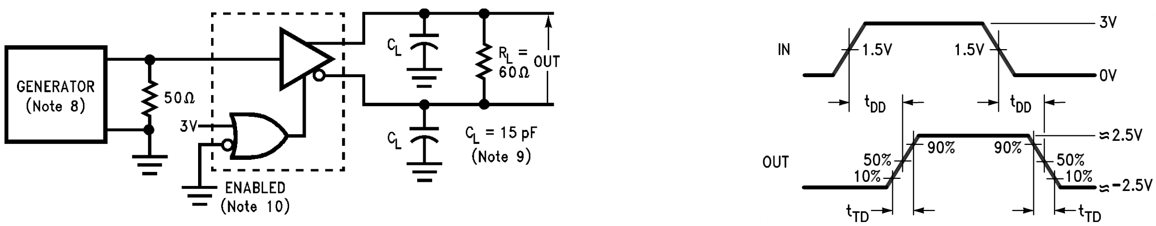
Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Figure 7. Differential and Common Mode Output Voltage



Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Figure 8. Differential Output Voltage with Varying Common Mode Voltage

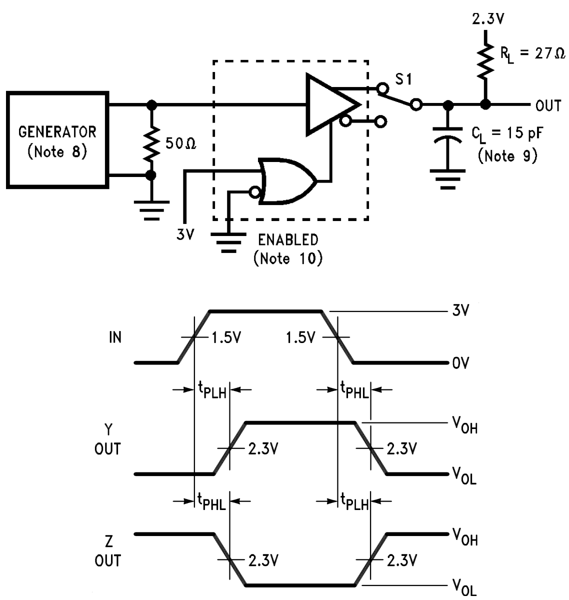


Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, t_r ≤ 5.0 ns, t_f ≤ 5.0 ns, Z_O = 50Ω.

Note 9: C_L includes probe and jig capacitance.

Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Figure 9. Differential Output Delay and Transition Times



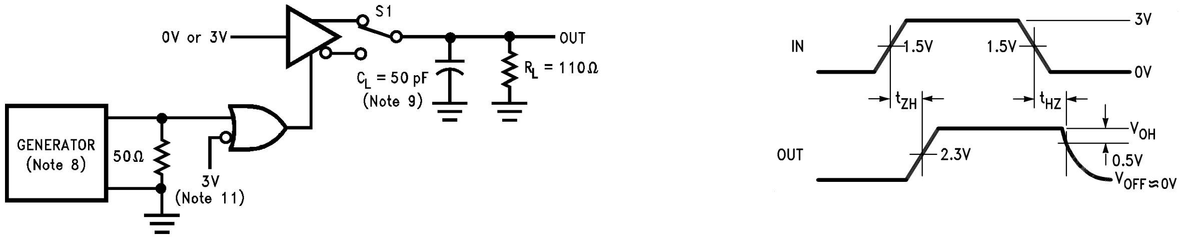
Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, t_r ≤ 5.0 ns, t_f ≤ 5.0 ns, Z_O = 50Ω.

Note 9: C_L includes probe and jig capacitance.

Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Figure 10. Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION (continued)

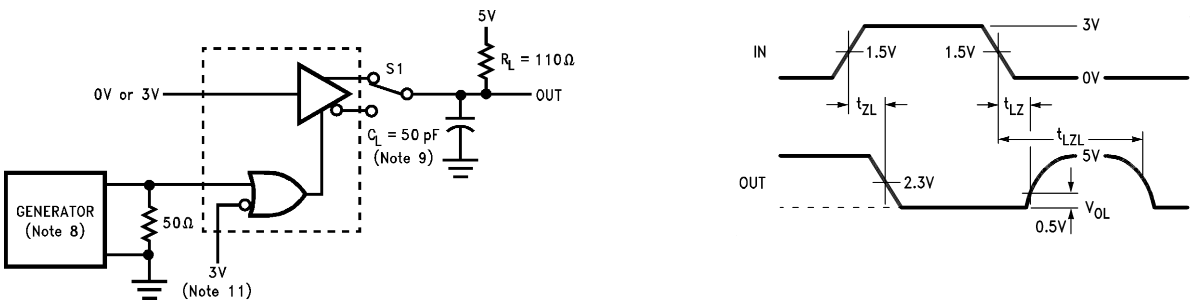


Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, $t_r \le 5.0$ ns, $t_f \le 5.0$ ns, $Z_O = 50\Omega$.

Note 9:C_L includes probe and jig capacitance.

Note 11: To test the active low Enable $\overline{E}$ of DS96F172 ground $\overline{E}$ and apply an inverted waveform to $\overline{E}$. DS96F174 has active high Enable only.

Figure 11. t_{ZH} and t_{HZ}



Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, $t_r \le 5.0$ ns, $t_f \le 5.0$ ns, $Z_O = 50\Omega$.

Note 9:C_L includes probe and jig capacitance.

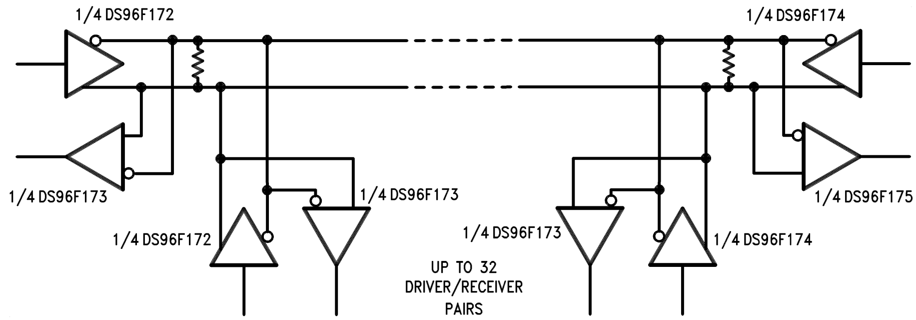
Note 11: To test the active low Enable $\overline{E}$ of DS96F172 ground $\overline{E}$ and apply an inverted waveform to $\overline{E}$. DS96F174 has active high Enable only.

Figure 12. t_{ZL}, t_{LZ}, t_{LZL}

NOTE

For more information see Application Bulletin, Contact Product Marketing.

TYPICAL APPLICATION



The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

Table 4. Revision History

Released	Revision	Section	Changes
8–Apr-11	A	New Release, Corporate format	2 MDS data sheets converted into one Corp. data sheet format. MNDS96F172M-X Rev 1A0 & MNDS96F174M-X Rev 1B0 will be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9076501M2A	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	DS96F172ME /883 Q 5962-90765 01M2A ACO 01M2A >T	Samples
5962-9076501MEA	ACTIVE	CDIP	NFE	16	25	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS96F172MJ/883 5962-9076501MEA Q	Samples
5962-9076502M2A	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	DS96F174ME /883 Q 5962-90765 02M2A ACO 02M2A >T	Samples
5962-9076502MEA	ACTIVE	CDIP	NFE	16	25	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS96F174MJ/883 5962-9076502MEA Q	Samples
5962-9076502VEA	ACTIVE	CDIP	NFE	16	25	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS96F174MJ-QMLV 5962-9076502VEA Q	Samples
DS96F172ME/883	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	DS96F172ME /883 Q 5962-90765 01M2A ACO 01M2A >T	Samples
DS96F172MJ/883	ACTIVE	CDIP	NFE	16	25	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS96F172MJ/883 5962-9076501MEA Q	Samples
DS96F174ME/883	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	DS96F174ME /883 Q 5962-90765 02M2A ACO 02M2A >T	Samples
DS96F174MJ-QMLV	ACTIVE	CDIP	NFE	16	25	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS96F174MJ-QMLV 5962-9076502VEA Q	Samples
DS96F174MJ/883	ACTIVE	CDIP	NFE	16	25	TBD	CU SNPB	Level-1-NA-UNLIM	-55 to 125	DS96F174MJ/883 5962-9076502MEA Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF DS96F174MQML, DS96F174MQML-SP :

- Military: DS96F174MQML

- Space: DS96F174MQML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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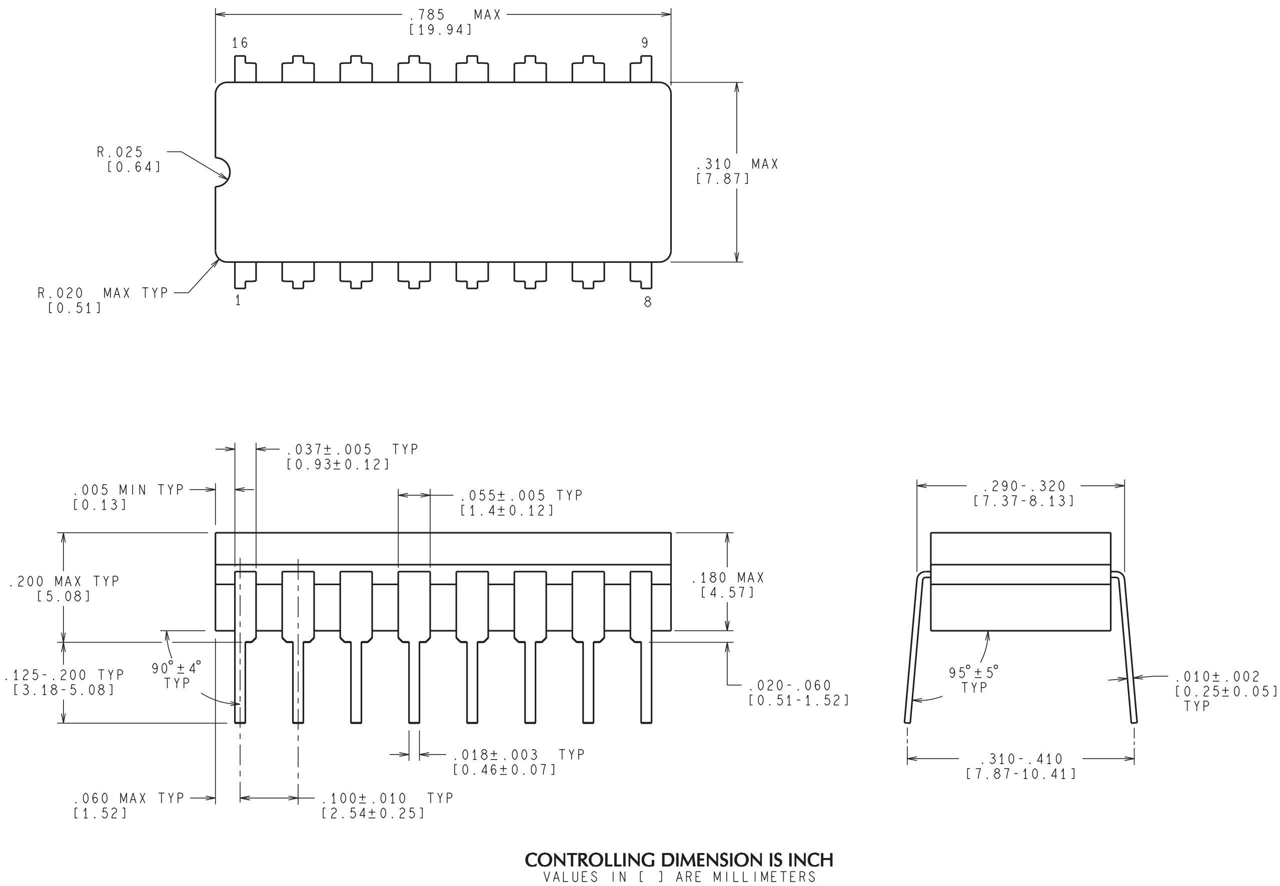
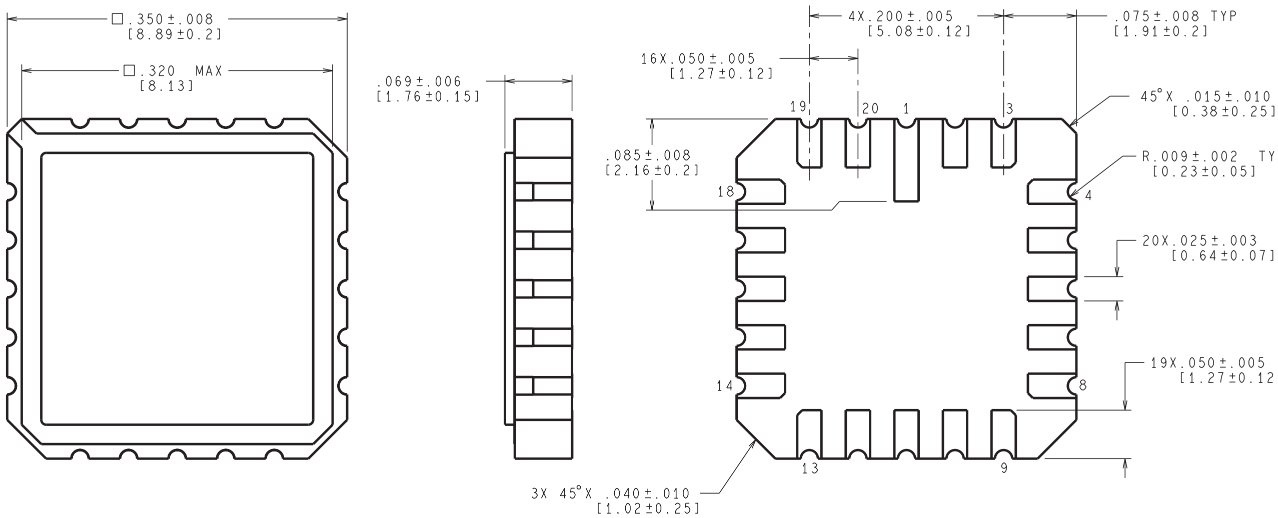


J16A (REV L)

NAJ0020A



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E20A (Rev F)

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