

## FAN6755W / FAN6755UW mWSaver™ PWM Controller

### Features

- mWSaver™ Technology Provides Industry's Best-in-Class Standby Power
  - <100mW at 25mW Load for LCDM Adaptor
  - Internal High-Voltage JFET Startup
  - Low Operating Current Maximum: 2mA
  - Adaptive Decreasing of PWM Frequency to 23KHz at Light-Load Condition, Improved Light-Load Efficiency
  - Feedback Impedance Switching During Minimum Load or No Load
- Proprietary Asynchronous Frequency Hopping Reduced EMI
- Fixed PWM Frequency: 65KHz (FAN6755W), 130KHz (FAN6755UW)
- Internal Leading-Edge Blanking
- Built-in Synchronized Slope Compensation
- Auto-Restart Protection: Feedback Open-Loop Protection (OLP), V<sub>DD</sub> Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and Line Over-Voltage Protection
- Soft Gate Drive with Clamped Output Voltage: 18V
- V<sub>DD</sub> Under-Voltage Lockout (UVLO)
- Programmable Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis
- Build-in 5ms Soft-Start Function
- Input Voltage Sensing (V<sub>IN</sub> Pin) for Brown-In/Out Protection with Hysteresis and Line Over-Voltage Protection

### Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- LCD Monitor Power Supply
- Open-Frame SMPS

### Description

This highly integrated PWM controller provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary adaptive green-mode function reduces switching frequency at light-load condition. To avoid acoustic-noise problems, the minimum PWM frequency is set above 23kHz. This green-mode function enables the power supply to meet international power conservation requirements, such as Energy Star®. With the internal high-voltage startup circuitry, the power loss caused by bleeding resistors is also eliminated. To further reduce power consumption, FAN6755W/UW uses the BiCMOS process, which allows an operating current of only 2mA. The standby power consumption can be under 100mW for most of LCD monitor power supply designs.

FAN6755W/UW integrates a frequency-hopping function that reduces EMI emission of a power supply with minimum line filters. Its built-in synchronized slope compensation achieves a stable peak-current-mode control and improves noise immunity. The proprietary, external line compensation ensures constant output power limit over a wide AC input voltage range from 90V<sub>AC</sub> to 264V<sub>AC</sub>.

FAN6755W/UW provides many protection functions. The internal feedback open-loop protection circuit protects the power supply from open feedback loop condition or output short condition. It also has line under-voltage protection (brownout protection) and over-voltage protection using an input voltage sensing pin (V<sub>IN</sub>).

FAN6755W/UW is available in a 7-pin SOP package.

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### Ordering Information

Part Number	Operating Temperature Range	Package	PWM Frequency	Packing Method
FAN6755WMY	-40 to +105°C	7-Lead, Small Outline Integrated Circuit (SOIC), Depopulated JEDEC MS-112, .150 Inch Body	65kHz	Reel & Tape
FAN6755UWY	-40 to +105°C		130kHz	Reel & Tape

### Application Diagram

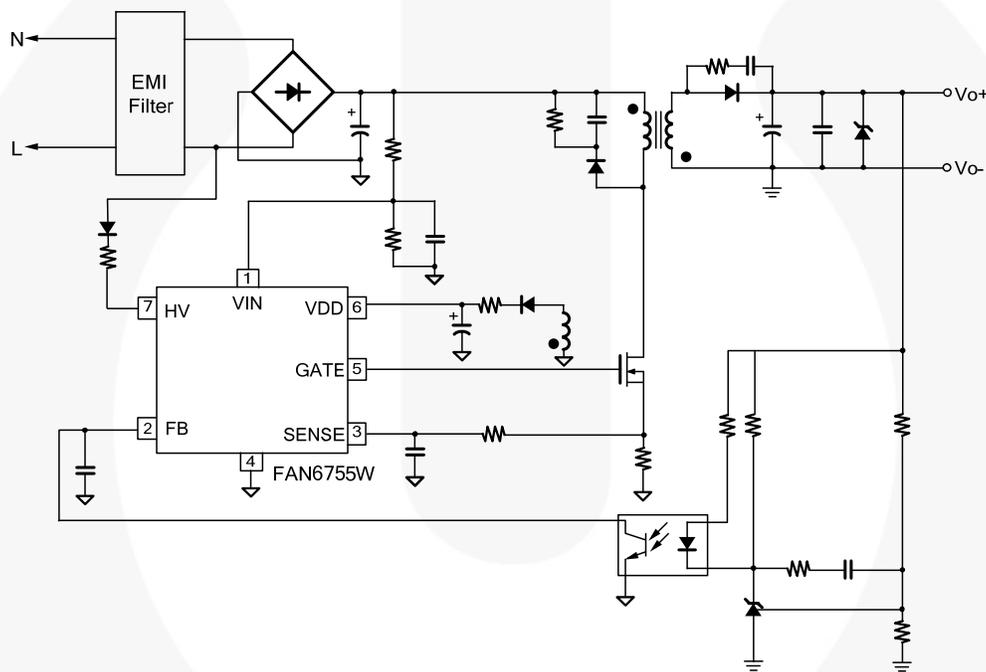


Figure 1. Typical Application



### Internal Block Diagram

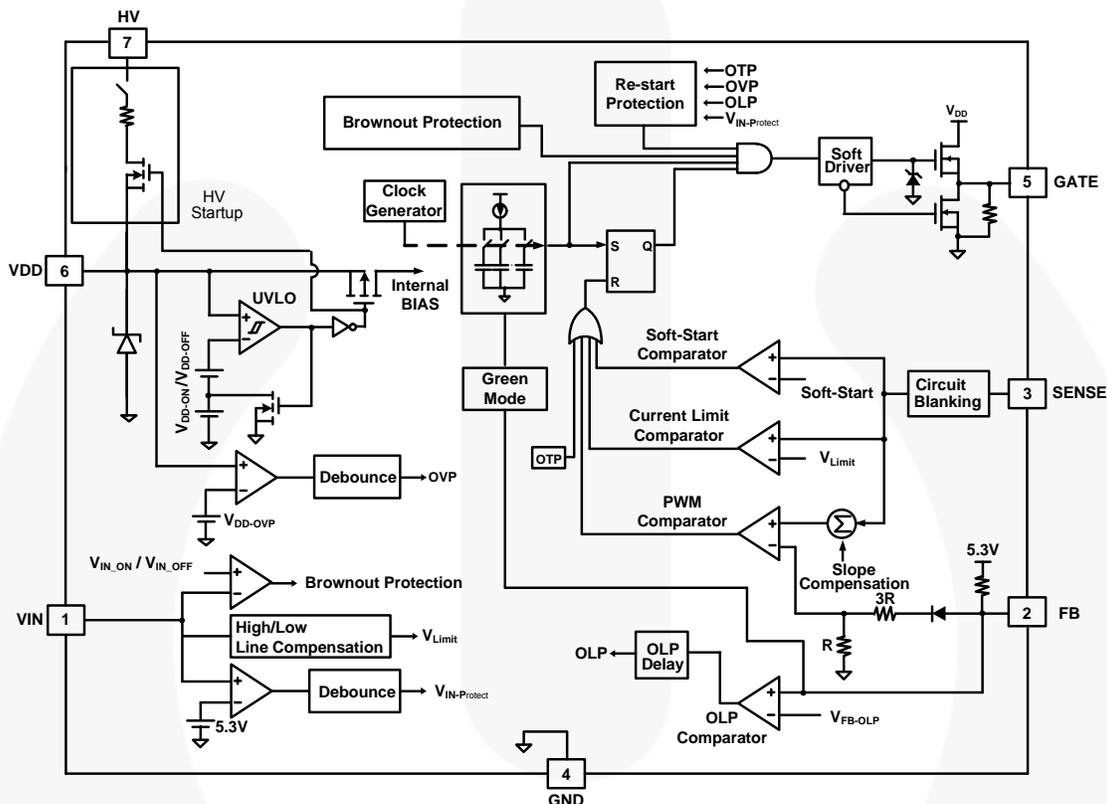
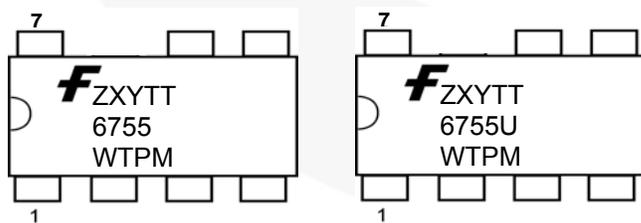


Figure 2. Internal Block Diagram

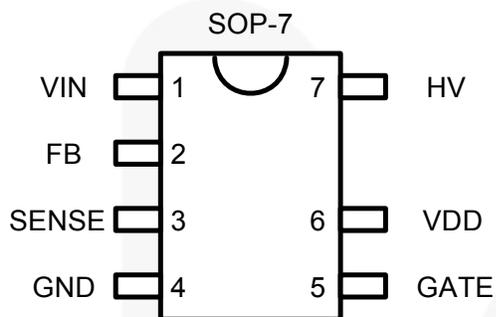
### Marking Information



Z: Plant Code  
 X: 1-Digit Year Code  
 Y: 1-Digit Week Code  
 TT: 2-Digit Die Run Code  
 T: Package Type (M:SOP)  
 P: Y=Green Package  
 M: Manufacture Flow Code

Figure 3. Top Mark

## Pin Configuration



**Figure 4. Pin Configuration (Top View)**

## Pin Definitions

Pin #	Name	Description
1	VIN	Line-voltage detection. The line-voltage detection is used for brownout protection with hysteresis. Constant output power limit over universal AC input range is also achieved using this VIN pin. It is suggested to add a low-pass filter to filter out line ripple on the bulk capacitor. Pulling VIN HIGH also triggers auto-restart protection.
2	FB	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on the SENSE pin.
3	SENSE	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
4	GND	Ground
5	GATE	The totem-pole output driver. Soft-driving waveform is implemented for improved EMI.
6	VDD	Power supply. The internal protection circuit disables PWM output as long as $V_{DD}$ exceeds the OVP trigger point.
7	HV	For startup, this pin is pulled HIGH to the line input or bulk capacitor via resistors.



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>VDD</sub>	DC Supply Voltage <sup>(1, 2)</sup>			30	V
V <sub>FB</sub>	FB Pin Input Voltage		-0.3	7.0	V
V <sub>SENSE</sub>	SENSE Pin Input Voltage		-0.3	7.0	V
V <sub>VIN</sub>	VIN Pin Input Voltage		-0.3	7.0	V
V <sub>HV</sub>	HV Pin Input Voltage			700	V
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> < 50°C)			400	mW
Θ <sub>JA</sub>	Thermal Resistance (Junction-to-Air)			150	°C/W
T <sub>J</sub>	Operating Junction Temperature		-40	+125	°C
T <sub>STG</sub>	Storage Temperature Range		-55	+150	°C
T <sub>L</sub>	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins Except HV Pin		5.5	kV
	Charged Device Model, JEDEC: JESD22-C101	All Pins Except HV Pin		2.0	

### Notes:

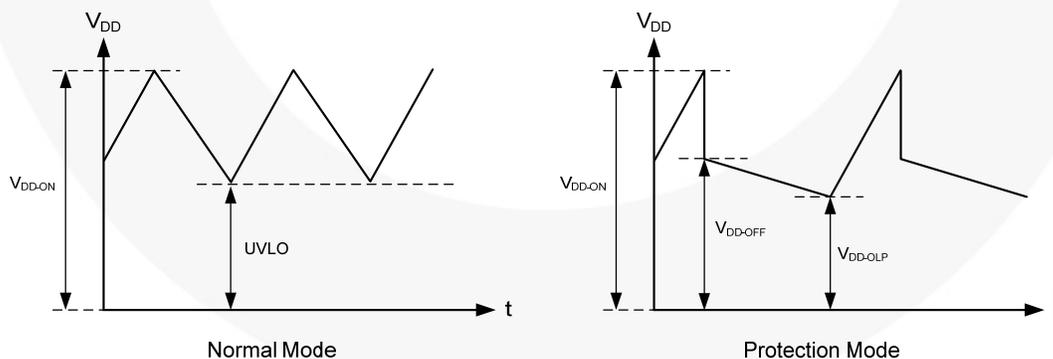
- All voltage values, except differential voltages, are given with respect to the network ground terminal.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
- ESD with HV pin: CDM=2000V (FAN6755W) or 1500V (FAN6755UW), and HBM=3500V.



## Electrical Characteristics

$V_{DD}=15V$ ,  $T_A=25^{\circ}C$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>V<sub>DD</sub> Section</b>						
$V_{OP}$	Continuously Operating Voltage	Full Load			22	V
$V_{DD-ON}$	Start Threshold Voltage		15	16	17	V
$V_{DD-OFF}$	Protection Mode		9	10	11	V
UVLO	Normal Mode		6.8	7.8	8.8	V
$I_{DD-ST}$	Startup Current	$V_{DD-ON} - 0.16V$			30	$\mu A$
$I_{DD-OP}$	Operating Supply Current	$V_{DD}=15V$ , GATE Open			2	mA
$I_{DD-OLP}$	Internal Sink Current	$V_{TH-OLP}+0.1V$	30	60	90	$\mu A$
$V_{DD-OLP}$	Threshold Voltage on $V_{DD}$ for HV JFET Turn-On		6.5	7.5	8.0	V
$V_{DD-OVP}$	$V_{DD}$ Over-Voltage Protection		25	26	27	V
$t_{D-VDDOVP}$	$V_{DD}$ Over-Voltage Protection Debounce Time		75	125	200	$\mu s$
<b>HV Section</b>						
$I_{HV}$	Supply Current Drawn from HV Pin	$V_{DC}=120V$ , $V_{DD}=10\mu F$ , $V_{DD}=0V$	2.0	3.5	5.0	mA
$I_{HV-LC}$	Leakage Current after Startup	HV=700V, $V_{DD}=V_{DD-OFF}+1V$		1	20	$\mu A$



**Figure 5. V<sub>DD</sub> Behavior**

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## Electrical Characteristics

$V_{DD}=15V$ ,  $T_A=25^{\circ}C$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>Oscillator Section</b>							
$f_{OSC}$	Frequency in Normal Mode	Center Frequency	FAN6755W	62	65	68	KHz
			FAN6755UW	124	130	136	
		Hopping Range	FAN6755W	$\pm 4.5$	$\pm 5.2$	$\pm 5.9$	
			FAN6755UW	$\pm 9$	$\pm 10.4$	$\pm 11.8$	
$f_{OSC-G}$	Green-Mode Frequency		20	23	26	KHz	
$t_{HOP}$	Hopping Period		10.00	12.00	14.00	ms	
$f_{DV}$	Frequency Variation vs. $V_{DD}$ Deviation	$V_{DD}=11V$ to $22V$			5	%	
$f_{DT}$	Frequency Variation vs. Temperature Deviation	$T_A=-40$ to $85^{\circ}C=T_J$			5	%	
<b>V<sub>IN</sub> Section</b>							
$V_{IN-OFF}$	PWM Turn-Off Threshold Voltage		0.66	0.70	0.74	V	
$V_{IN-ON}$	PWM Turn-On Threshold Voltage		$V_{IN-OFF}^{+}$ 0.17	$V_{IN-OFF}^{+}$ 0.20	$V_{IN-OFF}^{+}$ 0.23	V	
$V_{IN-Protect}$	PWM Protect Threshold Voltage		5.1	5.3	5.5	V	
$t_{VIN-Protect}$	PWM Protect Debounce Time		60	100	140	$\mu s$	
<b>Current-Sense Section</b>							
$V_{TH-P}$ at $V_{IN}=1V$	Threshold Voltage for Current Limit	$V_{IN}=1V$	0.80	0.83	0.86	V	
$V_{TH-P}$ at $V_{IN}=3V$	Threshold Voltage for Current Limit	$V_{IN}=3V$	0.67	0.70	0.73	V	
$t_{PD}$	Delay to Output			100	200	ns	
$t_{LEB}$	Leading-Edge Blanking Time	Soft-Start (FAN6755UW)	125	150	175	ns	
		Steady State	240	290	340		
$t_{SS}$	Period During Soft-Start Time	Startup Time	4.0	5.5	7.0	ms	

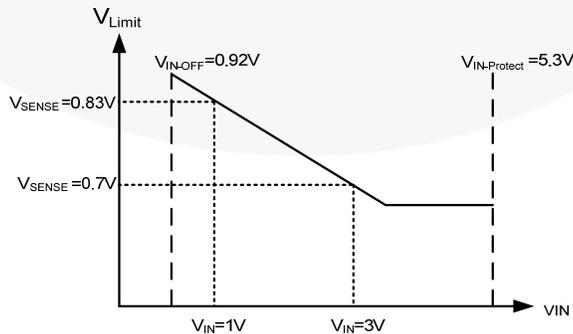


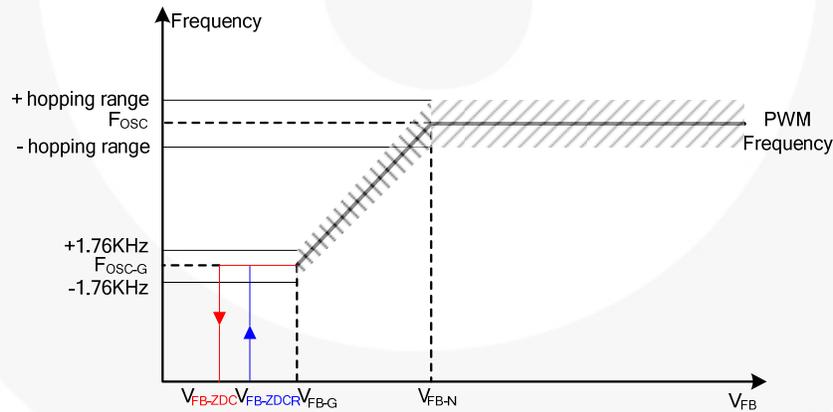
Figure 6.  $V_{IN}$  vs.  $V_{SENSE}$

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## Electrical Characteristics

$V_{DD}=15V$ ,  $T_A=25^\circ C$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Feedback Input Section</b>						
$A_V$	Input Voltage to Current-Sense Attenuation		1/4.5	1/4.0	1/3.5	V/V
$Z_{FB}$	Input Impedance	$V_{FB}=4V$	10	15	19	k $\Omega$
$V_{FB-OPEN}$	Output High Voltage	FB Pin Open	5.1	5.3	5.5	V
$V_{FB-OLP}$	FB Open-Loop Trigger Level		4.4	4.6	4.8	V
$t_{D-OLP}$	Delay Time of FB Pin Open-loop Protection		45.0	62.5	70.0	ms
$V_{FB-N}$	Green-Mode Entry FB Voltage		2.8	3.0	3.2	V
$V_{FB-G}$	Green-Mode Ending FB Voltage			$V_{FB-N} - 0.6$		V
$V_{FB-ZDCR}$	FB Threshold Voltage for Zero-Duty Recovery		1.6	1.8	2.0	V
$V_{FB-ZDC}$	FB Threshold Voltage for Zero-Duty		1.4	1.6	1.8	V
$V_{FB-ZDCR} - V_{FB-ZDC}$	ZDC Hysteresis		0.12	0.15	0.19	V



**Figure 7.  $V_{FB}$  vs. PWM Frequency**

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## Electrical Characteristics

$V_{DD}=15V$ ,  $T_A=25^{\circ}C$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>GATE Section</b>						
$DCY_{MAX}$	Maximum Duty Cycle		60	75	90	%
$V_{GATE-L}$	Gate Low Voltage	$V_{DD}=15V$ , $I_O=50mA$			1.5	V
$V_{GATE-H}$	Gate High Voltage	$V_{DD}=12V$ , $I_O=50mA$	8			V
$t_r$	Gate Rising Time	$V_{DD}=15V$ , $C_L=1nF$		100		ns
$t_f$	Gate Falling Time	$V_{DD}=15V$ , $C_L=1nF$		30		ns
$I_{GATE-SOURCE}$	Gate Source Current	$V_{DD}=15V$ , $GATE=6V$		700		mA
$V_{GATE-CLAMP\_1}$	Gate Output Clamping Voltage	$V_{DD}=22V$			18	V
<b>Over-Temperature Protection Section (OTP)</b>						
$T_{OTP}$	Protection Junction Temperature <sup>(4,6)</sup>			140		$^{\circ}C$
$T_{Restart}$	Restart Junction Temperature <sup>(5,6)</sup>			$T_{OTP}-25$		$^{\circ}C$

### Notes:

- When activated, the output is disabled and the latch is turned off.
- The threshold temperature for enabling the output again and resetting the latch after over-temperature protection has been activated.
- These parameters are guaranteed by design.



## Typical Performance Characteristics

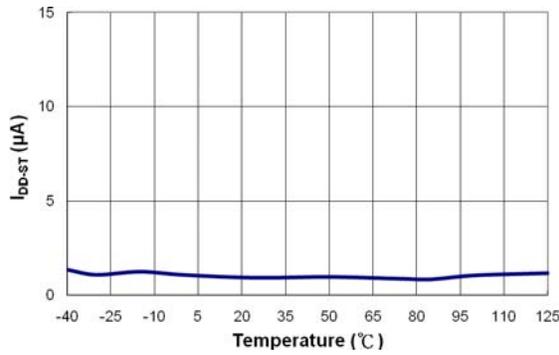


Figure 8. Startup Current ( $I_{DD-ST}$ ) vs. Temperature

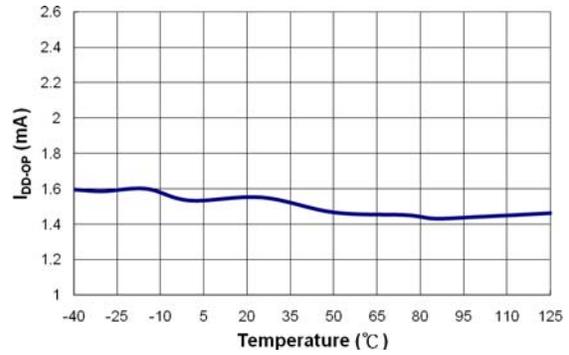


Figure 9. Operation Supply Current ( $I_{DD-OP}$ ) vs. Temperature

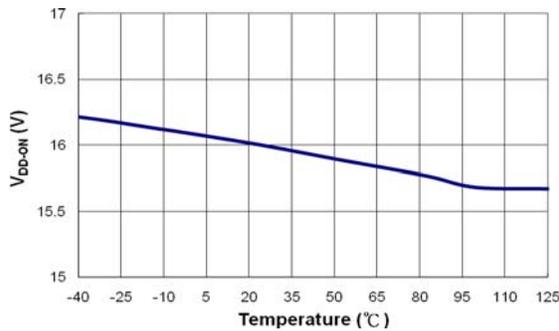


Figure 10. Start Threshold Voltage ( $V_{DD-ON}$ ) vs. Temperature

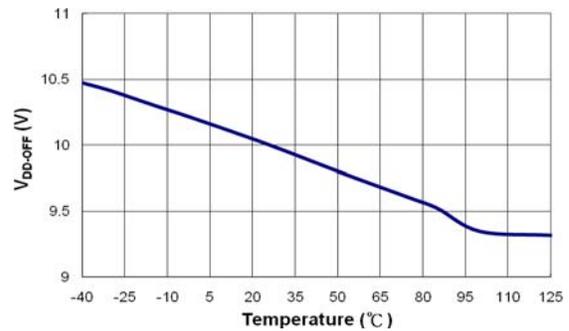


Figure 11. Minimum Operating Voltage ( $V_{DD-OFF}$ ) vs. Temperature

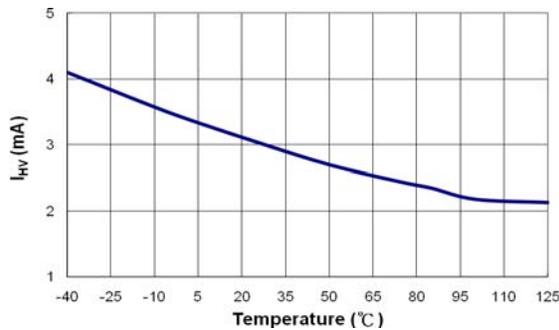


Figure 12. Supply Current Drawn from HV Pin ( $I_{HV}$ ) vs. Temperature

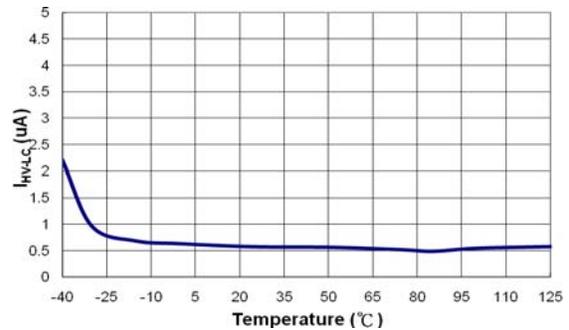


Figure 13. HV Pin Leakage Current After Startup ( $I_{HV-LC}$ ) vs. Temperature

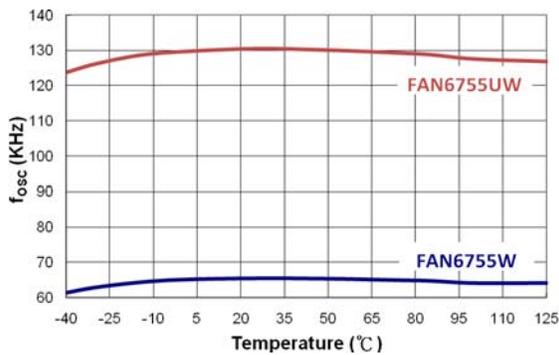


Figure 14. Frequency in Normal Mode ( $f_{osc}$ ) vs. Temperature

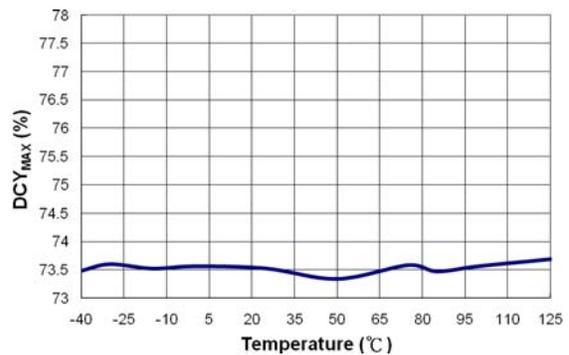


Figure 15. Maximum Duty Cycle ( $DCY_{MAX}$ ) vs. Temperature

Typical Performance Characteristics

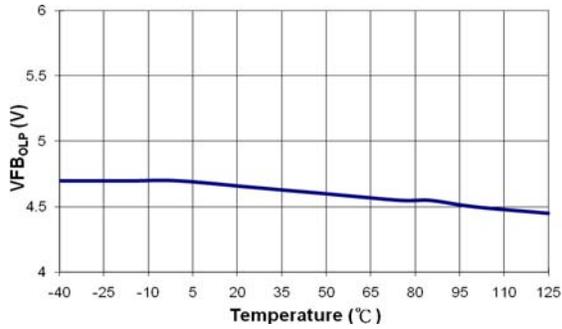


Figure 16. FB Open-Loop Trigger Level ( $V_{FB-OLP}$ ) vs. Temperature

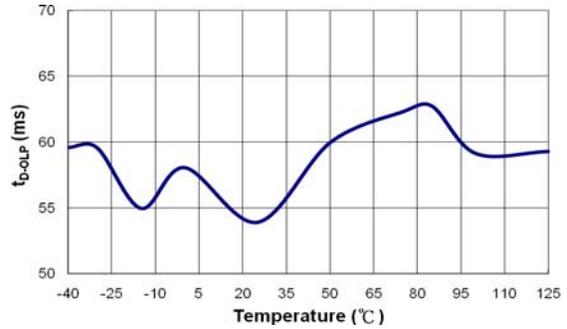


Figure 17. Delay Time of FB Pin Open-Loop Protection ( $t_{D-OLP}$ ) vs. Temperature

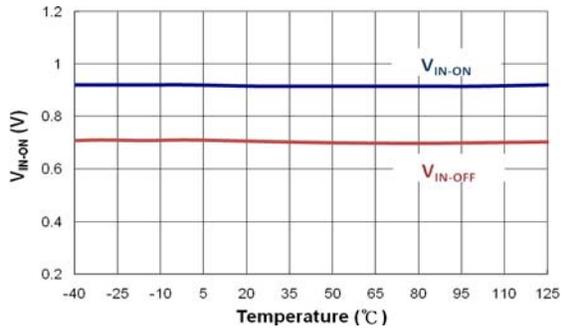


Figure 18. PWM Turn-Off Threshold Voltage ( $V_{IN-OFF}$  &  $V_{IN-ON}$ ) vs. Temperature

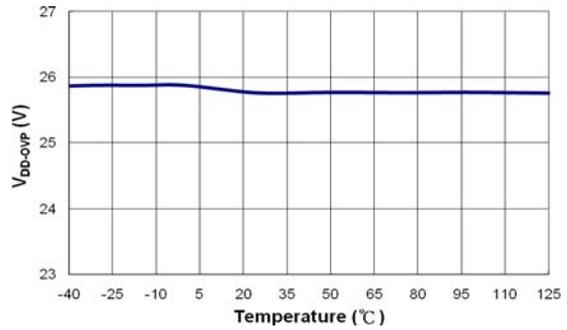


Figure 19.  $V_{DD}$  Over-Voltage Protection ( $V_{DD-OVP}$ ) vs. Temperature

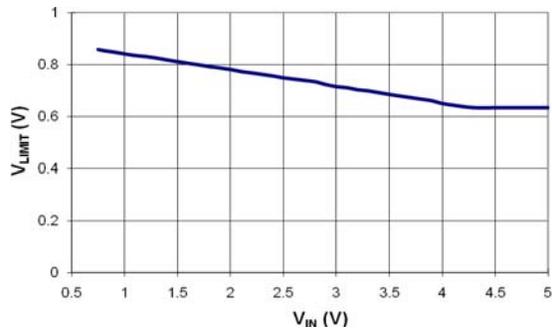


Figure 20.  $V_{IN}$  vs.  $V_{LIMIT}$

## Functional Description

### Startup Current

For startup, the HV pin is connected to the line input (1N4007 / 100KΩ recommended) or bulk capacitor through a resistor,  $R_{HV}$ . Startup current drawn from pin HV (typically 3.5mA) charges the hold-up capacitor through the diode and resistor. When the  $V_{DD}$  capacitor level reaches  $V_{DD-ON}$ , the startup current switches off. At this moment, the  $V_{DD}$  capacitor only supplies the FAN6755W/UW to maintain  $V_{DD}$  before the auxiliary winding of the main transformer to provide the operating current.

### Operating Current

Operating current is around 2mA. The low operating current enables better efficiency and reduces the requirement of  $V_{DD}$  hold-up capacitance.

### Green-Mode Operation

The proprietary green-mode function provides an off-time modulation to reduce the switching frequency in light-load and no-load conditions. The on time is limited for better abnormal or brownout protection.  $V_{FB}$ , which is derived from the voltage feedback loop, is taken as the reference. Once  $V_{FB}$  is lower than the threshold voltage, switching frequency is continuously decreased to the minimum green-mode frequency of around 23KHz.

### Current Sensing / PWM Current Limiting

Peak-current-mode control is utilized to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current sense signal and  $V_{FB}$ , the feedback voltage. When the voltage on the SENSE pin reaches around  $V_{COMP}=(V_{FB}-0.6)/4$ , a switch cycle is terminated immediately.  $V_{COMP}$  is internally clamped to a variable voltage around 0.83V for output power limit.

### Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

### Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16V and 7.8V in normal mode. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable the IC. The hold-up capacitor continues to supply  $V_{DD}$  before the energy can be delivered from auxiliary winding of the main transformer.  $V_{DD}$  must not drop below 7.8V during startup. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply  $V_{DD}$  during startup.

### Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

### Soft-Start

For many applications, it is necessary to minimize the inrush current at startup. The built-in 5.5ms soft-start circuit significantly reduces the startup current spike and output voltage overshoot.

### Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. FAN6755W/UW inserts a synchronized positive-going ramp at every switching cycle.

### Constant Output Power Limit

For constant output power limit over universal input-voltage range, the peak-current threshold is adjusted by the voltage of the VIN pin. Since the VIN pin is connected to the rectified AC input line voltage through the resistive divider, a higher line voltage generates a higher  $V_{IN}$  voltage. The threshold voltage decreases as  $V_{IN}$  increases, making the maximum output power at high-line input voltage equal to that at low-line input. The value of R-C network should not be so large that it affects the power limit (shown in Figure 21). R and C should be less than 100Ω and 470pF, respectively.

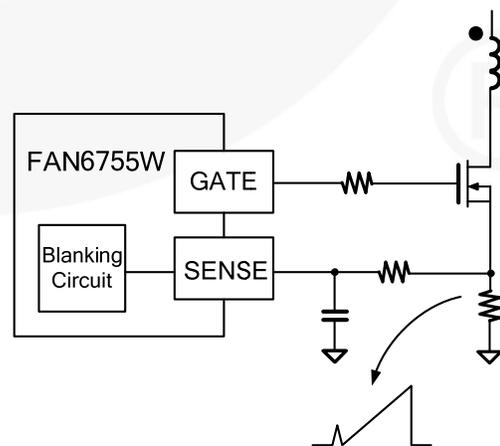


Figure 21. Current-Sense R-C Filter

## V<sub>DD</sub> Over-Voltage Protection

V<sub>DD</sub> over-voltage protection prevents damage due to abnormal conditions. Once the V<sub>DD</sub> voltage is over the over-voltage protection voltage (V<sub>DD-OVP</sub>), and lasts for t<sub>D-VDDOVP</sub>, the PWM pulses are disabled. When the V<sub>DD</sub> voltage drops below the UVLO, PWM pulses start again. Over-voltage conditions are usually caused by open feedback loops.

## Brownout Protection

Since the VIN pin is connected through a resistive divider to the rectified AC input line voltage, it can also be used for brownout protection. If V<sub>IN</sub> is less than 0.7V, the PWM output is shut off. When V<sub>IN</sub> reaches over 0.9V, the PWM output is turned on again. The hysteresis window for ON/OFF is around 0.2V. The brownout voltage setting is determined by the potential divider formed with R<sub>Upper</sub> and R<sub>Lower</sub>. Equations to calculate the resistors are shown below:

$$V_{IN} = \frac{R_{Lower}}{R_{Lower} + R_{Upper}} \times V_{AC} \sqrt{2}, (\text{unit} = V) \quad (1)$$

## Thermal Overload Protection

Thermal overload protection limits total power dissipation. When the junction temperature exceeds T<sub>J</sub> = +135°C, the thermal sensor signals the shutdown logic and turns off most of the internal circuitry. The thermal sensor turns internal circuitry on again after the IC's junction temperature drops by 25°C. Thermal overload protection is designed to protect the FAN6755W/UW in the event of a fault condition. For continual operation, do not exceed the absolute maximum junction temperature of T<sub>J</sub> = +150°C.

## Limited Power Control

The FB voltage is saturated HIGH when the power supply output voltage drops below its nominal value and shut regulator (KA431) does not draw current through the opto-coupler. This occurs when the output feedback loop is open or output is short circuited. If the FB voltage is higher than a built-in threshold for longer than t<sub>D-OLP</sub>, PWM output is turned off. As PWM output is turned off, V<sub>DD</sub> begins decreasing since no more energy is delivered from the auxiliary winding.

When V<sub>DD</sub> goes below the turn-off threshold (~7.5V), the controller is totally shut down. V<sub>DD</sub> is charged up to the turn-on threshold voltage of 16V through the startup resistor until PWM output is restarted. This protection feature continues as long as the over loading condition persists. This prevents the power supply from overheating due to overloading conditions.

## Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6755W/UW, and increasing the power MOS gate resistance improve performance.



Applications Information

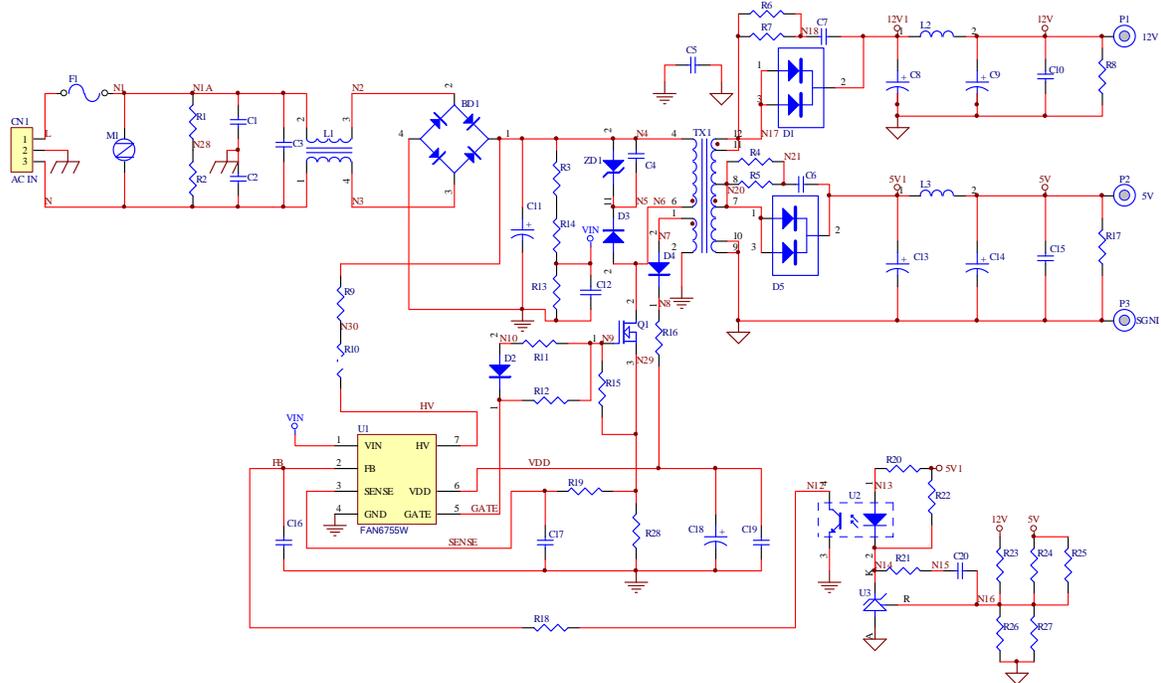


Figure 22. 44W Flyback 12V/2A, 5V/4A Application Circuit

## Build of Materials

Designator	Part Type	Designator	Part Type
BD1	BD 4A/600V	Q1	MOS 9A/600V
C1	YC 2200pF/Y1	R1	R 1.5M $\Omega$ 1/4W
C2	YC 2200pF/Y1	R2	R 1.5M $\Omega$ 1/4W
C3	XC 0.33 $\mu$ F/300V	R3	R 10M $\Omega$ 1/4W
C4	NC	R4, R5, R6, R7	R 47 $\Omega$ 1/4W
C5	YC 2200pF/Y1	R8, R17, R25, R27	NC
C6	CC 2200pF/100V	R9	R 50K $\Omega$ 1/4W
C7	CC 1000pF/100V	R10	R 50K $\Omega$ 1/4W
C8	EC 1000 $\mu$ F/25V	R11	R 0 $\Omega$ 1/8W
C9	EC 470 $\mu$ F/25V	R12	R 47 $\Omega$ 1/8W
C10	CC 100pF/50V	R13	R 100K $\Omega$ 1/8W
C11	EC 100 $\mu$ F/400V	R14	R 0 $\Omega$ 1/4W
C12	C 1 $\mu$ F/50V	R15	R 10K $\Omega$ 1/8W
C13	EC 1000 $\mu$ F/10V	R16	R 1 $\Omega$ 1/8W
C14	EC 470 $\mu$ F/10V	R18	R 0 $\Omega$ 1/8W
C15	CC 100pF/50V	R19	R 100 $\Omega$ 1/8W
C16	C 1nF/50V	R20	R 1K $\Omega$ 1/8W
C17	C 470pF/50V	R21	R 4.7K $\Omega$ 1/8W
C18	EC 47 $\mu$ F/50V	R22	R 7.5K $\Omega$ 1/8W
C19	C 0.01 $\mu$ F/50V	R23	R 120K $\Omega$ 1/8W
C20	C 0.1 $\mu$ F/50V	R24	R 15K $\Omega$ 1/8W
D1	FYP1010	R26	R 10K $\Omega$ 1/8W
D2	1N4148	R28	R 0.43 $\Omega$ 2W
D3	FR107	TX1	800 $\mu$ H(ERL-28)
D4	FR103	U1	IC FAN6755W
D5	FYP1010	U2	IC PC817
ZD1	P6KE150A	U3	IC TL431
F1	FUSE 4A/250V		
M1	VZ 9G		
L1	13mH		
L2	Inductor (2 $\mu$ H)		
L3	Inductor (2 $\mu$ H)		

Physical Dimensions

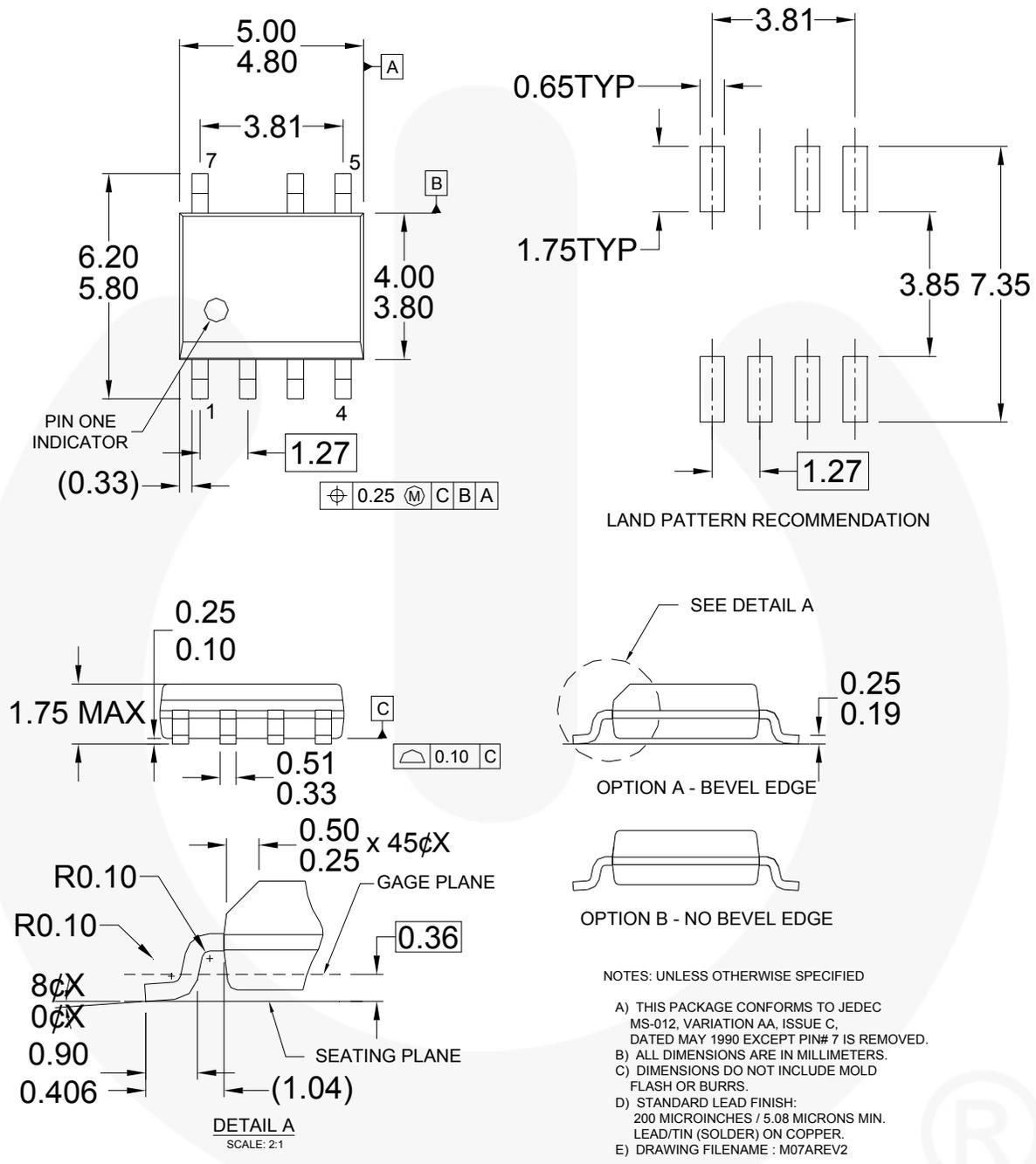


Figure 23. 7-Lead, Small Outline Package (SOP)

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