FAIRCHILD SEMICONDUCTOR®

May 2009

FAN6861
Low-Cost, Highly Integrated, Green-Mode PWM Controller for Peak Power Management

Features

- Low Startup Current: 15µA Maximum
- Green-Mode and Burst-Mode Operation for Low Standby Power Consumption
- Internal Soft Start: 10ms
- Frequency Hopping for EMI Reduction
- Peak-Current Mode Control with Cycle-by-Cycle Current Limiting
- Constant Output Power Limit (Full AC Input Range)
- Built-in Slope Compensation
- Two-Level Over-Current Protection (OCP) with Delayed Shutdown (780ms) for Peak Power Management
- Open-Loop / Over-Load Protection (OLP)
- V_{DD} Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)

Applications

- Switched Mode Power Supply (SMPS) with Motor Load; such as for printer, scanner, motor drivers, etc.
- AC/DC Adapters
- Open-Frame SMPS

Description

Highly integrated PWM controller, FAN6861 is optimized for applications with motor load; such as printer and scanner, which inherently impose some kind of overload condition on the power supply during acceleration mode. The two-level OCP function allows the SMPS to stably deliver peak power during the motor acceleration mode without causing premature shutdown and while protecting the SMPS from overload condition.

The green-mode and burst-mode functions with a low operating current (2.2mA maximum in green mode) maximize the light load efficiency so that the power supply can meet most stringent standby power regulations.

The frequency-hopping function helps reduce electro-magnetic interference (EMI) of a power supply by spreading the energy over a wider frequency range.

The constant power limit function; minimizes the components stress in abnormal condition and helps designer to optimize the power stage more easily.

Many protection functions such; as OCP, OLP, OVP and OTP, are fully integrated into FAN6861, which improves the SMPS reliability without increasing the system cost.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FAN6861TY	-40 to +105°C	Green	SSOT-6	Tape & Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application

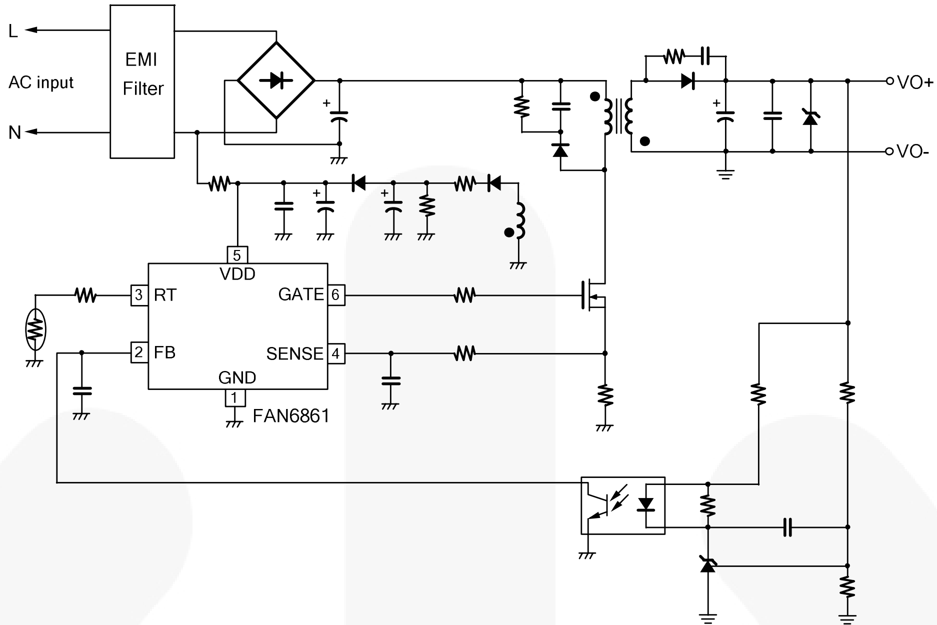

Figure 1. Typical Application

Block Diagram

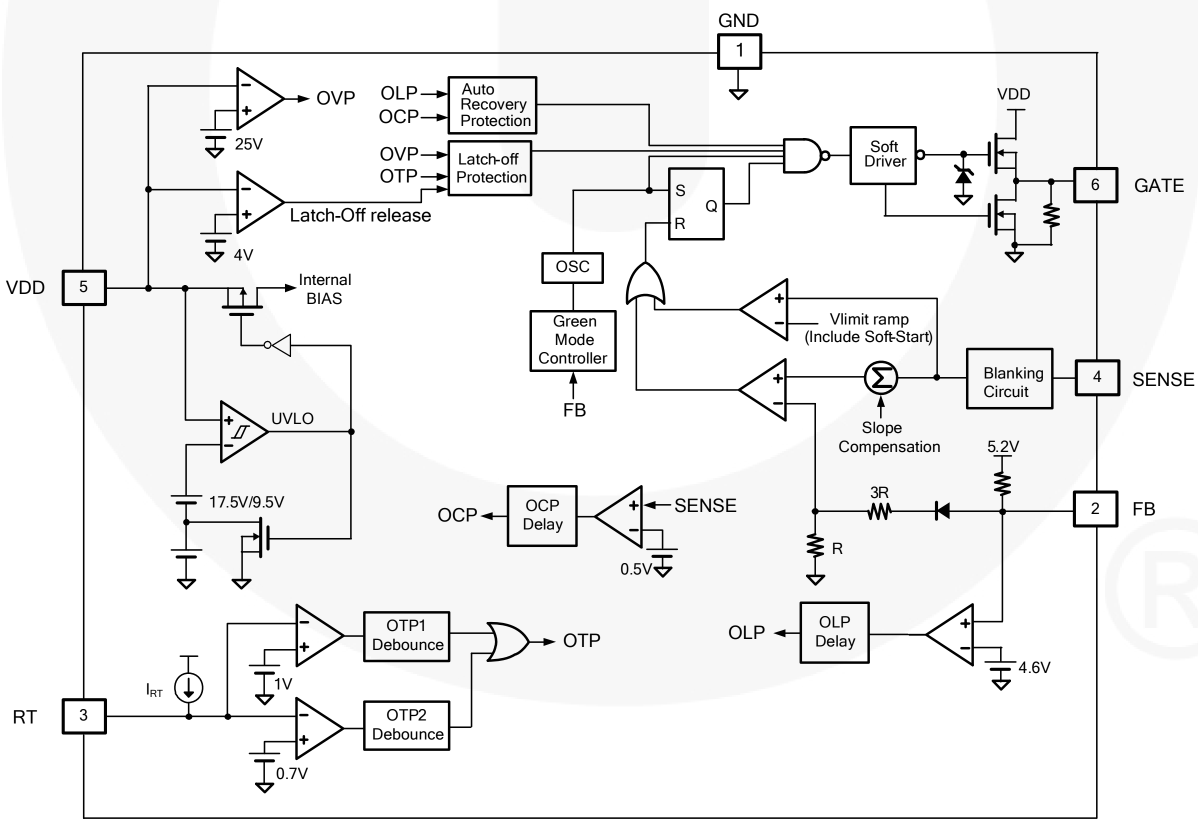

Figure 2. Block Diagram

Marking Information

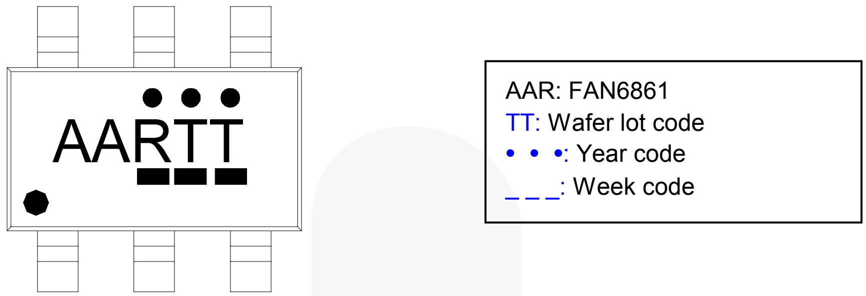

Figure 3. Top Mark

Pin Configuration

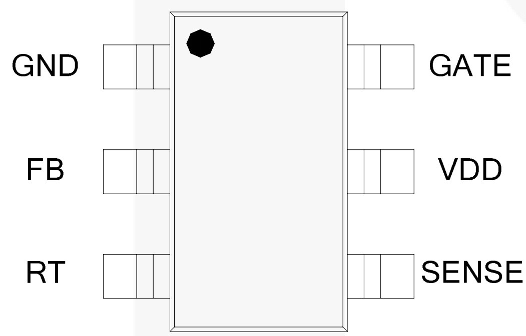

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	Ground.
2	FB	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin is higher than 4.6V for longer than 780ms, the overload protection is triggered and PWM output is disabled.
3	RT	This pin is for programmable over-temperature protection. An external NTC thermistor is connected between this pin and GND pin. Once the voltage of this pin drops below a threshold of 0.7V, PWM output is disabled.
4	SENSE	This pin is for current sense. This pin senses the voltage across a resistor. The voltage of this pin is compared with the feedback information determining the PWM duty cycle.
5	VDD	This pin is the positive supply voltage input.
6	GATE	The totem-pole output driver to drive the gate of power MOSFET. Soft driving waveform is implemented to reduce EMI.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage			30	V
V_L	Input Voltage to FB, SENSE, VIN, RT,RI Pin		-0.3	7.0	V
P_D	Power Dissipation at T_A<50°C			300	mW
Θ_{JC}	Thermal Resistance (Junction-to-Case)			208.4	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature, Wave Soldering, 10 Seconds			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4.5	kV
		Charge Device Model, JESD22-C101		1.0	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD} = 15V and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{DD-OP}	Continuously Operating Voltage				24	V
V_{DD-ON}	Turn-On Threshold Voltage		16.5	17.5	18.5	V
V_{DD-OFF}	Turn-Off Voltage		8.5	9.5	10.5	V
V_{DD-SCP}	Threshold Voltage for Output Short-Circuit Protection (SCP)		V_{DD-OFF} +0.5	V_{DD-OFF} +1.0	V_{DD-OFF} +1.5	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Latch-Off)		24	25	26	V
V_{DD-LH}	Threshold Voltage for Latch-Off Release		3	4	5	V
I_{DD-ST}	Startup Current	V_{TH-ON} – 0.16V		8	15	μA
I_{DD-OP}	Normal Operating Supply Current	With 1nF Load on Gate, $V_{FB} \geq V_{FB-N}$		3	4	mA
I_{DD-BM}	Green-Mode Operating Supply Current	GATE Open, $V_{FB} = V_{FB-G}$			2.2	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Latch-Off)		24	25	26	V
$t_{D-VDDOVP}$	V_{DD} OVP Debounce Time		100	170	240	μs
I_{DD-LH}	Latch-Off Holding Current	V_{DD} = 5V	25	40	55	μA
Feedback Input Section						
A_V	Input Voltage to Current Sense Attenuation	At Green Mode	1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Input Impedance		14	16	18	kΩ
V_{FBO}	FB Pin Open Voltage		5.0	5.2	5.4	V
V_{FB-OLP}	Threshold Voltage for Open-loop Protection		4.3	4.6	4.9	V
t_{D-OLP}	Open-Loop Protection Delay Time		700	780	860	ms
t_{D-SCP}	Short-Circuit Protection Delay Time		20	25	30	ms
Current Sense Section						
t_{PD}	Delay to Output			100	250	ns
t_{LEB}	Leading-Edge Blanking Time		270	360		ns
V_{STHFL}	Flat Threshold Voltage for Current Limit	Duty > 51%	0.85	0.89	0.93	V
V_{STHVA}	Valley Threshold Voltage for Current Limit	Duty = 0%	0.65	0.70	0.75	V
V_{OCP}	OCP Trigger Level		0.47	0.50	0.53	V
V_{SLOPE}	Slope Compensation	Duty = DCY_{MAX}	0.30	0.33	0.36	V
t_{SS}	Soft-Start Time		7.5	10.0	12.5	ms
t_{D-OCP}	FB Pin Protection Delay Time for Peak Loading		700	780	860	ms

Continued on following page…

Electrical Characteristics (Continued)

V_{DD} = 15V and T_A = 25°C, unless otherwise noted.

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
Oscillator Section							
f_{OSC}	Normal PWM Frequency	Center Frequency	$V_{FB} > V_{FB-N}$	60	65	70	kHz
		Jitter Range	$V_{FB} \geq V_{FB-N}$	±3.7	±4.2	±4.7	
			$V_{FB} = V_{FB-G}$	±1.27	±1.45	±1.63	
t_{hop-1}	Jitter Period 1		$V_{FB} \geq V_{FB-N}$	3.9	4.4	4.9	ms
t_{hop-3}	Jitter Period 3		$V_{FB} = V_{FB-G}$	10.2	11.5	12.8	ms
f_{OSC-G}	Green-Mode Minimum Frequency			18.0	22.5	25.0	kHz
V_{FB-N}	Beginning of Green-On Mode at FB Level	Pin, FB Voltage		2.60	2.85	3.10	V
V_{FB-G}	Beginning of Green-Off Mode at FB Level	Pin, FB Voltage		2.0	2.2	2.4	V
S_G	Slope for Green-Mode Modulation				65		Hz/mV
V_{FB-ZDC}	FB Threshold Voltage for Zero-duty			1.7	1.9	2.1	V
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD} = 11.5V to 20V	0	0.02	2.00	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A = -30 to 85°C			2	%
PWM Output Section							
DCY_{MAX}	Maximum Duty Cycle			65	70	75	%
V_{OL}	Output Voltage LOW		V_{DD} = 15V, I_O = 50mA			1.5	V
V_{OH}	Output Voltage HIGH		V_{DD} = 12V, I_O = 50mA	8			V
t_R	Rising Time		GATE = 1nF		230		ns
t_F	Falling Time		GATE = 1nF		30		ns
V_{CLAMP}	Gate Output Clamping Voltage		V_{DD} = 20V	15.00	16.75	18.50	V
Over-Temperature Protection (OTP) Section							
I_{RT}	Output Current of RT Pin			90	99	108	µA
V_{RTO}	RT Pin Open Voltage				3.7		V
V_{OTP1}	Threshold Voltage for Over-Temperature Protection			0.92	1.00	1.08	V
$t_{DOTP-LATCH}$	Over-Temperature Latch-Off Debounce		$V_{FB} = V_{FB-N}$	15	17	19	ms
			$V_{FB} = V_{FB-G}$	40	51	62	
V_{OTP2}	Second Threshold Voltage for Over-Temperature Protection			0.65	0.70	0.75	V
$t_{DOTP2-LATCH}$	Second Over-Temperature Latch-Off Debounce			50	100	150	µs

Electrical Characteristics (Continued)

V_{DD} = 15V and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle		65	70	75	%
V_{OL}	Output Voltage LOW	V_{DD} = 15V, I_O = 50mA			1.5	V
V_{OH}	Output Voltage HIGH	V_{DD} = 12V, I_O = 50mA	8			V
t_R	Rising Time	GATE = 1nF		230		ns
t_F	Falling Time	GATE = 1nF		30		ns
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD} = 20V	15.00	16.75	18.50	V
Over-Temperature Protection (OTP) Section						
I_{RT}	Output Current of RT Pin		90	99	108	µA
V_{RTO}	RT Pin Open Voltage			3.7		V
V_{OTP1}	Threshold Voltage for Over-Temperature Protection		0.92	1.00	1.08	V
$t_{DOTP-LATCH}$	Over-Temperature Latch-Off Debounce	$V_{FB} = V_{FB-N}$	15	17	19	ms
		$V_{FB} = V_{FB-G}$	40	51	62	ms
V_{OTP2}	Second Threshold Voltage for Over-Temperature Protection		0.65	0.70	0.75	V
$t_{DOTP2-LATCH}$	Second Over-Temperature Latch-Off Debounce		50	100	150	µs

Typical Performance Characteristics

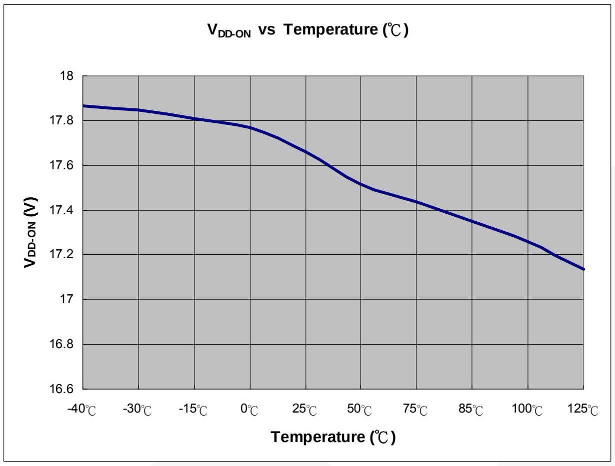

Figure 5. Turn-On Threshold Voltage ($V_{DD\text{-}ON}$) vs. Temperature

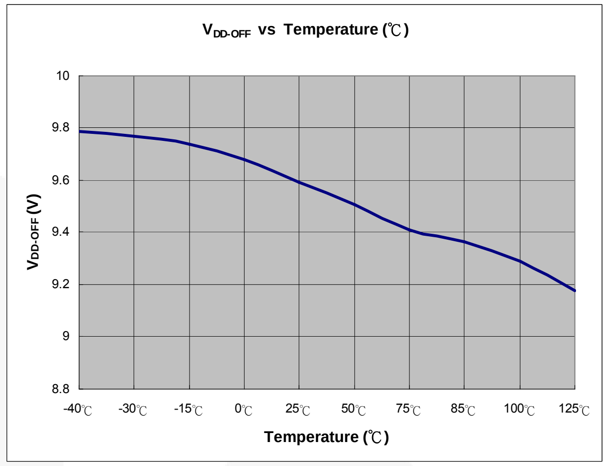

Figure 6. Turn-Off Threshold Voltage ($V_{DD\text{-}OFF}$) vs. Temperature

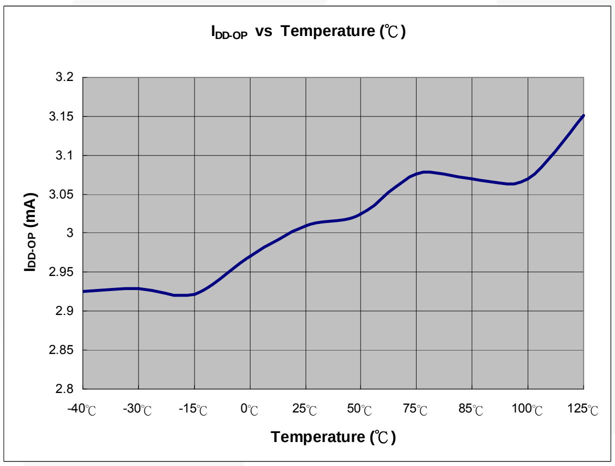

Figure 7. Operating Current ($I_{DD\text{-}OP}$) vs. Temperature

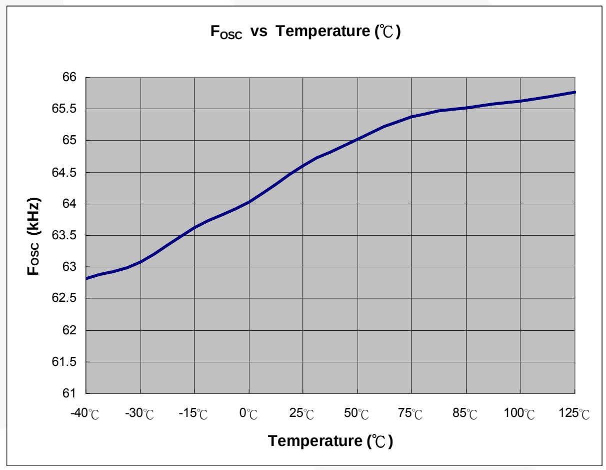

Figure 8. Normal PWM Frequency (f_{OSC}) vs. Temperature

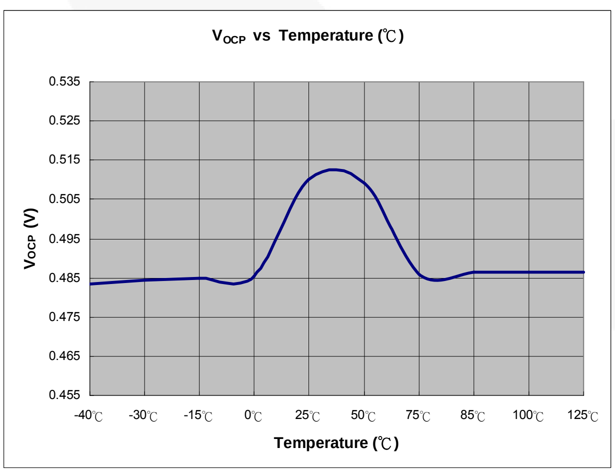

Figure 9. OCP Trigger Level (V_{OCP}) vs. Temperature

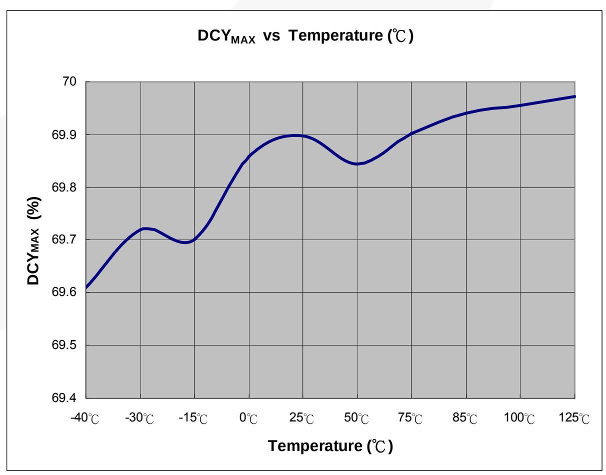

Figure 10. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Typical Performance Characteristics

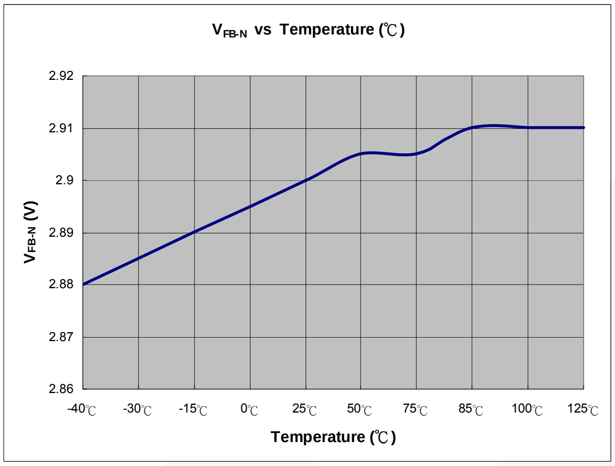

Figure 11. FB Threshold Voltage For Frequency Reduction (V_{FB-N}) vs. Temperature

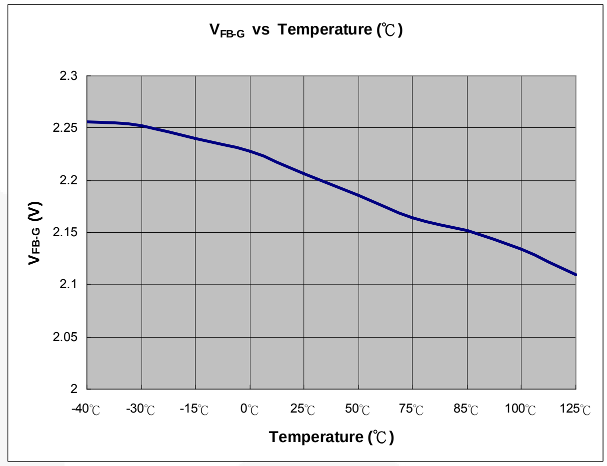

Figure 12. FB Voltage at f_{OSC-G} (V_{FB-N}) vs. Temperature

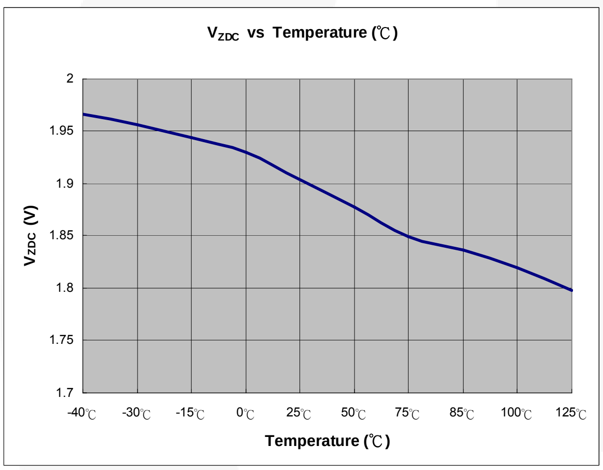

Figure 13. FB Threshold Voltage for Zero Duty (V_{FB-ZDC}) vs. Temperature

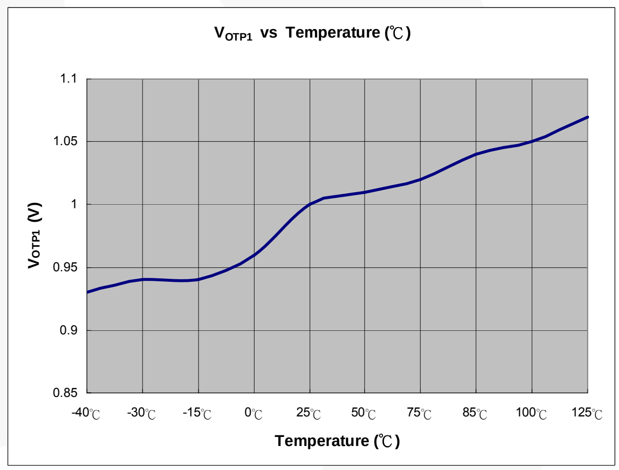

Figure 14. Threshold Voltage for Over-Temperature Protection (V_{OTP1}) vs. Temperature

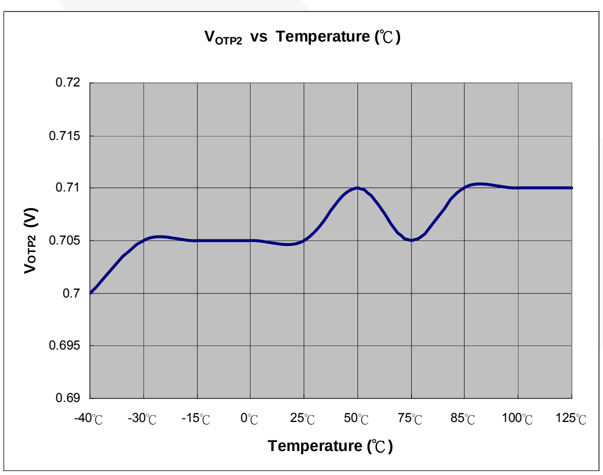

Figure 15. Second Threshold Voltage for Over-Temperature Protection (V_{OPT2}) vs. Temperature

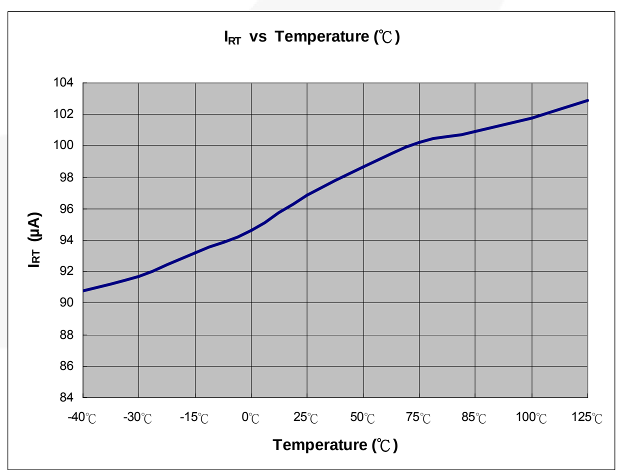

Figure 16. Output Current of RT Pin (I_{RT}) vs. Temperature

Operation Description

Startup Operation

Figure 17 shows the typical startup circuit and transformer auxiliary winding for FAN6861 application. Before FAN6861 begins switching operation, it consumes only startup current (typically 8µA) and the current supplied through the startup resistor charges the V_{DD} capacitor (C_{DD}). When V_{DD} reaches turn-on voltage of 17.5V (V_{DD-ON}), FAN6861 begins switching and the current consumed increases to 3mA. Then, the power required is supplied from the transformer auxiliary winding. The large hysteresis of V_{DD} (8V) provides more holdup time, which allows using small capacitor for V_{DD}. The startup resistor is typically connected to AC line for a fast reset of latch protection.

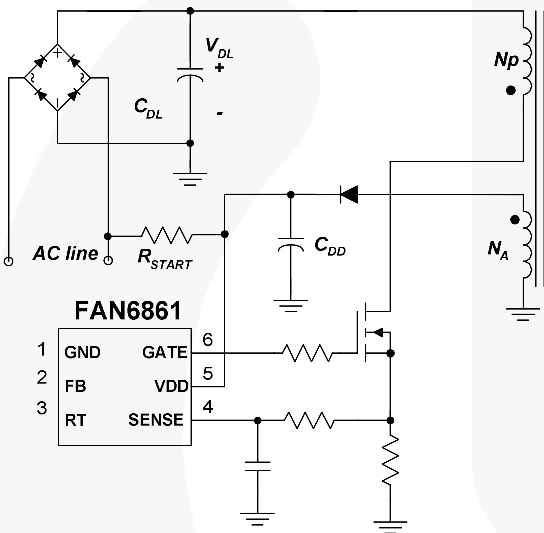

Figure 17. Startup Circuit

Green-Mode Operation

The FAN6861 uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 18, such that the switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is 65KHz. Once V_{FB} decreases below V_{FB-N} (2.85V), the PWM frequency starts to linearly decrease from 65KHz to 22kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.2V), the switching frequency is fixed at 22.5kHz and FAN6861 enters into deep green mode, where the operating current reduces to 2.2mA (maximum), further reducing the standby power consumption. As V_{FB} decreases below V_{FB-ZDC} (1.9V), FAN6861 enters into burst-mode operation. When V_{FB} drops below V_{FB-ZDC}, FAN6861 stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above V_{FB-ZDC}, switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss in standby mode, as shown in Figure 19.

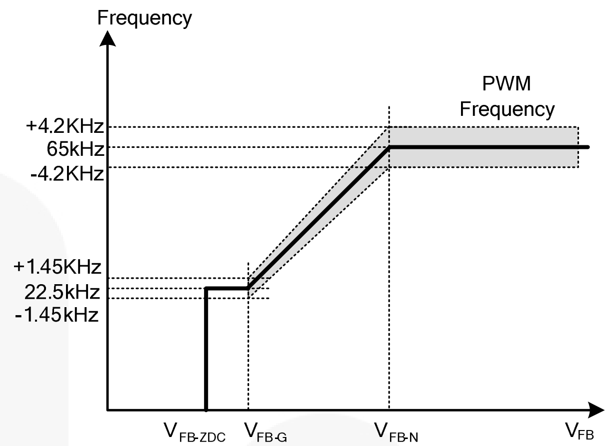

Figure 18. PWM Frequency

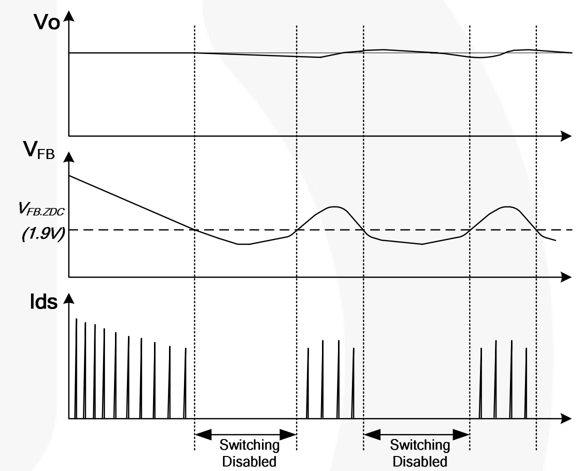

Figure 19. Burst Mode Operation

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. An internal frequency hopping circuit changes the switching frequency between 60.8kHz and 69.2kHz with a period of 4.4ms, as shown in Figure 20.

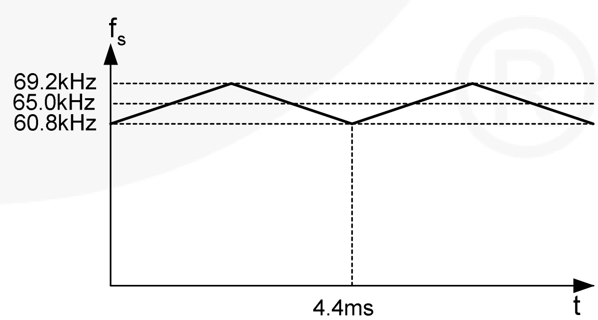

Figure 20. Frequency Hopping

Protections

Self-protective functions include V_{DD} Over-Voltage Protection (OVP), Open-Loop/Overload Protection (OLP), Over-Current Protection (OCP), Over-Temperature Protection (OTP). Among them, OLP, OCP, and SCP are auto-restart mode protections; while OVP and OTP are latch-mode protections.

Auto-Restart Mode Protection: Once a fault condition is detected, switching is terminated and the MOSFET remains off. This causes V_{DD} to fall because no more power is delivered from auxiliary winding. When V_{DD} falls to $V_{DD\text{-}OFF}$ (9.5V), the protection is reset and the operating current reduces to startup current, which causes V_{DD} to rise. FAN6861 resumes normal operation when V_{DD} reaches $V_{DD\text{-}ON}$ (17.5V). In this manner, the auto-restart can alternately enable and disable the switching of the MOSFET until the fault condition is eliminated (*see Figure 21*).

Latch-Mode Protection: Once this protection is triggered, switching is terminated and the MOSFET remains off. The latch is reset only when V_{DD} is discharged below 4V by unplugging AC power line.

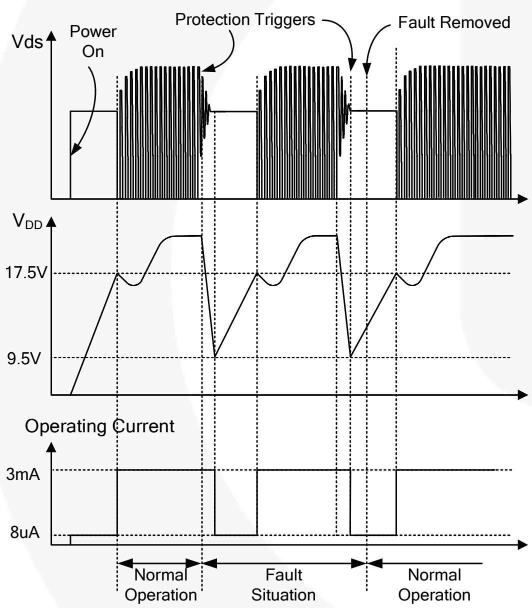

Figure 21. Auto Restart Operation

Two-Level Over-Current Protection (OCP)

FAN6861 has two levels of over-current protection thresholds. One is for pulse-by-pulse current limit, which turns off MOSFET for the remainder of the switching cycle when the sensing voltage of MOSFET drain current reaches the threshold. The other threshold is for the over-current protection, which shuts down the MOSFET gate when the sensing voltage of MOSFET drain current is above the threshold longer than the shutdown delay time (780ms).

This two-level OCP protection is designed for applications with peak load characteristics, such as printers and scanners.

These applications have motor load and inherently impose over-load condition on the power supply during acceleration mode. Therefore, the protection circuit should be triggered after a specified time to determine whether it is a transient situation or an abnormal situation.

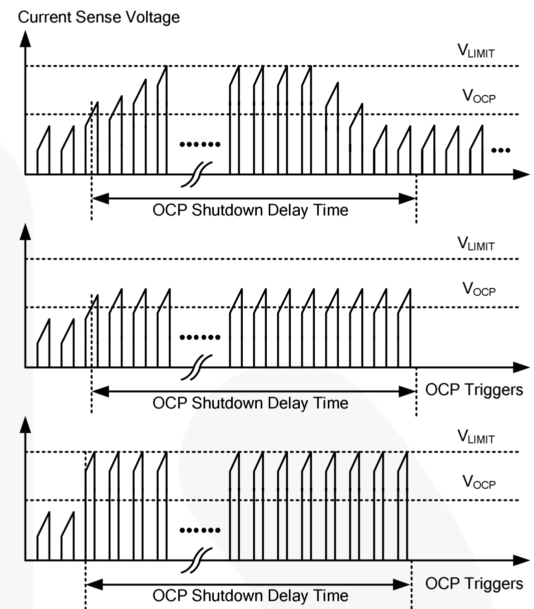

Figure 22. Two-Level OCP Operation

Open-Loop / Over-Load Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is broken, as shown in Figure 23, there is no current flowing through the opto-coupler transistor, which pulls up the feedback voltage to 5.2V.

When the feedback voltage is above 4.6V longer than 780ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 780ms due to the overload condition.

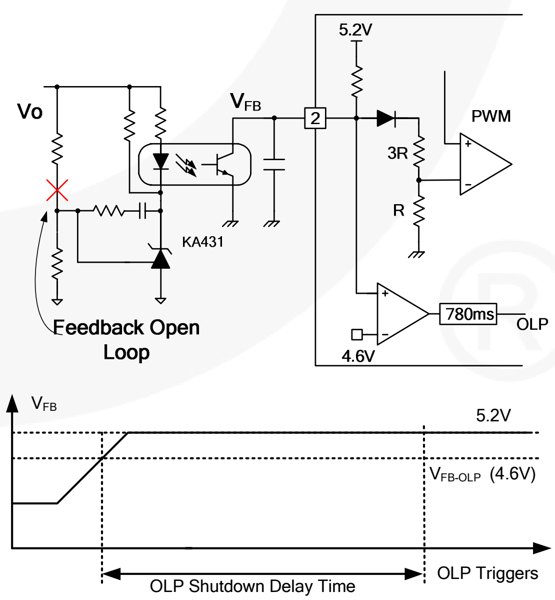

Figure 23. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage caused by over voltage on the V_{DD} pin. The OVP is triggered when V_{DD} voltage reaches 25V. It has a debounce time (typically 250µs) to prevent false trigger by switching noise.

Over-Temperature Protection (OTP)

The OTP circuit is composed of current source and voltage comparators. Typically NTC thermistor is connected between the RT pin and the GND pin. Once the voltage of this pin drops below a threshold of 0.7V, PWM output is disabled. Another comparator with 1V threshold is used to introduce hysteresis of OTP.

Constant Output Power Limit

FAN6861 has saw-limiter for pulse-by-pulse current limit, which guarantees almost constant power limit over different line voltages of universal input range.

The conventional pulse-by-pulse current limiting scheme has a constant threshold for current limit comparator, which results in higher power limit for high line voltage. FAN6861 has a sawtooth current limit threshold that increases progressively within a switching cycle, which provides lower current limit for high line and makes the actual power limit level almost constant over different line voltages of universal input range, as shown in Figure 24.

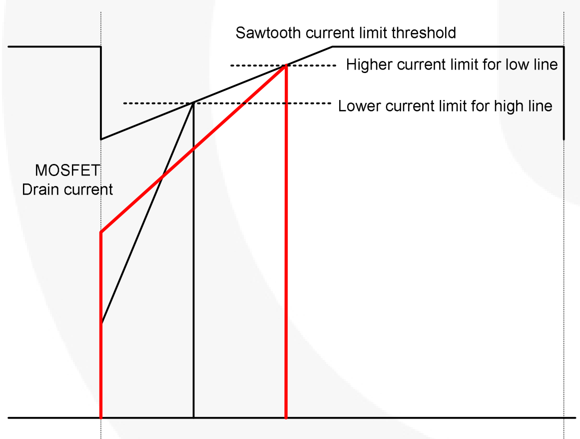

Figure 24. Sawtooth Current Limiter

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sense-resistor caused by primary-side capacitance and secondary-side rectifier reverse recovery. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (360ns), the PWM comparator is disabled and cannot switch off the gate driver. Thus, RC filter with a small RC time constant is enough for current sensing.

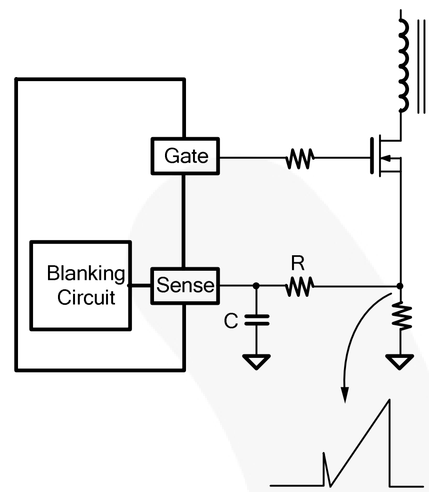

Figure 25. Current Sense R-C Filter

Soft-Start

The FAN6861 has an internal soft-start circuit that increases pulse-by-pulse current-limit comparator inverting input voltage slowly after it starts. The typical soft-start time is 10ms. The pulsewidth to the power MOSFET is progressively increased to establish the correct working conditions for transformers, rectifier diodes, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

Typical Application Circuit (Flyback Converter for Printer Application)

Application	Fairchild Devices	Input Voltage Range	Output
SMPS for Printer	FAN6861	90~264V_{AC}	32V/0.6254A Nominal (20W) 32V/1.56A Peak (50W)

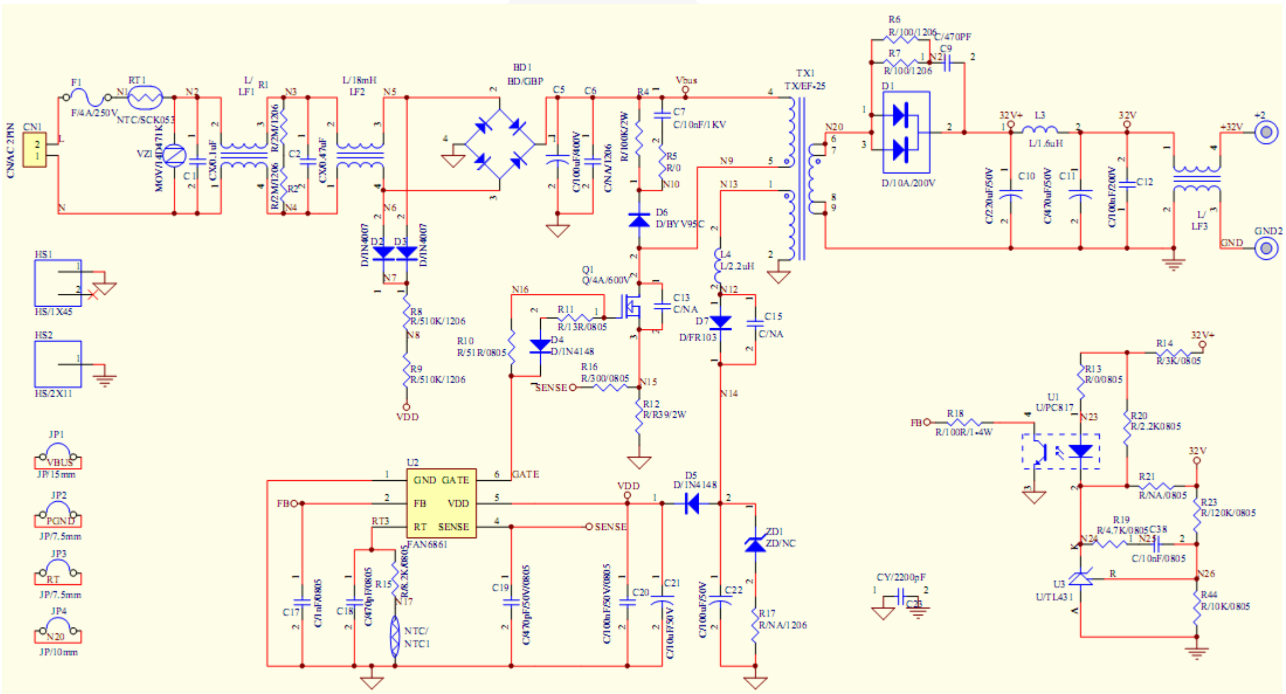

Figure 26. Schematic of Application Circuit

Transformer

- Core: EF-25/13/11
- Primary-Side Inductance: 500µH

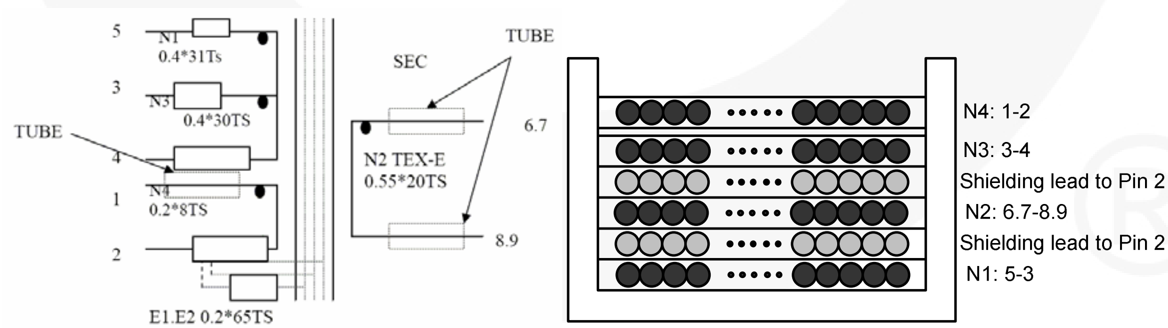

Figure 27. Transformer Structure

Physical Dimensions

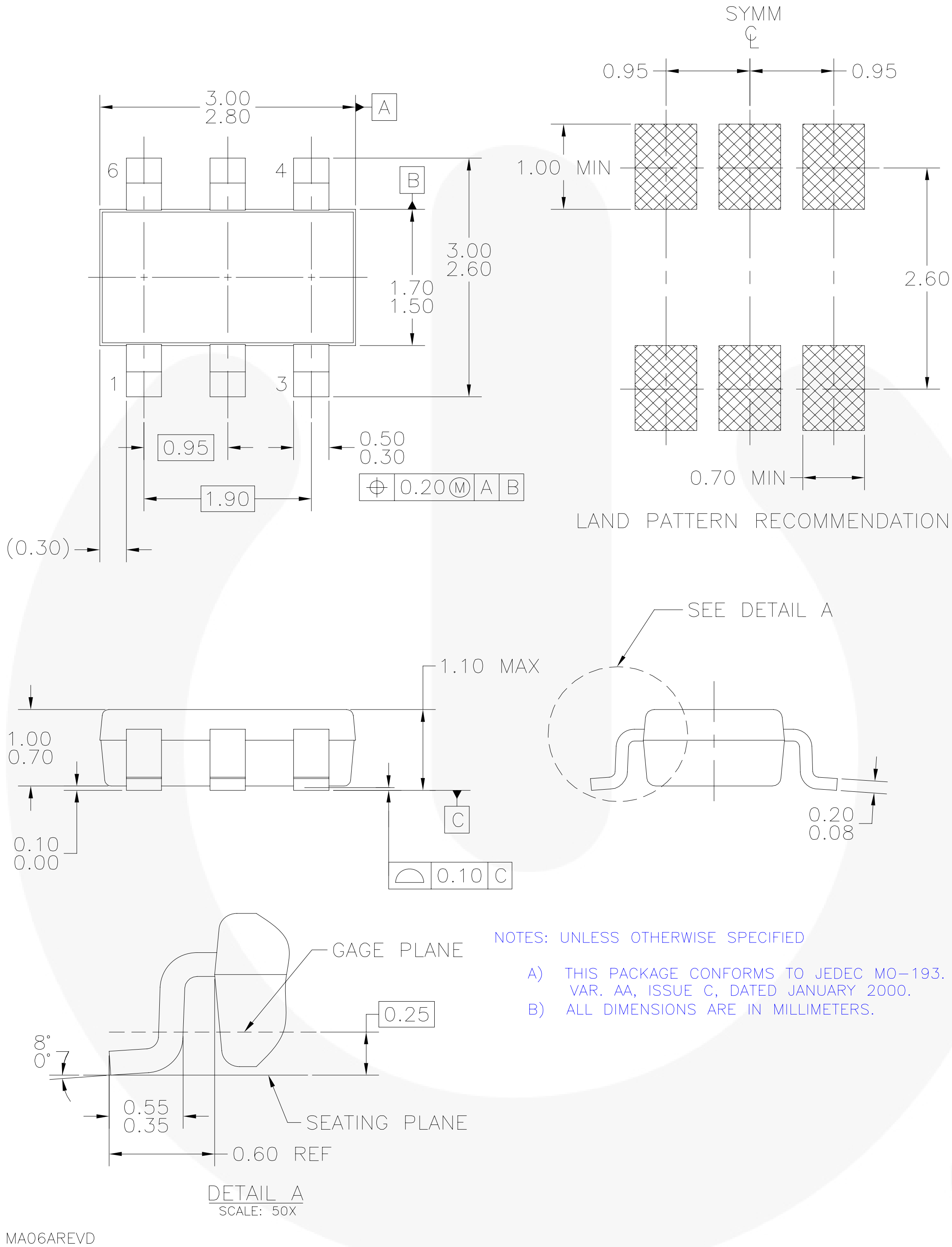

Figure 28. 6-Pin SSOT-6 Package

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