

FDME430NT

N-Channel PowerTrench® MOSFET

30 V, 6 A, 40 mΩ

Features

- Max $r_{DS(on)}$ = 40 mΩ at $V_{GS} = 4.5$ V, $I_D = 6$ A
- Max $r_{DS(on)}$ = 51 mΩ at $V_{GS} = 2.5$ V, $I_D = 5$ A
- Max $r_{DS(on)}$ = 71 mΩ at $V_{GS} = 1.8$ V, $I_D = 4$ A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

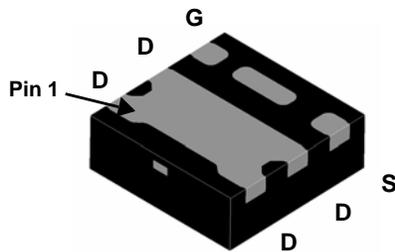


General Description

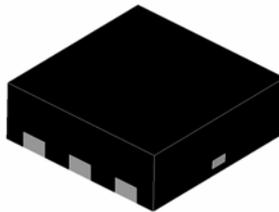
This single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench® process to optimize the $r_{DS(ON)}$ @ $V_{GS} = 1.8$ V on special MicroFET leadframe.

Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion

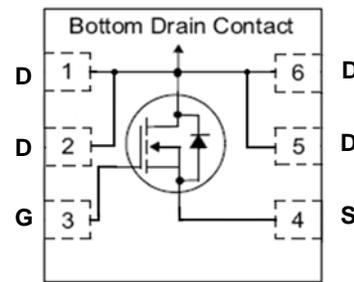


BOTTOM



TOP

MicroFET 1.6x1.6 Thin



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±12	V
I_D	Drain Current -Continuous $T_A = 25$ °C (Note 1a)	6	A
	-Pulsed	30	
P_D	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1a)	2.1	W
	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	175	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
YA	FDME430NT	MicroFET 1.6x1.6 Thin	7 "	8 mm	5000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	0.6	0.8	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 6\text{ A}$		25	40	m Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 5\text{ A}$		29	51	
		$V_{GS} = 1.8\text{ V}$, $I_D = 4\text{ A}$		38	71	
		$V_{GS} = 4.5\text{ V}$, $I_D = 6\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		34	54	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 6\text{ A}$		31		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		572	760	pF
C_{oss}	Output Capacitance			74	100	pF
C_{rss}	Reverse Transfer Capacitance			51	75	pF

Switching Characteristics

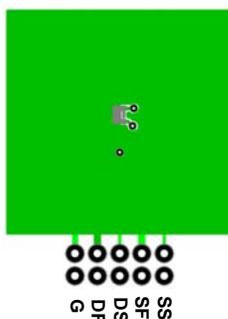
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 6\text{ A}$, $V_{GS} = 4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		7	14	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns
t_f	Fall Time			3.3	10	ns
Q_g	Total Gate Charge	$V_{DD} = 15\text{ V}$, $I_D = 6\text{ A}$, $V_{GS} = 4.5\text{ V}$		6.5	9	nC
Q_{gs}	Gate to Source Gate Charge			0.9		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.6		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 6\text{ A}$ (Note 2)		0.8	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 1.6\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		12	22	ns
Q_{rr}	Reverse Recovery Charge			2.9	10	nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $60\text{ }^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $175\text{ }^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

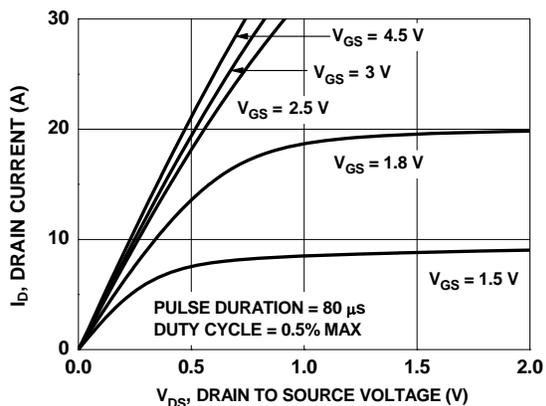


Figure 1. On Region Characteristics

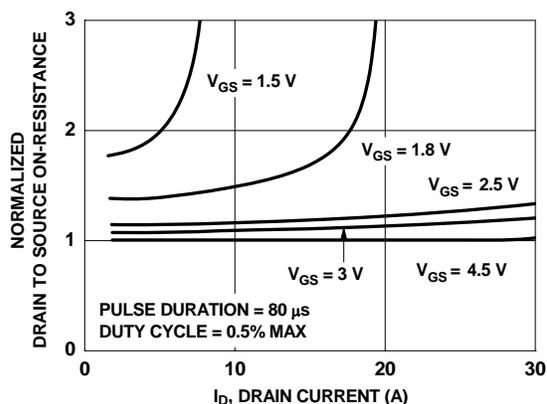


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

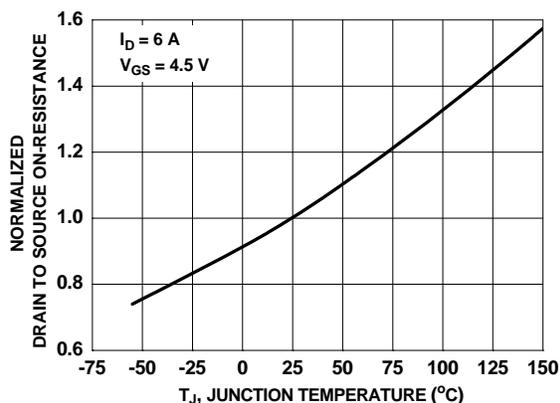


Figure 3. Normalized On Resistance vs Junction Temperature

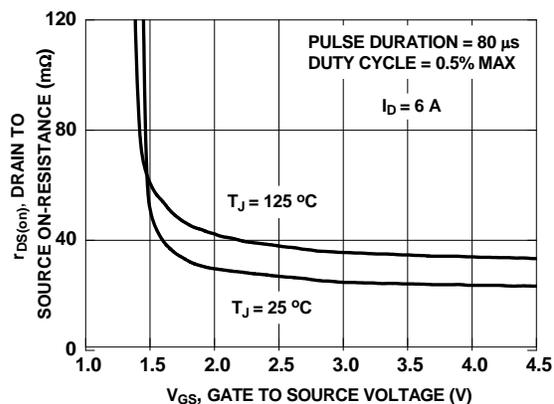


Figure 4. On-Resistance vs Gate to Source Voltage

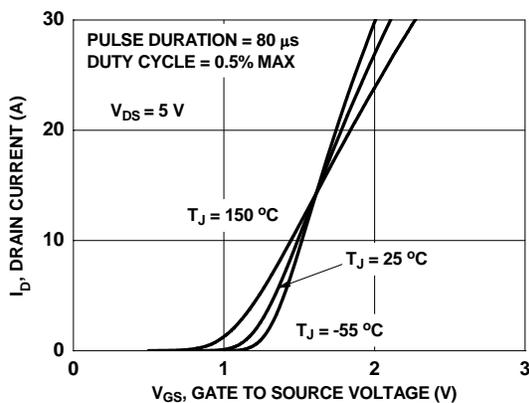


Figure 5. Transfer Characteristics

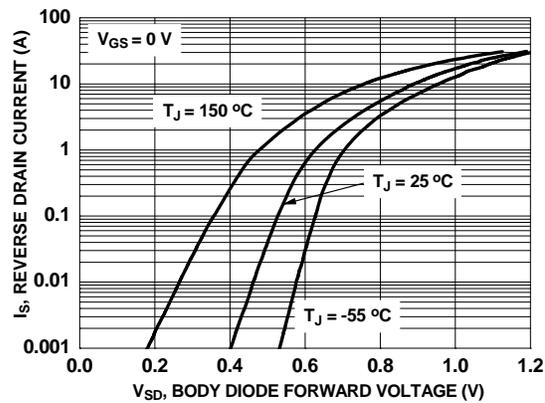


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

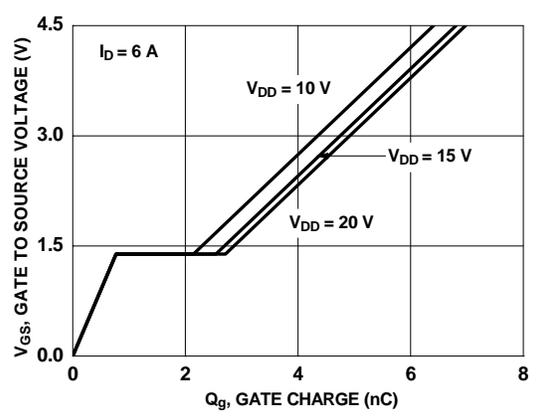


Figure 7. Gate Charge Characteristics

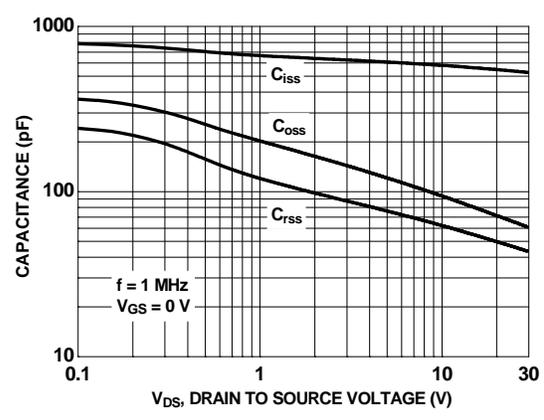


Figure 8. Capacitance vs Drain to Source Voltage

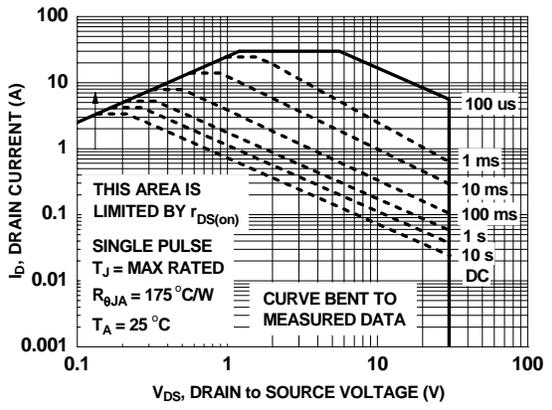


Figure 9. Forward Bias Safe Operating Area

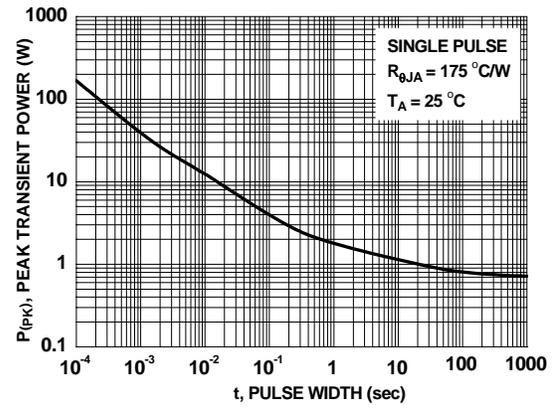


Figure 10. Single Pulse Maximum Power Dissipation

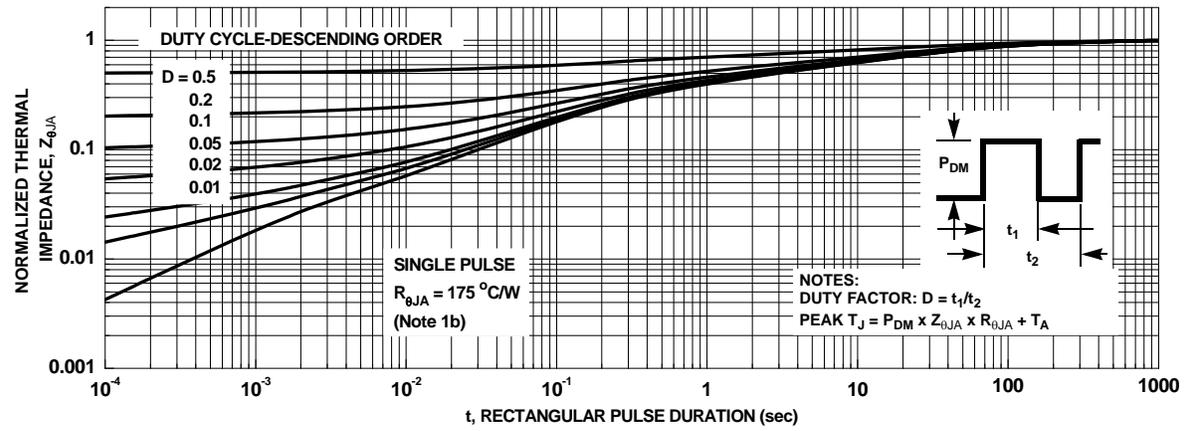
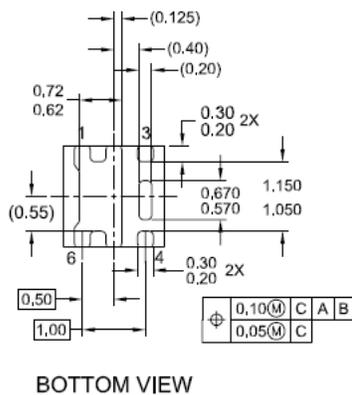
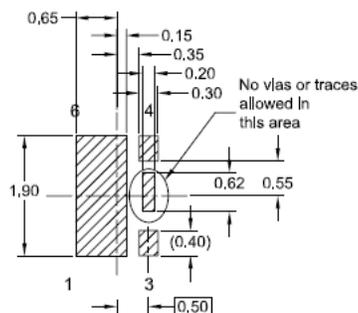
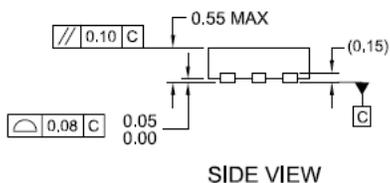
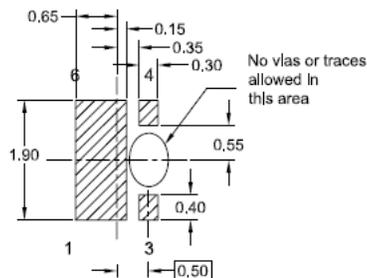
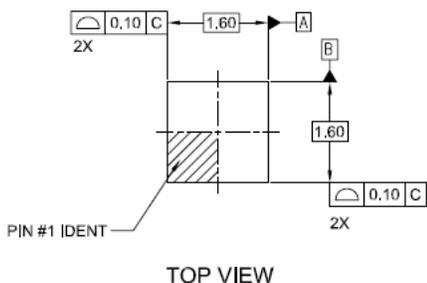


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



- NOTES:
- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 - D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY



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