FAIRCHILD SEMICONDUCTOR®

August 2012

FDMQ86530L

N-Channel PowerTrench® MOSFET
60 V, 8 A, 17.5 mΩ

Features

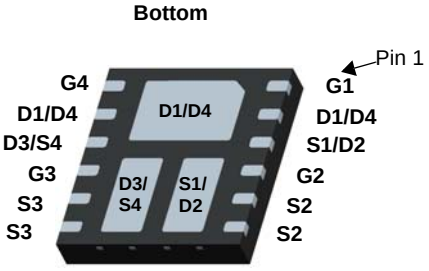
- Max $r_{DS(on)}$ = 17.5 mΩ at V_{GS} = 10 V, I_D = 8 A
- Max $r_{DS(on)}$ = 23 mΩ at V_{GS} = 6 V, I_D = 7 A
- Max $r_{DS(on)}$ = 25 mΩ at V_{GS} = 4.5 V, I_D = 6.5 A
- Substantial efficiency benefit in PD solutions
- RoHS Compliant

General Description

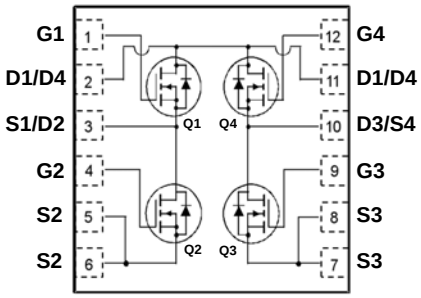
This quad MOSFET solution provides ten-fold improvement in power dissipation over diode bridge.

Application

- Active bridge



MLP 4.5x5



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			60	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		8	A
	-Continuous	T_A = 25 °C	(Note 1a)	8	
	-Pulsed			50	
P_D	Power Dissipation	T_C = 25 °C		22	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	1.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	135	

Package Marking and Ordering Information

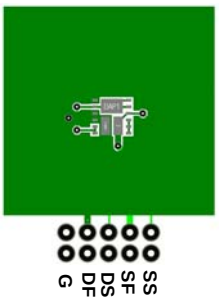
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMQ86530L	FDMQ86530L	MLP 4.5x5	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

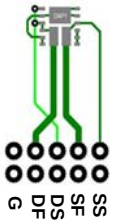
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		27		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8 A		12	17.5	mΩ
		V_{GS} = 6 V, I_D = 7 A		15	23	
		V_{GS} = 4.5 V, I_D = 6.5 A		20	25	
		V_{GS} = 10 V, I_D = 8 A, T_J = 125 °C		18	26	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 8 A		28		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz		1725	2295	pF
C_{oss}	Output Capacitance			299	400	pF
C_{rss}	Reverse Transfer Capacitance			10	15	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 8 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8.8	18	ns
t_r	Rise Time			3.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
t_f	Fall Time			2.8	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 30 V, I_D = 8 A		23	33	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 30 V, I_D = 8 A		11	16	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 30 V, I_D = 8 A		5.1		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 30 V, I_D = 8 A		2.3		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 8 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.6 A (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 8 A, di/dt = 100 A/μs		27	43	ns
Q_{rr}	Reverse Recovery Charge			12	22	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in^2 pad of 2 oz copper. the board designed Q1+Q3 or Q2+Q4.



b. 135 °C/W when mounted on a minimum pad of 2 oz copper. the board designed Q1+Q3 or Q2+Q4.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25 °C unless otherwise noted

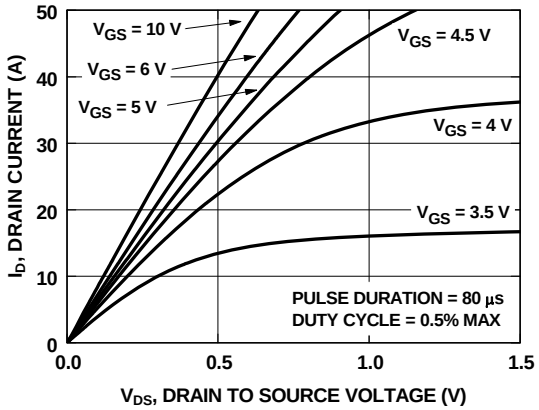


Figure 1. On-Region Characteristics

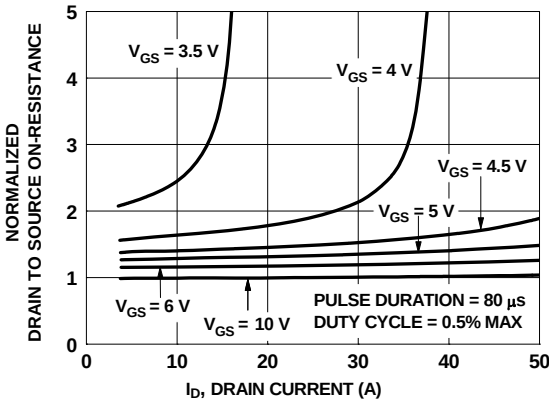


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

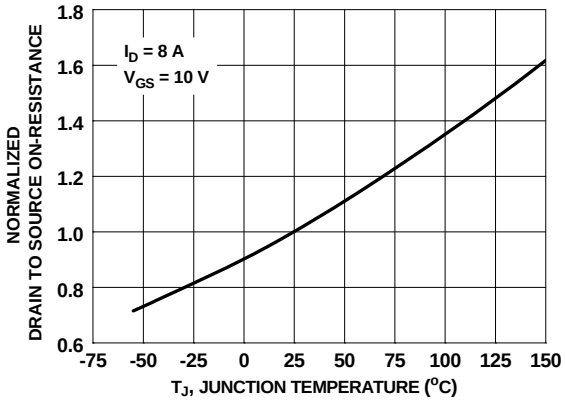


Figure 3. Normalized On-Resistance vs Junction Temperature

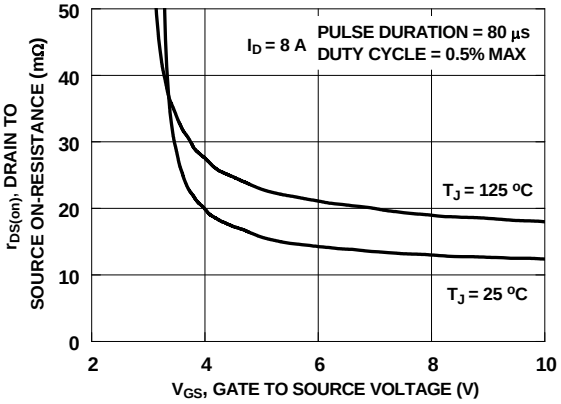


Figure 4. On-Resistance vs Gate to Source Voltage

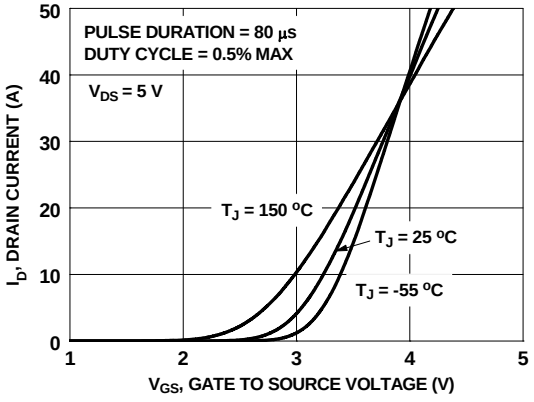


Figure 5. Transfer Characteristics

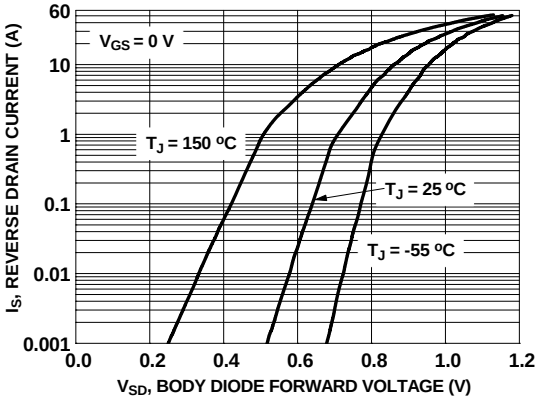


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

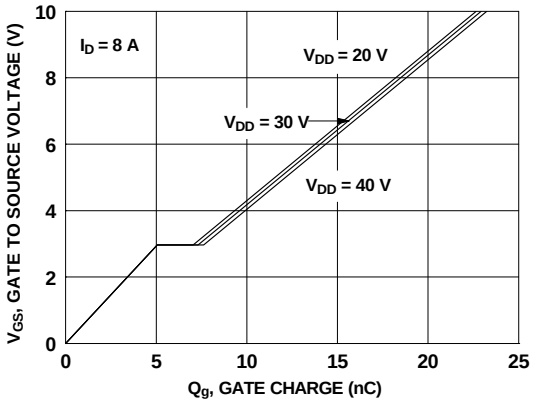


Figure 7. Gate Charge Characteristics

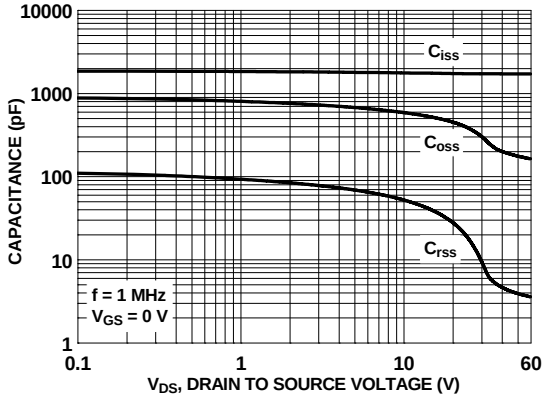


Figure 8. Capacitance vs Drain to Source Voltage

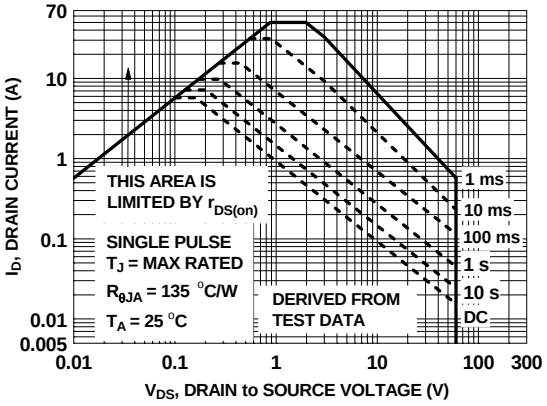


Figure 9. Forward Bias Safe Operating Area

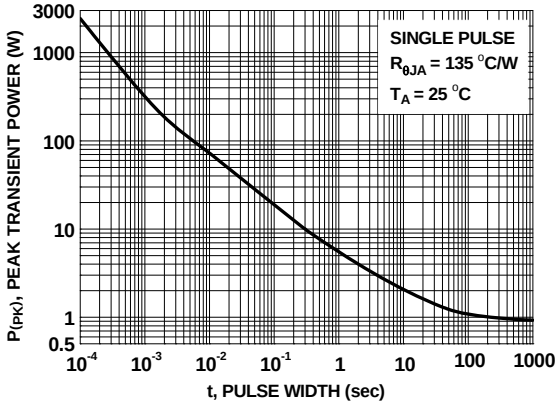


Figure 10. Single Pulse Maximum Power Dissipation

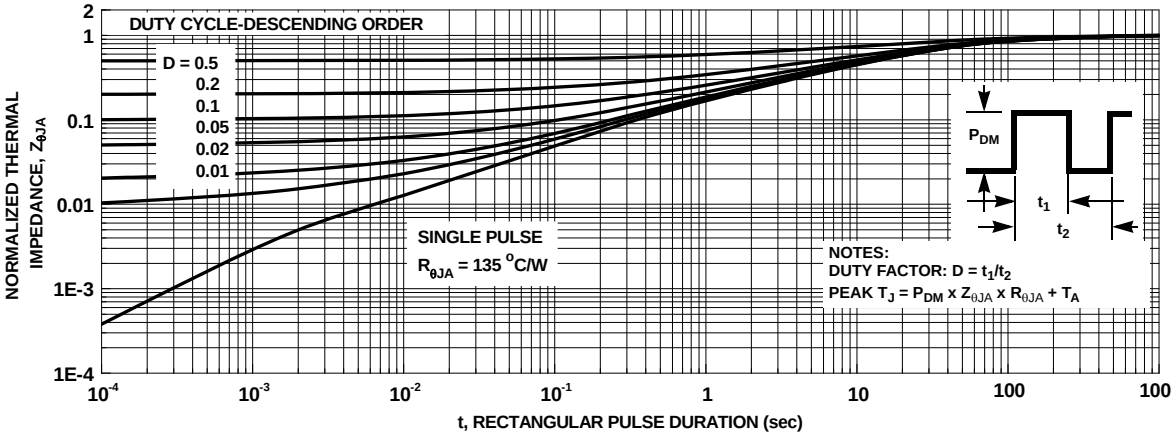
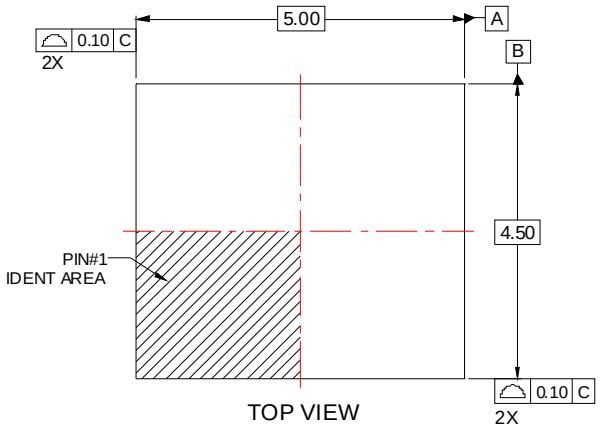
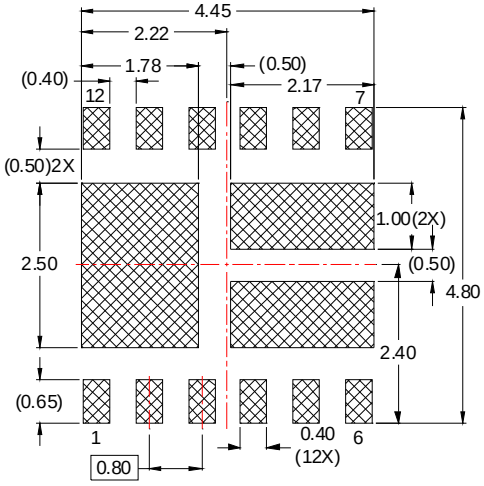


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

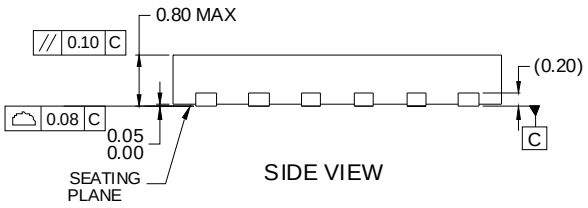
Dimensional Outline and Pad Layout



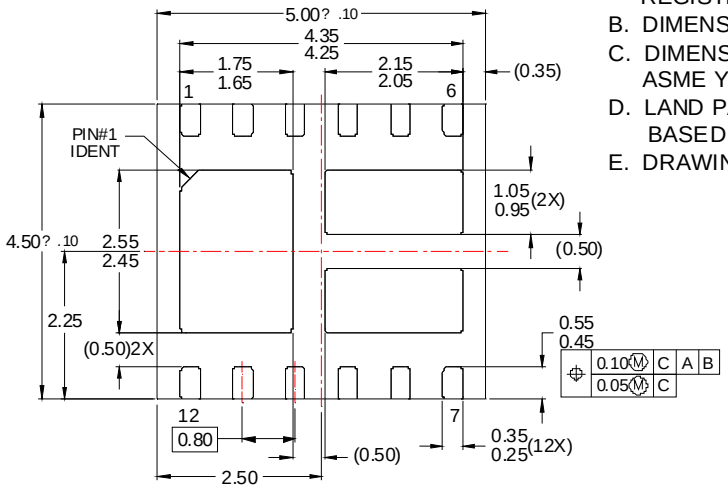
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. THIS MKT. DWG. DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.

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