FAIRCHILD

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FIN1028 — 3.3V LVDS 2-Bit High-Speed Differential Receiver

Features

- Greater than 400Mbs Data Rate
- Power Supply Operation: 3.3V
- Maximum Differential Pulse Skew: 0.4ns
- Maximum Propagation Delay: 2.5ns
- Low-Power Dissipation
- Power-Off Protection
- Fail-Safe Protection for Open-Circuit, Shorted, and Terminated Conditions
- Meets or Exceeds the TIA/EIA-644 LVDS Standard
- Flow-through Pinout Simplifies PCB Layout

Description

This dual receiver is designed for high-speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100mV, to LVTTL signal levels. LVDS provides low EMI at ultra-low power dissipation, even at high frequencies. This device is ideal for high-speed transfer of clock and data signals.

The FIN1028 can be paired with its companion driver, the FIN1027, or any other LVDS driver.

Ordering Information

Part Number	Operating Temperature Range	🍃 Eco Status	Package	Packing Method
FIN1028M	-40 to +85°C	RoHS	8-Lead Small Outline Package (SOIC) JEDEC MS-012, 0.150 inch Narrow	Trays
FIN1028MX	-40 to +85°C	RoHS	8-Lead Small Outline Package (SOIC) JEDEC MS-012, 0.150 inch Narrow	Tape and Reel

🍃 *For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.*

Pin Configuration
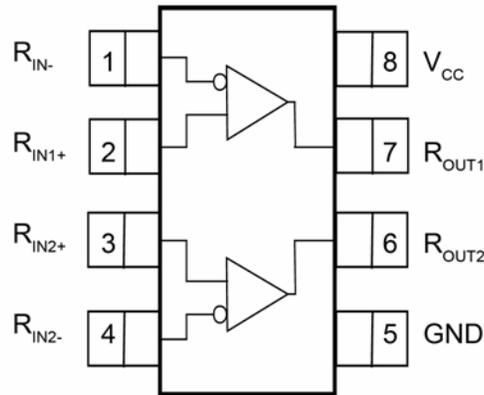
Figure 1. SOIC Pin Assignments (Top View)

Pin Definitions

Pin #	Name	Description
1	R_{IN1-}	Inverting LVDS Input
2	R_{IN1+}	Non-Inverting LVDS Input
3	R_{IN2+}	Non-Inverting LVDS Input
4	R_{IN2-}	Inverting LVDS Input
5	GND	Ground
6	R_{OUT2}	LVTTL Data Output
7	R_{OUT1}	LVTTL Data Output
8	V_{CC}	Power Supply

Function Table

Inputs		Outputs
R_{IN+}	R_{IN-}	R_{OUT}
LOW	HIGH	LOW
HIGH	LOW	HIGH
Fail-Safe Conditions[1]		HIGH

Note:
1. Fail-safe=open, shorted, terminated.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	4.6	V
R_{INx+}, R_{INx-}	DC Input Voltage	-0.5	4.7	V
R_{OUTx}	DC Output Voltage	-0.5	6.0	V
I_O	DC Output Current		16	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature, Soldering 10 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114		≥6500	V
	Machine Model, JESD22-A115		≥300	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
$\left|V_{ID}\right|$	Magnitude of Differential Voltage	100	V_{CC}	mV
V_{IC}	Common-Mode Input Voltage	0.05	2.35	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

Typical values are at T_A=25°C and with V_{CC}=3.3V. Over-supply voltage and operating temperature ranges, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input Threshold HIGH	Figure 2, Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	Figure 2, Table 1	-100			mV
I_{IN}	Input Current	V_{IN}=0V or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-off Input Current	V_{CC}=0V, V_{IN}=0V or 3.6V			±20	µA
V_{OH}	Output HIGH Voltage	I_{OH}=-100µA	V_{CC}-0.2			V
		I_{OH}=-8mA	2.4			
V_{OL}	Output LOW Voltage	I_{OL}=100µA			0.2	V
		I_{OL}=8mA			0.5	
V_{IK}	Input Clamp Voltage	I_{IK}=-18mA	-1.5			V
I_{CC}	Power Supply Current	R_{IN+}=1V and R_{IN-}=1.4V or R_{IN+}=1.4V and R_{IN-}=1V			9	mA
C_{IN}	Input Capacitance			4		pF
C_{OUT}	Output Capacitance			6		pF

DC Electrical Characteristics

Typical values are at T_A=25°C and with V_{CC}=3.3V. Over-supply voltage and operating temperature ranges, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Differential Propagation Delay, LOW-to-HIGH		0.9		2.5	ns
t_{PHL}	Differential Propagation Delay, HIGH-to-LOW		0.9		2.5	ns
t_{TLH}	Output Rise Time (20% to 80%)	$\lvert V_{ID} \rvert$=400mV, C_L=10pF Figure 2, Figure 3		0.5		ns
t_{THL}	Output Fall Time (80% to 20%)			0.5		ns
$t_{SK(P)}$	Pulse Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.4	ns
$t_{SK(LH)}$, $t_{SK(HL)}$	Channel-to-Channel Skew[2]				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew[3]				1.0	ns

Notes:
2. $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.
3. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.
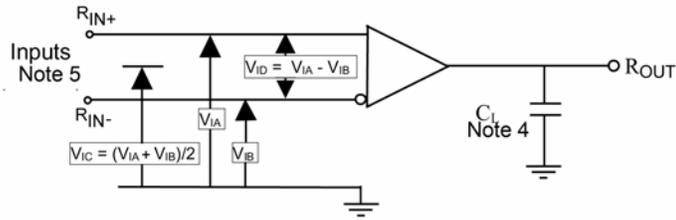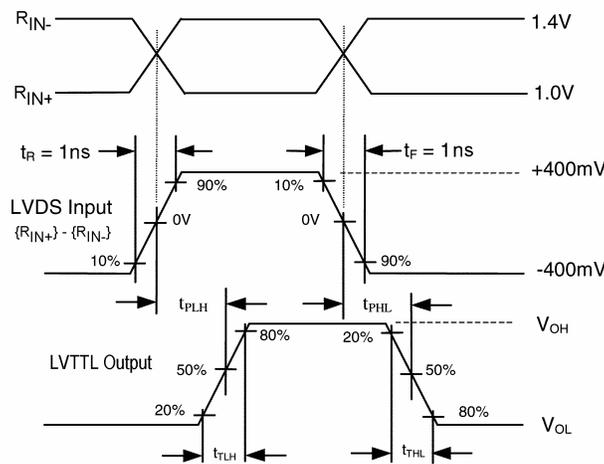
Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

Notes:
4. C_L includes all probe and fixture capacitances.
5.   All input pulses have frequency = 10MHz, t_R or t_F=1ns.

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
2.4	2.3	100	2.35
2.3	2.4	-100	2.35
0.1	0	100	0.05
0	0.1	-100	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3

Figure 3. AC Waveforms

Typical Performance Characteristics
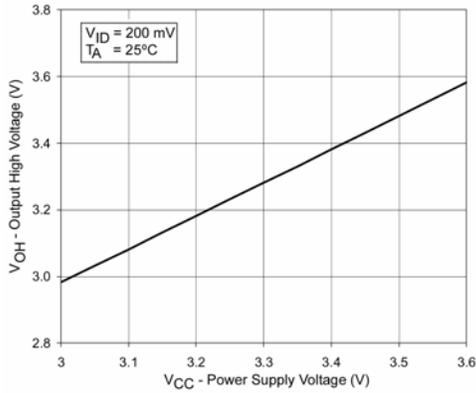
**Figure 4. Output High Voltage
vs. Power Supply Voltage**
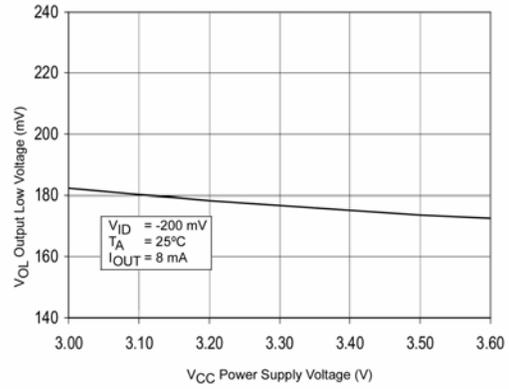
**Figure 5. Output Low Voltage
vs. Power Supply Voltage**
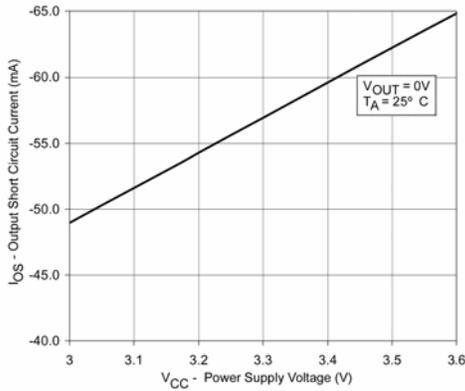
**Figure 6. Output Short Circuit Current
vs. Power Supply Voltage**
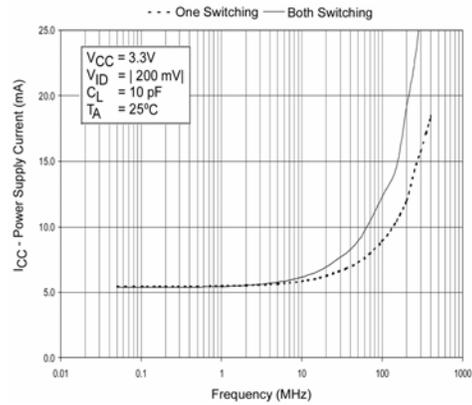
Figure 7. Power Supply Current vs. Frequency
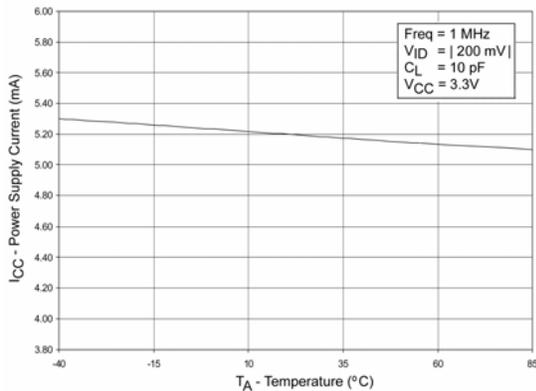
**Figure 8. Power Supply Current
vs. Ambient Temperature**
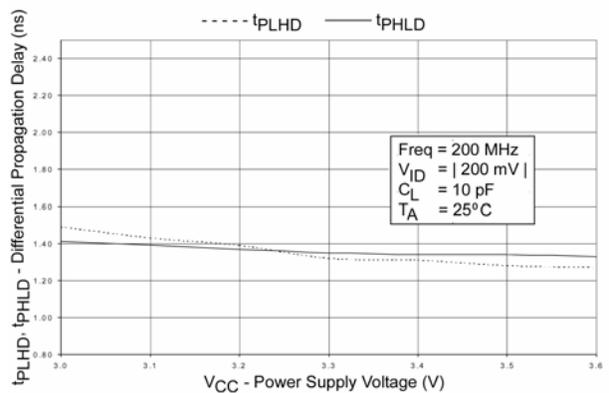
**Figure 9. Differential Propagation Delay
vs. Power Supply Voltage**

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Typical Performance Characteristics (Continued)

Figure 10. Differential Propagation Delay vs. Ambient Temperature
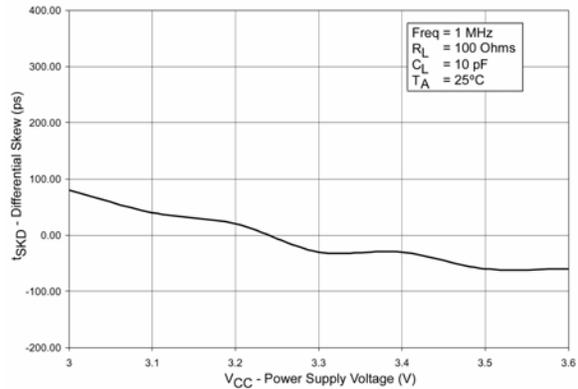
Figure 11. Differential Skew (t_{PLH}-t_{PHL}) vs. Power Supply Voltage
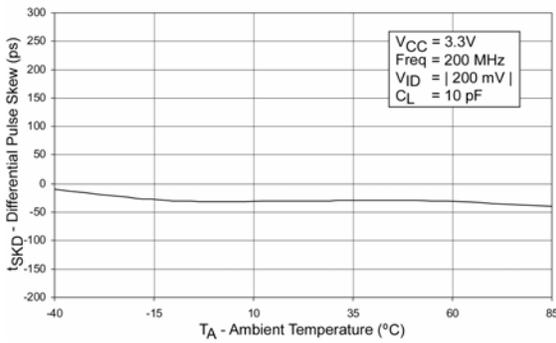
Figure 12. Differential Skew (t_{PHL}-t_{PHL}) vs. Ambient Temperature
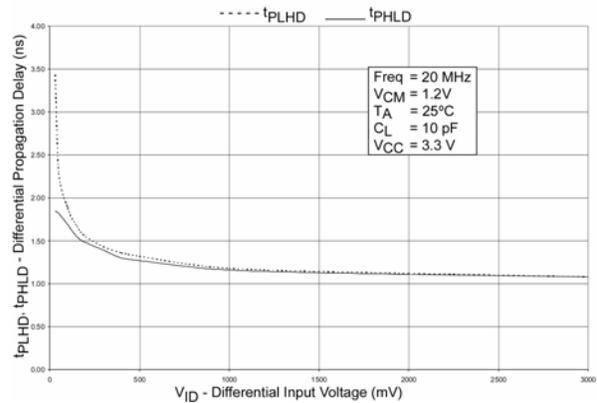
Figure 13. Differential Propagation Delay vs. Differential Input Voltage
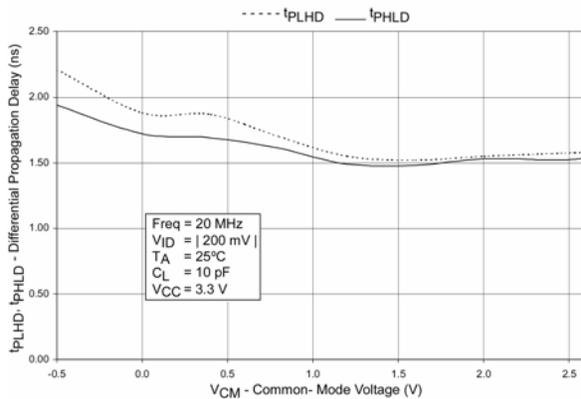
Figure 14. Differential Propagation Delay vs. Common-Mode Voltage
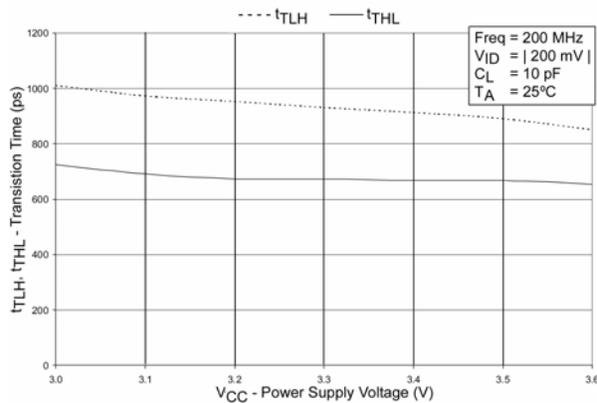
Figure 15. Transition Time vs. Power Supply Voltage

Typical Performance Characteristics (Continued)
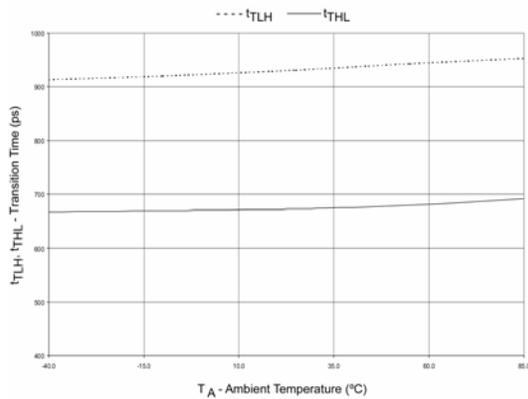
Figure 16. Transition Time vs. Ambient Temperature
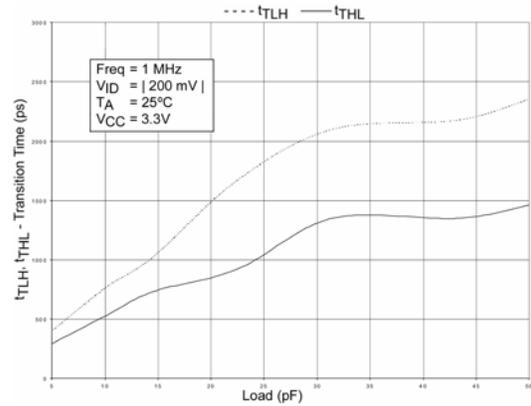
Figure 17. Differential Propagation Delay vs. Load
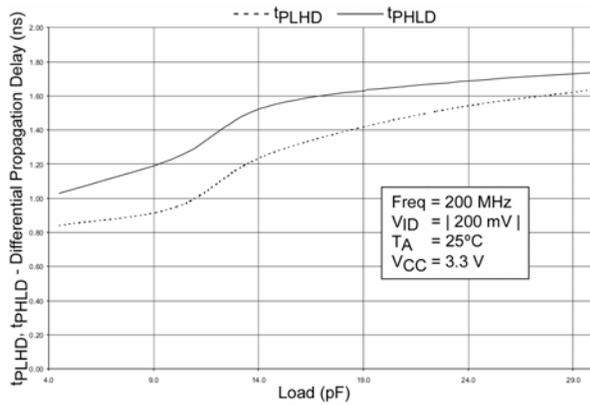
Figure 18. Differential Propagation Delay vs. Load
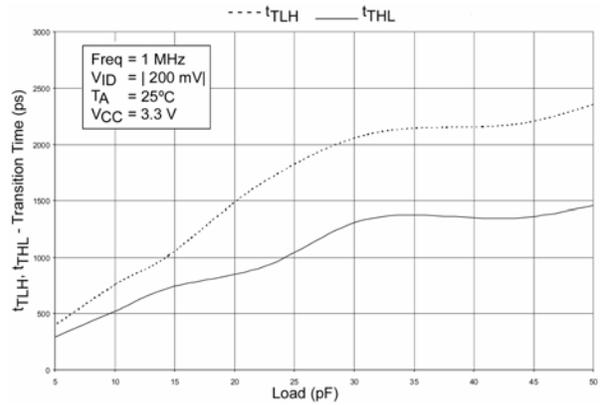
Figure 19. Transition Time vs. Load
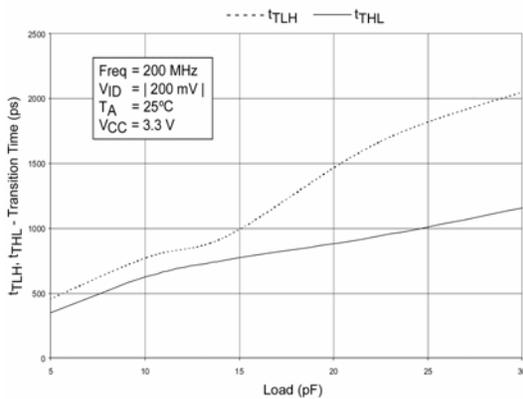
Figure 20. Transition Time vs. Load

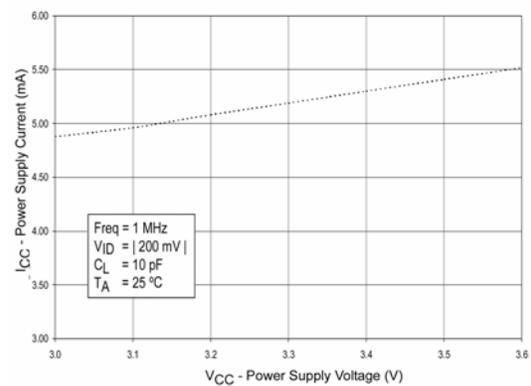**Figure 21. Power Supply Current vs. Power Supply Voltage**
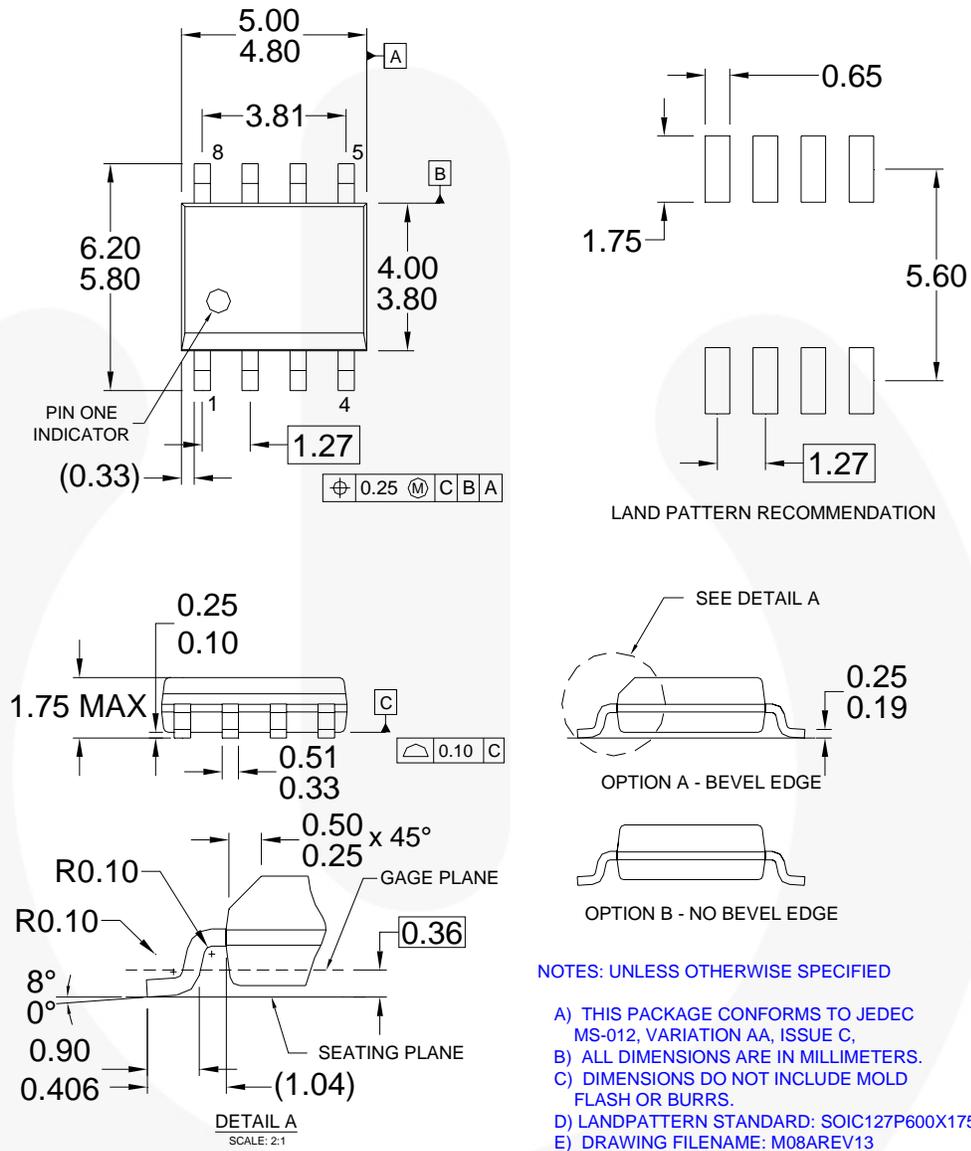
Physical Dimensions

5.00 / 4.80 [A]

3.81

8   5

6.20 / 5.80

4.00 / 3.80 [B]

PIN ONE INDICATOR

1   4

(0.33)

1.27

⊕ | 0.25 Ⓜ | C | B | A

0.65

1.75

5.60

1.27

LAND PATTERN RECOMMENDATION

0.25 / 0.10

1.75 MAX

[C]

0.51 / 0.33

△ | 0.10 | C

0.50 / 0.25 x 45°

R0.10

R0.10

GAGE PLANE

0.36

8°
0°

0.90 / 0.406

SEATING PLANE

(1.04)

DETAIL A
SCALE: 2:1

SEE DETAIL A

0.25 / 0.19

OPTION A - BEVEL EDGE

OPTION B - NO BEVEL EDGE

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 22. 8-Lead, Small Outline Package (SOIC), JEDEC MS-012, 0.150-inch, Narrow Body

Click here for tape and reel specifications, available at:

http://www.fairchildsemi.com/products/discrete/pdf/soic8_tr.pdf

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FastvCore™	®	SyncFET™	VisualMax™
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		SYSTEM GENERAL®	

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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