

FPD87346BXA Low EMI, Low Dynamic Power (SVGA) XGA/WXGA TFT-LCD Timing Controller with Reduced Swing Differential Signaling (RSDS™) Outputs

Check for Samples: [FPD87346BXA](#)

FEATURES

- Reduced Swing Differential Signalling (RSDS™) digital bus reduces dynamic power, EMI and bus width from the timing controller
- LVDS single pixel input interface system
- Input clock range from 40 MHz to 85 MHz
- Drives RSDS™ Column Drivers at 170 Mb/s with an 85 MHz clock (Max.)
- Virtual 8 bit color depth in FRC/Dithering mode
- Single narrow 9-bit differential Source Driver bus minimizes width of Source PCB
- Ability to drive (SVGA) XGA and Wide XGA TFT-LCD Systems
- Failure detect function in DE mode (Bonding Option)
- CMOS circuitry operates from a 3.0V–3.6V supply

DESCRIPTION

The FPD87346BXA is a timing controller that combines an LVDS single pixel input interface with National's Reduced Swing Differential Signaling (RSDS™) output driver interface for (SVGA) XGA and Wide XGA resolutions. It resides on the TFT-LCD panel and provides the data buffering and control signal generation for (SVGA) XGA, and Wide XGA graphic modes. The RSDS™ path to the column driver contributes toward lowering radiated EMI and reducing system dynamic power consumption.

This single RSDS™ bus conveys the 8-bit color data for (SVGA) XGA, and Wide XGA panels at 170 Mb/s when using VESA 60 Hz standard timing.

System Diagram

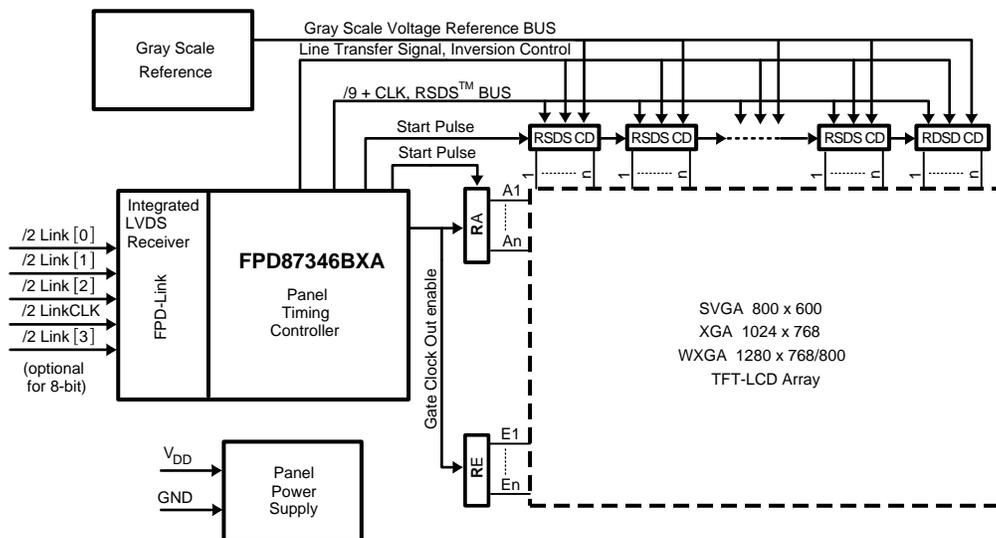


Figure 1. Block Diagram of the LCD Module



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Block Diagram

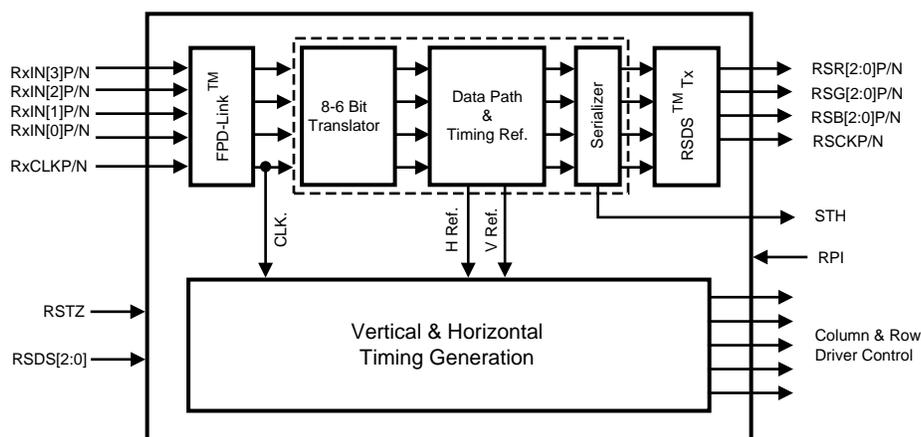


Figure 2. Block Diagram

Functional Description

FPD-LINK RECEIVER

The FPD87346BXA is TFT-LCD Timing Controller (TCON) that is based on National Semiconductor's Embedded Logic Array family of TCON devices. The logic architecture is implemented using standard and default timing controller functionality based on an Embedded Gate Array. In its standard configuration the Gate Driver Control, Column Driver Control signals, and Logic Functions of the device are preset. Customization of control signal timing and other logic functions of the device are reconfigurable through customer supplied Verilog/RTL Code or User-defined specifications. The combination of Embedded Logic Array and National Semiconductor's world class Mixed-signal Analog functional blocks such as LVDS and RSDS™ provides a flexible platform to meet the needs of TFT-LCD Manufacturers.

SPREAD SPECTRUM SUPPORT

The FPD-Link receiver supports graphics controllers with Spread Spectrum interfaces for reducing EMI. The Spread Spectrum methods supported are center and down spread. A maximum of deviation of $\pm 2\%$ center spread or -4% down spread is supported at a frequency modulation of 100 kHz maximum.

8-6 BIT TRANSLATOR

8-bit data is reduced to a 6-bit data path via a time multiplexed dithering technique or simple truncation of the LSBs. This function is enabled via the input control pins.

DATAPATH BLOCK AND RSDS™ TRANSMITTER

6(8)-bit video data (RGB) is input to the Datapath Block supports up to an 85 MHz pixel rate. The data is delayed to align the Column Driver Start Pulse with the Column Driver data. The data bus (RSR[2:0]P/N, RSG[2:0]P/N, RSB[2:0]P/N) outputs at a 170 MHz rate on 9 differential output channels. The clock is output on the RSCKP/N differential pair. The RSDS Column Drivers latch data on both positive and negative edges of the clock. The RSDS™ output setup/hold timings are also adjustable through the RSDS[2:0] input pins.

TIMING CONTROL FUNCTION

The Timing Controller Functional Block generates all the necessary control signals to the Column Driver (TP, STH, and REV) and Gate Drivers (STV, CPV, and OE) to interface with a TFT-LCD panel.

RSDS OUTPUT VOLTAGE CONTROL

The RSDS™ output voltage swing is controlled through an external load resistor connected to the R_{PI} pin. The RSDS™ output signal levels can be adjusted to suit the particular application. This is dependent on overall LCD module design characteristics such as trace impedance, termination, etc. The RSDS™ output voltage is inversely related to the R_{PI} value. Lower R_{PI} values will increase the RSDS™ output voltage swing and consequently overall power consumption will also increase.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

Supply Voltage (V _{DD})	-0.3V to +4.0V
DC TTL Input Voltage (V _{IN})	-0.3V to (V _{DD} + 0.3V)
DC Output Voltage (V _{OUT})	-0.3V to (V _{DD} + 0.3V)
Junction Temperature	+150°C
Storage Temperature Range (T _{STG})	-65°C to +150°C
Lead Temperature (T _L) (Soldering 10 sec.)	260°C
ESD Rating:	
(C _{ZAP} = 120 pF, R _{ZAP} = 1500Ω)	MM = 200V, HBM = 2000V

(1) "Absolute Maximum Rating" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Operating Conditions

	Min	Max	Units
Supply Voltage (V _{DD})	3.0	3.6	V
Operating Temp Range (T _A)	0	70	°C
Supply Noise Voltage (V _{DD})		200	mV _{PP}
Spread Spectrum Support, LVDS			
Spreading Range		± 2.0	%
Modulation Rate		100	kHz
Operating Frequency (f)	40	85	MHz

DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$, $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified).

TTL DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Minimum High Level Output Voltage	STV, CPV, OE	$I_{OH} = -6\ \text{mA}$	2.4			V
		TP, REV	$I_{OH} = -8\ \text{mA}$				
		STH	$I_{OH} = -24\ \text{mA}$				
V_{OL}	Maximum Low Level Output Voltage	STV, CPV, OE	$I_{OL} = +6\ \text{mA}$			0.4	V
		TP, REV	$I_{OL} = +8\ \text{mA}$				
		STH	$I_{OL} = +24\ \text{mA}$				
V_{IH}	Minimum High Level Input Voltage			2.0			V
V_{IL}	Maximum Low Level Input Voltage					0.8	V
I_{IN}	Input Current	$V_{IN} = V_{DD}, \text{GND}$		-10		+10	μA
I_{DD}	Average Supply Current	$f = 85\ \text{MHz}$ $V_{DD} = 3.6\text{V}$, $C_{L(\text{TTL})} = 15\ \text{pF}$, $I_{PI} = 100\ \mu\text{A}$ (Typically PI pin connected to $13\ \text{k}\Omega$ to ground) $R_{L(\text{RSDS})} = 100\ \Omega$ and $C_{L(\text{RSDS})} = 5\ \text{pF}$ (jig & test fixture capacitance), See Figure 4 for input conditions			85	150	mA

Figure 3. FPD-Link Receiver Input Pattern Used to Measure I_{DD}

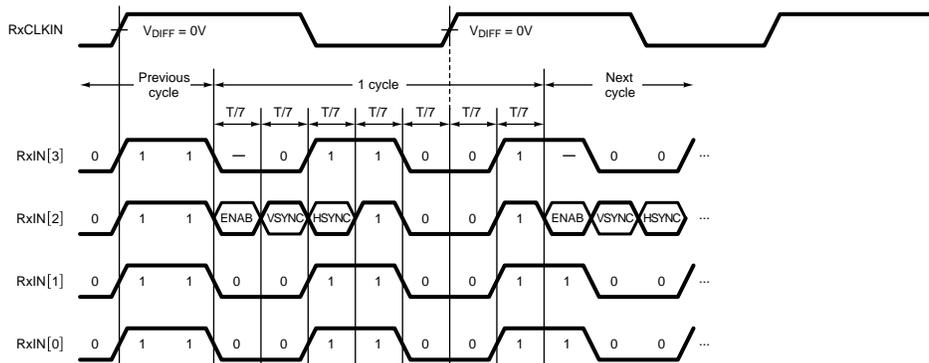
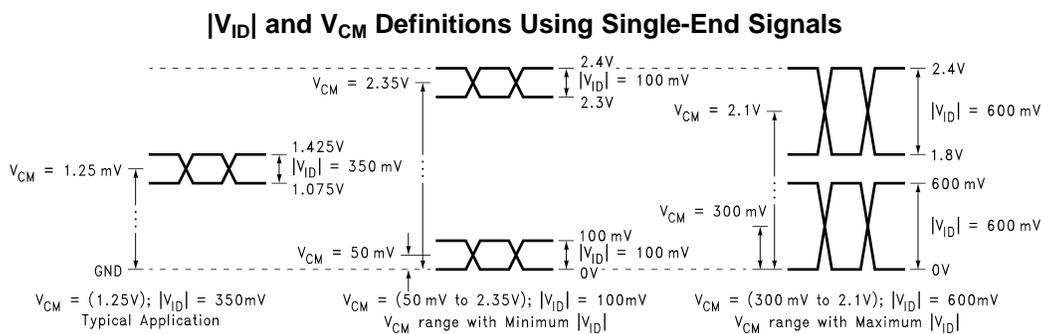


Figure 4. FPD-Link Receiver I_{DD} Pattern

FPD-Link (LVDS) RECEIVER INPUT (RxCLK+/-, RxIN[y] +/-; y = 0, 1, 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS RECEIVER DC SPECIFICATIONS (1)						
V_{THLVDS}	Differential Input High Threshold Voltage	$V_{CM} = 1.2V$			+100	mV
V_{TLVDS}	Differential Input Low Threshold Voltage		-100			mV
I_{IN}	Input Current	$V_{IN} = 2.4V, V_{DD} = 3.6V$	-10		+10	μA
		$V_{IN} = 0V, V_{DD} = 3.6V$	-10		+10	μA
V_{IN}	Input Voltage Range (Single-ended)		0		2.4	V
$ V_{ID} $	Differential Input Voltage		0.100		0.600	V
V_{CM}	Common Mode Voltage Offset		$0 + V_{ID} /2$		$2.4 - V_{ID} /2$	V

(1) LVDS Receiver DC parameters are measured under static and steady state conditions which may not reflect the actual performance in the end application.



RSDS TRANSMITTER OUTPUT (RSCKP/N, RSx[y]P/N; x = R, G, B y = 0, 1, 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ODRSDS}	Differential Output Voltage	$R_L = 100\Omega$ $R_{PI} = 13\text{ k}\Omega$		± 200 ⁽¹⁾ and (Figure 6)		mV
V_{OSRSDS}	Offset Voltage		1.1	1.3	1.5	V

(1) $V_{OSRSDS} = (V(F\&B)CLKP + V(F\&B)CLKN)/2$ or $V_{OSRSDS} = (V(F\&B)XYP + V(F\&B)XYN)/2$. $V_{ODRSDS} = V(F\&B)CLKP - V(F\&B)CLKN$ or $V_{ODRSDS} = V(F\&B)XYP - V(F\&B)XYN$. The load between the positive and negative output is 100Ω .

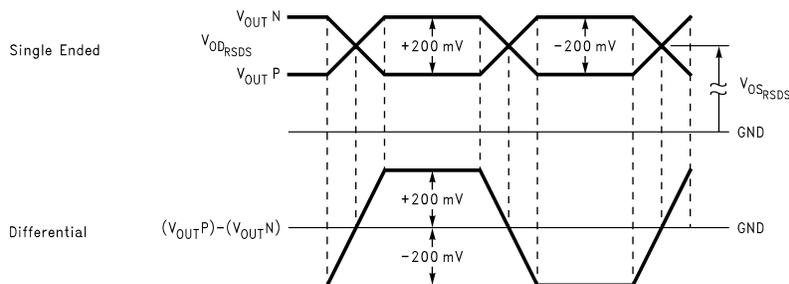


Figure 6. RSDS Waveform - Single Ended and Differential

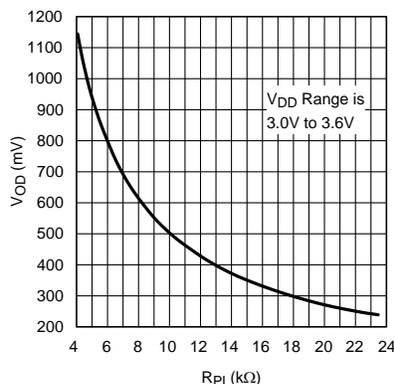


Figure 7. Typical RSDS_{VOD} vs. R_{PI} Response Curve

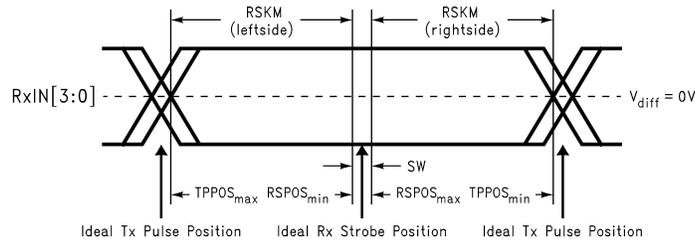
AC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$, $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified).

LVDS Data Input

Symbol	Parameter	Conditions	Min	Max	Units
RSCLKOUTDLY	FPD-Link Receiver Phase Lock Loop Wake-up Time	Figure 10		10	ms
RSKM	RxIN Skew Margin ⁽¹⁾ and (Figure 8)	$f = 85\ \text{MHz}$, $V_{DD} = 3.3\text{V}$	220		ps

- (1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window: RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type and length of cable, and source clock (FPD-Link Transmitter TxCLK IN) jitter (less than 190 ps). The specified RSKM minimum assumes a TPPOS max of 200 ps. $\text{RSKM} = \text{cable skew (type, length)} + \text{source clock jitter (cycle to cycle)} + \text{remaining margin for data sampling} (\geq 0)$. This parameter is guaranteed by design. The limits are based on statistical analysis of the device performance over PVT (Process, Voltage, Temperature) range.



Acronyms:

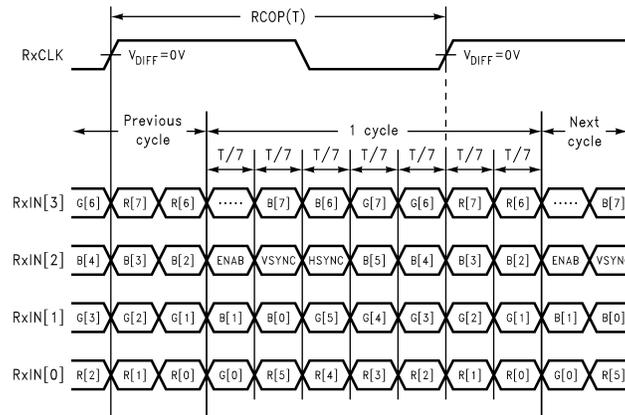
RSKM Receiver Skew Margin
 TPPOS Transmitter Pulse Position
 RSPOS Receiver Strobe Position
 SW Strobe Width

Definitions:

SW Setup and Hold Time (Internal data sampling window)
 $\text{RSKM} = \text{Cable Skew (type, length)} + \text{Source Clock Jitter (cycle to cycle)} + \text{Remaining margin for data sampling} (\geq 0)$

Cable Skew Typically 10 ps - 40 ps per foot.

Figure 8. FPD87346BXA (FPD-Link Receiver) Input Skew Margin



R/G/B[7]s are MSBs and R/G/B[0]s are LSBs

Figure 9. FPD87346BXA (FPD-Link Receiver) Input Data Mapping

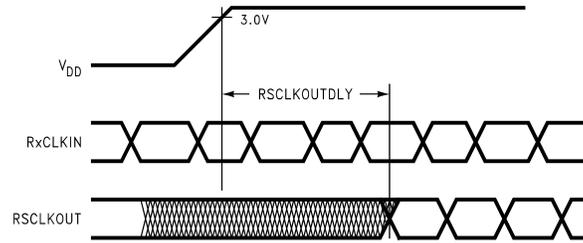


Figure 10. FPD87346BXA (FPD-Link Receiver) Phase Lock Loop Wake-up Time

Output Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TO1	TTL Output Rising from RSCLK Rising	$C_{L(TTL)} = 15 \text{ pF}$, $R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$	0.0		11.25	ns
TO2	TTL Output Falling from RSCK Rising	$C_{L(TTL)} = 15 \text{ pF}$, $R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$	0.0		11.25	ns
RCHP	RSDS Clock (RSCK) High Period	$R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$		5.7		ns
RCLP	RSDS Clock (RSCK) Low Period	$R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$		5.8		ns
RSTU	RS(R,G,B) Setup to Falling or Rising Edge of RSCK	$R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$, $RSDS[2:0] = [000]$		3.2		ns
RHLD	RS(R,G,B) Hold from Falling or Rising Edge of RSCK	$R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$, $RSDS[2:0] = [000]$		1.8		ns
SPSTU	STH Rising to RSCK Falling	$R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$	5.0			ns
SPHLD	STH Falling to RSCK Falling	$R_T = 100\Omega$, $C_{L(RSDS)} = 5 \text{ pF}$, $I_{PI} = 100 \mu\text{A}$, $f = 85 \text{ MHz}$	4.0			ns

Table 1. Typical Simulation Results of RSDS Skew Control Values⁽¹⁾ ($V_{DD} = 3.3\text{V}$; $R_T = 100\text{ohms}$; $I_{PI} = 100 \mu\text{A}$; 25°C)

RSDS[2:0]	f = 65 MHz		f = 85 MHz		Unit
	RSTU	RHLD	RSTU	RHLD	
000	5.03	1.83	3.23	1.83	ns
001	5.26	1.31	3.75	1.31	
010	6.03	0.83	4.23	0.83	
011	6.53	0.33	4.73	0.33	
100	3.01	3.77	1.21	3.77	ns
101	3.49	3.33	1.69	3.33	
110	4.00	2.86	2.20	2.86	
111	4.50	2.36	2.70	2.36	

- (1) The skew control value in the table are only sampling values of a specific condition and is not a parametric value. Typical values on this table are measured under Static and Steady state conditions which may not be reflective of its performance in the end application.

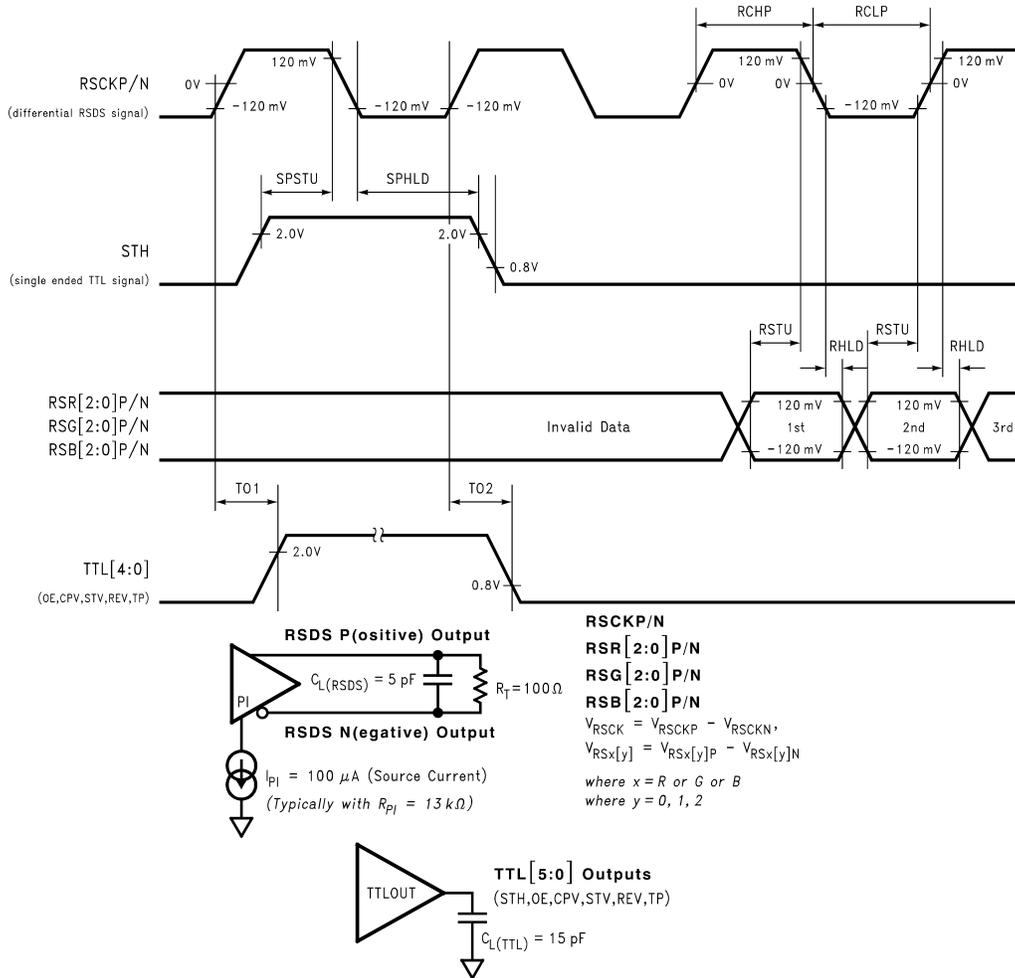
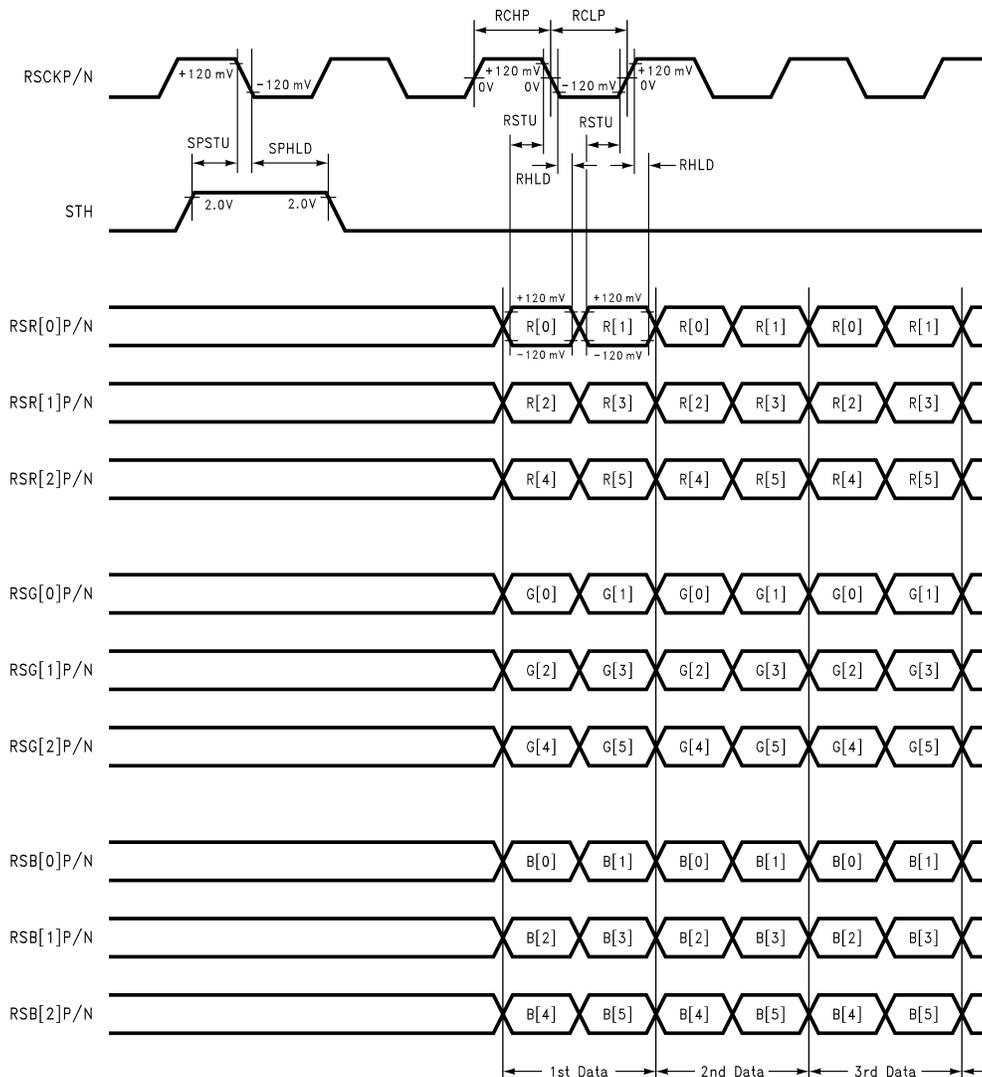


Figure 11. FPD87346BXA RSDS and TTL Output Timing Diagram



Note: RSKP/N, RSR[2:0]P/N, RSG[2:0]P/N and RSB[2:0]P/N are differential outputs, STH is a single ended TTL output.

Figure 12. FPD87346BXA RSDS Output Data Mapping

FPD87346BXA Failure Detect (Internal Bonding Option)

This function is valid in DE mode. As shown in [Figure 13](#), invalid external DE pulse will not affect the internal operation during failure zone.

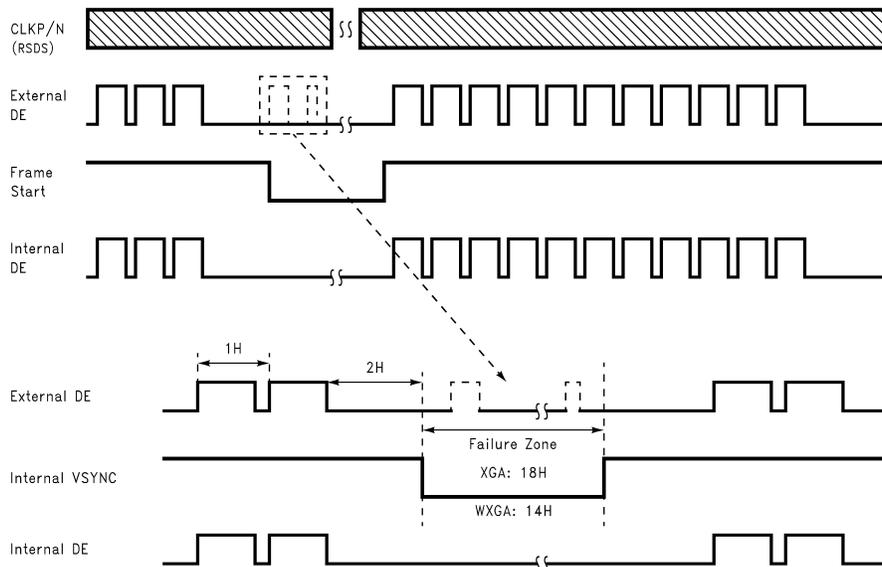


Figure 13. FPD87346BXA Failure Detection

Input Signal Timing

Signal	Item	Symbol		SVGA (800 x 600)	XGA (1024 x 768)	WXGA I (1280 x 768)	WXGA II (1280 x 800)	Unit
Clock Frequency	1/Tclk	f	typ	40	65	82	69	MHz
Vertical Timing	Total	Tv	min	620	772	772	804	Th
			typ	628	806	806	816	
			max	664	850	850	900	
	Active	Tvact	min	–	–	–	–	
			typ	600	768	768	800	
			max	–	–	–	–	
Horizontal Timing	Total	Th	min	1050	1050	1320	1320	Tclk
			typ	1056	1344	1688	1408	
			max	1056	1800	2000	2000	
	Active	Thact	min	–	–	–	–	
			typ	800	1024	1280	1280	
			max	–	–	–	–	

Output Timing—TTL

DE (Data Enable) Mode Only

Parameter	Comments	Display Mode WIDE(0/1) (Pin 57)			Remarks/ Unit
		SVGA (WIDE=0)	XGA (WIDE=0)	WXGA (WIDE=1)	
t1	STH Rising to Active Data	2	2	2	RxCLKP/N
t2	High Duration of STH	1	1	1	RxCLKP/N
t3	STH Rising to TP	1031	1031	1285	RxCLKP/N
t4	High Duration of TP	8	8	10	RxCLKP/N
t5	STH Rising to OE	904	904	1147	RxCLKP/N
t6	High Duration of OE	159	159	180	RxCLKP/N
t7	STH Rising to CPV	1031	1031	1283	RxCLKP/N

Parameter	Comments	Display Mode WIDE(0/1) (Pin 57)			
		SVGA (WIDE=0)	XGA (WIDE=0)	WXGA (WIDE=1)	Remarks/ Unit
t8	High Duration of CPV	684	684	724	RxCLKP/N
t9	STH Rising to STV	368	368	565	RxCLKP/N
t10	High Duration of STV	1	1	1	H Line ⁽¹⁾
t11	STH Rising to REV (1HRVS)	390	390	567	RxCLKP/N
t12	High/Low Duration of REV (1HRVS)	1	1	1	H Line ⁽¹⁾
t13	STH Rising to REV (2HRVS)	371	371	567	RxCLKP/N
t14	High/Low Duration of REV (2HRVS)	2	2	2	H Line ⁽¹⁾

(1) H Line: Hsync Cycle

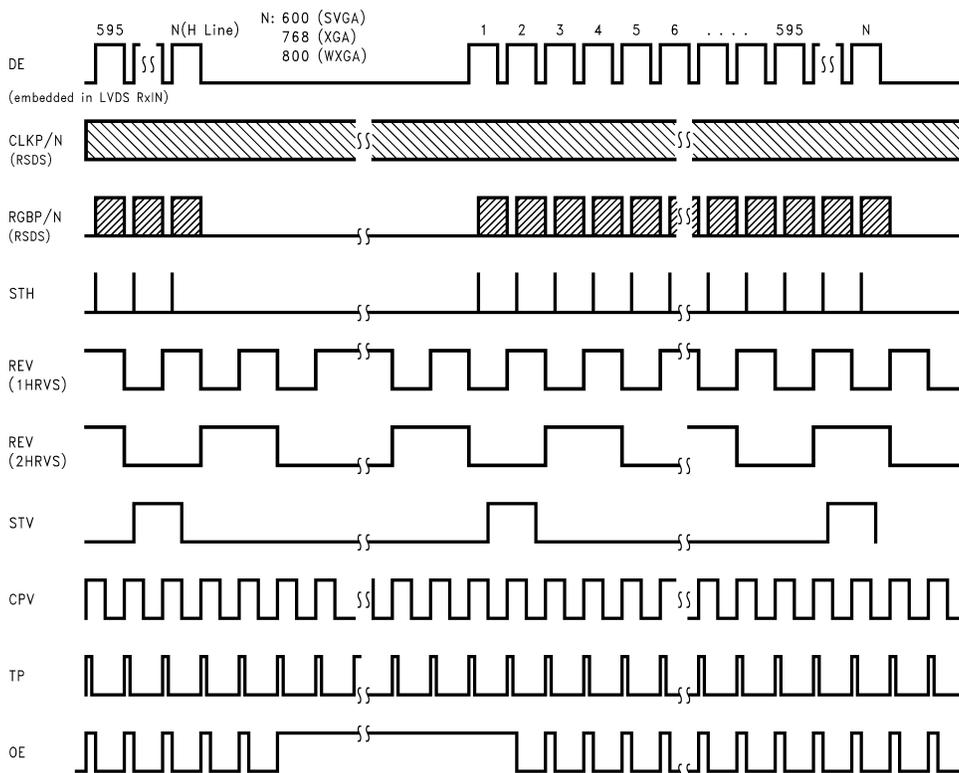
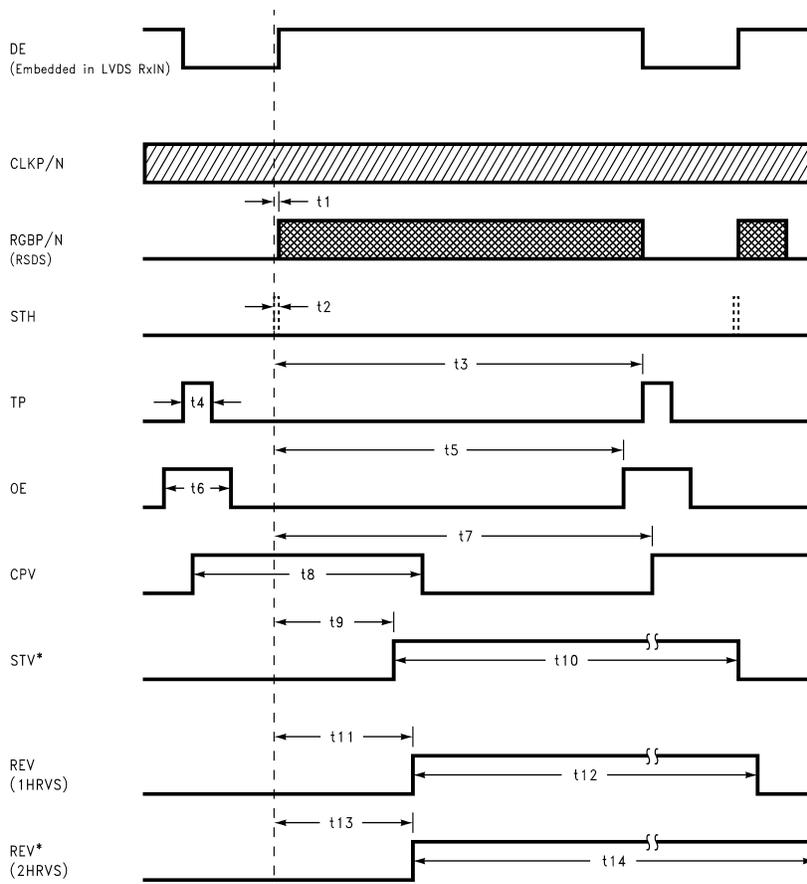


Figure 14. FPD87346BXA TTL Output Timing Diagram



* Timing based on first occurrence of STH signal to the left of the measured output.

Unit: Output pixel clock; CLKP/N: RxCLKP/N

Figure 15. FPD87346BXA TTL Output Timing Diagram (continued)

Table 2. RON(Sn) Configuration⁽¹⁾

RO2 (S2)	RO1 (S1)	RO0 (S0)	REV	OE		TP		Unit
				XGA (Front)	WXGA (Back)	XGA	WXGA	
0	0	0	1HRVS	2.4	2.1	0.12	0.12	μs
0	0	1	2HRVS			0.12	0.12	
0	1	0	2HRVS			0.25	0.50	
0	1	1	1HRVS	2.9	2.6	0.12	0.12	
1	0	0	2HRVS			0.12	0.12	
1	0	1	2HRVS			0.25	0.50	
1	1	0	1HRVS	3.4	3.1	0.25	0.50	
1	1	1	2HRVS			0.25	0.50	

(1) (T_A = 25°C; XGA: RxCLKP/N = 65 MHz; WXGA: RxCLKP/N = 85 MHz)

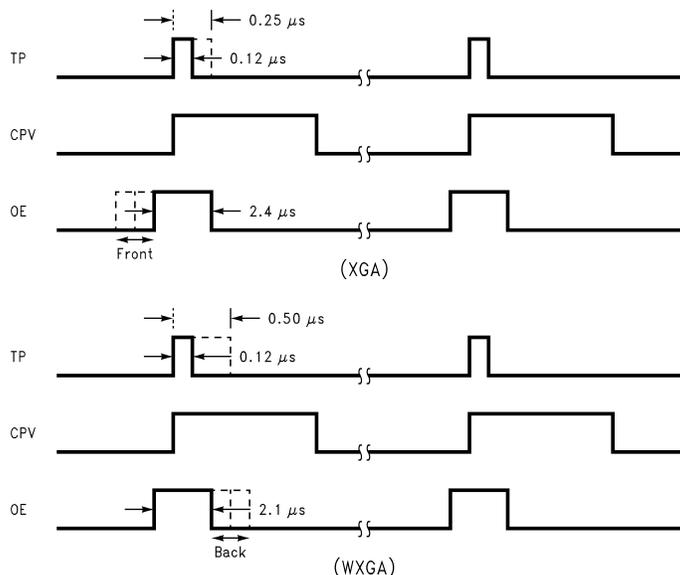


Figure 16. FPD87346BXA ROn (Sn) Configuration Timing Diagrams

Pin Connection

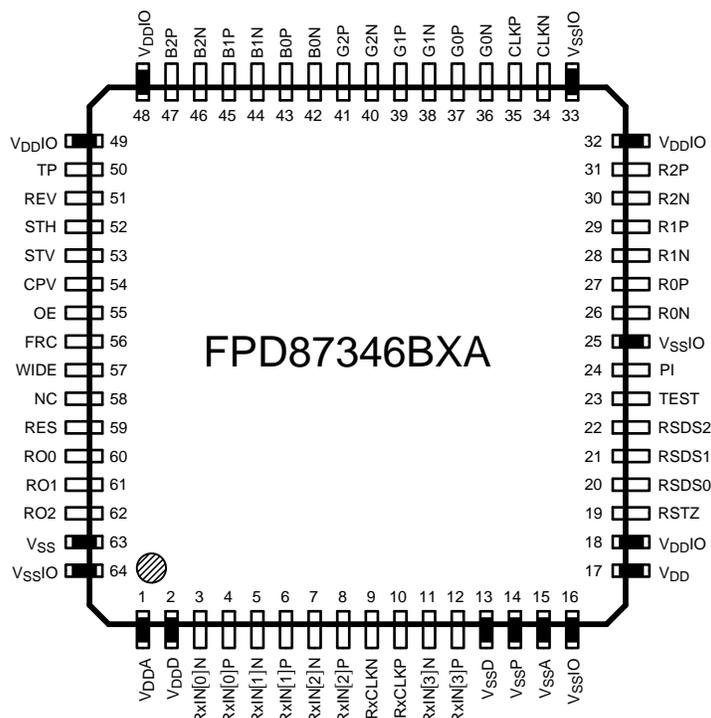


Figure 17. Pinout Assignments

Pin Description

Table 3. System Interface

Symbol	Pin	Type	Function
RxIN[0]P/N	3, 4	LVDSI	FPD-Link Data Differential Pair 0 Input
RxIN[1]P/N	5, 6	LVDSI	FPD-Link Data Differential Pair 1 Input
RxIN[2]P/N	7, 8	LVDSI	FPD-Link Data Differential Pair 2 Input
RxIN[3]P/N	11, 12	LVDSI	FPD-Link Data Differential Pair 3 Input
RxCLKP/N	9, 10	LVDSI	FPD-Link Clock Differential Pair Input
Sub-Total Pin Count	10		

Table 4. Column Driver Interface

Symbol	Pin	Type	Function
R[2:0]P/N	26–31	RSO	Red Reduced Swing Differential Outputs to Column Drivers
G[2:0]P/N	36–41	RSO	Green Reduced Swing Differential Outputs to Column Drivers
B[2:0]P/N	42–47	RSO	Blue Reduced Swing Differential Outputs to Column Drivers
CLKP/N	34, 35	RSO	Clock Reduced Swing Differential Outputs to Column Drivers
TP	50	TO, 8mA	Line Latch Signal Output to Column Drivers
STH	52	TO, 24mA	Horizontal Start Signal Output to Column Drivers
REV	51	TO, 8mA	Alternative Signal Output for each 1 or 2 Horizontal Line to Column Drivers and LC Control
Sub-Total Pin Count	23		

Table 5. Row Driver Interface

Symbol	Pin	Type	Function
STV	53	TO, 6mA	Row Driver Start Pulse
CPV	54	TO, 6mA	Row Driver Shift Clock
OE	55	TO, 6mA	Control TFT Gate Pulse Width to Row Drivers
Sub-Total Pin Count	3		

Table 6. Control Pins

Symbol	Pin	Type	Function
FRC	56	I	Data Dithering Option: 0: 8-Bit Input, Dithering (FRC) 1: 6-Bit Input, Non Dithering (No FRC)
RSDS[2:0]	20–22	I	RSDS Skew/Timing Control (See Table 1)
WIDE	57	I	0: SVGA (800 x 600) 0: XGA (1024 x 768) 1: WXGA (1280 x 768/800)
RO[2:0]	60–62	I	Alternate each 1 Horizontal/2 Horizontal on REV with OE Timing (See Table 2 and Figure 16)
RES	59	I	Reserved pin, tie to high (V _{DD})
TEST	23	I	0: Normal Operation 1: Test Mode
Sub-Total Pin Count	10		

Table 7. Power Supply

Symbol	Pin	Type	Function
V _{DD}	17	P	Digital Power for Logic Core and LVDS Deserializer
V _{SS}	63	G	Digital Ground for Logic Core and LVDS Deserializer
V _{DDIO}	18, 32, 48, 49	P	Digital I/O Power and RSDS Outputs
V _{SSIO}	16, 25, 33, 64	G	Digital I/O Ground and RSDS Outputs
V _{DDA}	1	P	Power for LVDS PLL and Analog Bandgap
V _{DDD}	2	P	Digital Power for LVDS Input Buffer
V _{SSD}	13	G	Digital Ground for LVDS Input Buffer
V _{SSP}	15	G	Ground for LVDS PLL and Analog Bandgap
V _{SSA}	14	G	Ground for LVDS PLL and Analog Bandgap
Sub-Total Pin Count	15		

Table 8. Other

Symbol	Pin	Type	Function
PI	24	I	Reference for Reduced Swing Differential Outputs
RSTZ	19	I	System Reset; Active Low
NC	58	I	No Connect
Sub-Total Pin Count	3		
Total Pin Count	64		System Interface = 10 Column Driver = 23 Row Driver = 3 Control Pins = 10 Power Supply = 15 Other = 3

Table 9. Bonding Options (B/O)

Symbol	Pin	Type	Function
FAIL_ON	B/O	PD	Failure Detect Function ON/OFFLow : OFF (Default) High : ON

Pin Types

- I** -Input (LVTTTL-Compatible)
- TO** -TTL Output (LVTTTL-Compatible)
- LVDSI** -Low Voltage Differential Signal Input
- RSO** -Reduced Swing Differential Output
- P** -Power
- G** -Ground
- B/O** -Bonding Option
- PD** -Internal Pull-Down
- PU** -Internal Pull-Up

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video
TI E2E Community	e2e.ti.com