



ON Semiconductor®

August 2017

FPF2498 Adjustable OVP with 28 V Input OVT Load Switch

Features

Function	Advanced Load Switch
Input	3.5 – 12 V
Features	28 V Absolute Ratings on VIN 1.7 A Maximum Continuous Current Capability 80 mΩ R _{ON} Typical Over-Voltage Protection (OVP) Over-Current Protection (OCP) Thermal Shutdown Under-Voltage Lockout (UVLO) Reverse Current Blocking (RCB)
ESD	15 kV IEC 61000-4-2 Air Gap
Operating Temperature Range	-40 to +85°C
Package	6-Ball WLCSP (1.05 x 1.3 x 0.625 mm, 0.4 mm Pitch)
Ordering Information	FPF2498BUCX
Top Mark	TK

Description

The FPF2498 advanced load-management switch targets applications requiring a highly integrated solution. It disconnects loads powered from the DC power rail (<12 V) with stringent off-state current targets and high load capacitances (<100 μF). The FPF2498 consists of a slew-rate controlled low-impedance MOSFET switch. FPF2498 has over-voltage protection and over-temperature protection.

Applications

- Cellular Phones, Smart Phones
- Tablets

Related Resources

- FPF2498 Evaluation Board*

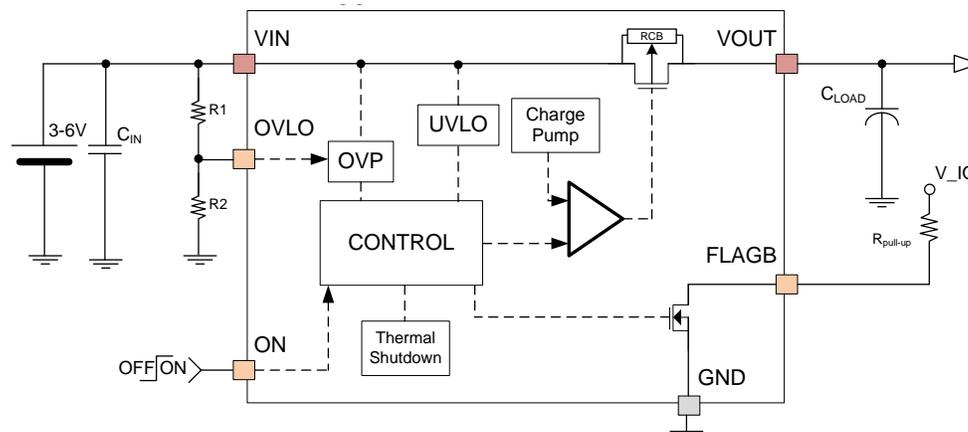


Figure 1. Block Diagram and Typical Application

Note:

1. Recommend C_{LOAD} value be larger than 2.2 μF.

Pin Configuration

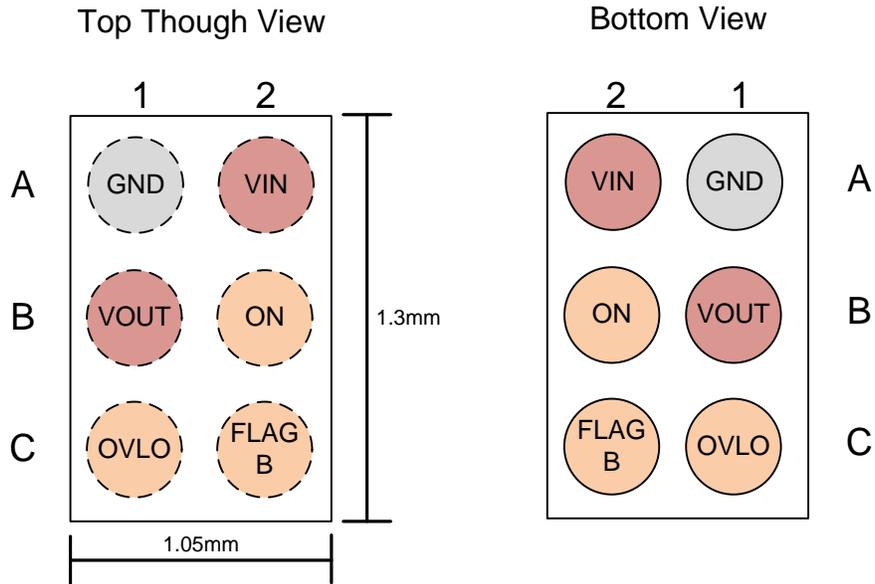


Figure 2. Pin Assignments

Pin Map

Name	Pin #	Type	Default State	Description	
VIN	A2	Input	N/A	Input voltage path	
VOUT	B1	Output	N/A	Output voltage path	
ON	B2	Input	LOW	On / Off control of device	V_{IH} =HIGH Enabled
					V_{IL} =LOW Disabled
OVLO	C1	Input		OVP Adjustment set by R1 and R2 and is compared to $1.2 V - V_{IN} \times R2 / (R1+R2) > 1.2 V$	
FLAGB	C2	Open-Drain Output	High-Z	Indicates a OVP / OCP / OTP fault	LOW / GND Active – Indicates: OVP (over 6.5 V at 3 – 6 V) OCP (over 2 A) OTP (over 150°C)
					HIGH / V _{IO} Normal Operation
GND	A1	GND	GND	Device ground	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters	Min.	Max.	Unit
V _{PIN}	Voltage on VIN to GND, VIN to VOUT, OVLO Pins	-0.3	28.0	V
	Voltage on ON, FLAGB Pins	-0.3	6.0	
	Voltage on VOUT to GND Pins	-0.3	20.0	
I _{SW}	Maximum Switch Current		1.75	A
t _{PD}	Total Power Dissipation at T _A =25°C		1	W
T _J	Operating Junction Temperature	-40	+150	°C
T _{STG}	Storage Junction Temperature	-65	+150	°C
Θ _{JA}	Thermal Resistance, Junction-to-Ambient (1-inch Square Pad of 2 oz. Copper)		95 ⁽²⁾	°C/W
			110 ⁽³⁾	
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS-001-2012	3	kV
		Charged Device Model, JESD22-C101	2	
	IEC61000-4-2 System Level	Air Discharge (V _{IN} , V _{ON} , V _{OUT} to GND)	15	
		Contact Discharge (V _{IN} , V _{ON} , V _{OUT} to GND)	8	

Notes:

- Measured using 2S2P JEDEC std. PCB.
- Measured using 2S2P JEDEC PCB cold plate method.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameters	Min.	Max.	Unit
V _{IN}	Supply Voltage	3.5	12.0	V
I _{SW}	Maximum Continuous Switch Current ⁽⁴⁾		1.7	A
T _A	Ambient Operating Temperature	-40	85	°C

Note:

- Maximum Junction Temperature = 85°C

Electrical Characteristics

Unless otherwise noted; $V_{IN}=3.5$ to 5.5 V, $T_A=-40$ to $+85^\circ\text{C}$; typical values are at $V_{IN}=5$ V and $T_A=25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
$I_{SD(OFF)}$	Shutdown Current	$V_{IN}=5.5$ V, $V_{OUT}=0$ V, $V_{ON}=GND$		0.4	3.0	μA
I_Q	Quiescent Current	$V_{IN}=5.5$ V, $V_{OUT}=\text{Floating}$, $I_{OUT}=0$ mA		90	125	μA
R_{ON}	On Resistance	$V_{IN}=3.7$ V, $I_{OUT}=200$ mA		90		m Ω
		$V_{IN}=5.0$ V, $I_{OUT}=200$ mA		80	95(5)	
		$V_{IN}=9$ V, $I_{OUT}=200$ mA				
		$V_{IN}=12$ V, $I_{OUT}=200$ mA				
V_{IH}	ON Input Logic HIGH Voltage	$V_{IN}=3.5$ V to 5.5 V	1.15			V
V_{IL}	ON Input Logic LOW Voltage	$V_{IN}=3.5$ V to 5.5 V			0.65	V
V_{OL_FLAG}	FLAGB Output Logic LOW Voltage	$V_{IN}=5$ V, $I_{SINK}=1$ mA		0.10	0.20	V
I_{FLAGB_LK}	FLAGB Output HIGH Leakage Current	$V_{IN}=5$ V, Switch On			0.5	μA
RPD	Pull-Down Resistance on ON Pin	$V_{IN}=5$ V, $OVLO=GND$		3		M Ω
Over-Voltage Protection						
V_{OV_TRIP}	Default Input OVP Lockout	V_{IN} Rising Threshold $OVLO=GND$	6.2	6.5	6.8	V
		V_{IN} Falling Threshold $OVLO=GND$		6.2		
V_{OVLO_SEL}	Voltage threshold for $OVLO$ selection	$V_{IN}=3.5$ V to 5.5 V, $OVLO=GND$		0.3		V
V_{OVP_HYS}	Input OVP Hysteresis	V_{IN} Falling Threshold $OVLO=\text{External Setting}$		0.3		V
V_{OVLO_TH}	$OVLO$ Set Threshold	$V_{IN}=3.5$ to V_{OVLO}		1.20		V
t_{OVP}	Response Time	$I_{OUT}=0.5$ A, $C_L=0$ μF , $T_A=25^\circ\text{C}$, $V_{IN}=6$ V to 7 V		0.5	1	μs
V_{UVLO}	Under-Voltage Lockout	V_{IN} Rising		3.2		V
		V_{IN} Falling		3.0		
V_{UVLO_HYS}	UVLO Hysteresis			200		mV
I_{RCB}	RCB Current	$V_{ON}=0$ V, $V_{OUT}=5.5$ V, $V_{IN}=0$ V		2	5	μA
TSD	Thermal Shutdown	Shutdown Threshold		150		$^\circ\text{C}$
		Return from Shutdown		130		
		Hysteresis		20		
Over-Current Protection						
I_{OCP}	Over-Current Protection Trip Point	$I_{SW} > I_{OCP}$		2		A
Dynamic Characteristics						
t_{DON}	Turn-On Delay ⁽⁷⁾	$V_{IN}=5$ V, $R_L=100$ Ω , $C_L=10$ μF , $T_A=25^\circ\text{C}$		4.3		ms
t_R	V_{OUT} Rise Time ⁽⁷⁾			3.0		ms
t_{ON}	Turn-On Time ⁽⁸⁾			7.3		ms
t_{DOFF}	Turn-Off Delay ^(6,7)			600		μs
t_F	V_{OUT} Fall Time ^(6,7)			2.0		ms
t_{OFF}	Turn-Off Time ^(6,9)			2.5		ms
t_{READY}	Time for Device Ready for Large Load Current ⁽¹⁰⁾	$C_L=10$ μF		5		ms

Continued on the following page...

Electrical Characteristics

Unless otherwise noted; $V_{IN}=3.5$ to 5.5 V, $T_A=-40$ to $+85^\circ\text{C}$; typical values are at $V_{IN}=5$ V and $T_A=25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{RESTART}	Over-Current Blanking Time ⁽⁶⁾	$V_{IN}=5$ V $I_{OUT} \geq 1.7$ A		64		ms
t_{OCP}	Over-Current Response Time ⁽⁶⁾	Moderate Over-Current Condition; $I_{OUT} \geq I_{LIM}$ $V_{OUT} \leq V_{IN}$		4		μs
t_{HOCP}	Hard Over-Current Response Time	Moderate Over-Current Condition; $I_{OUT} \geq I_{LIM}$ $V_{OUT} \leq 0$ V		3		μs
$t_{\text{FLAG_Release}}$	Over-Current/Voltage/Temp. Flag Release Time ⁽⁶⁾	Time for Flag to Release when Fault Condition Removed		100		ms

Notes:

5. $T_A=25^\circ\text{C}$.
6. This parameter is guaranteed by design and characterization; not production tested.
7. $t_{\text{DON}}/t_{\text{DOFF}}/t_{\text{R}}/t_{\text{F}}$ are defined in figure below.
8. $t_{\text{ON}}=t_{\text{R}} + t_{\text{DON}}$.
9. $t_{\text{OFF}}=t_{\text{F}} + t_{\text{DOFF}}$.
10. After t_{READY} , the device is ready for maximum DC current load condition.

Timing Diagram

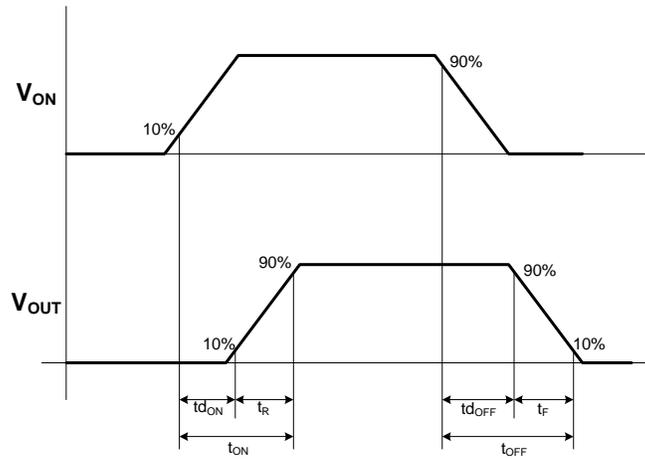


Figure 3. Timing Diagram

where:

- t_{dON} =Delay On Time;
- t_r = V_{OUT} Rise Time;
- t_{ON} =Turn-On Time;
- t_{dOFF} =Delay Off Time;
- t_f = V_{OUT} Fall Time; and
- t_{OFF} =Turn Off Time.

Device Fault Behavior Timing

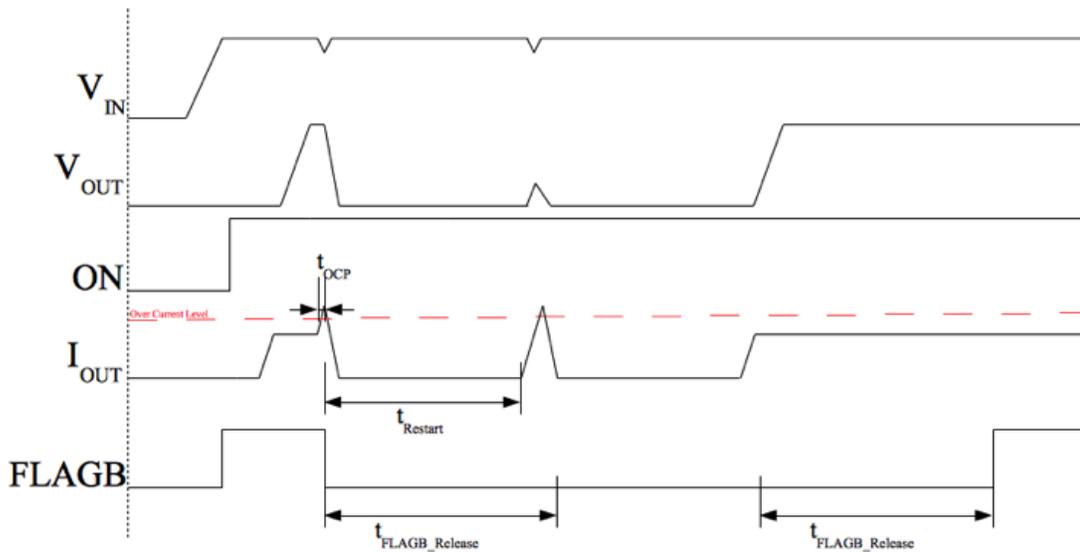


Figure 4. OCP Turn-Off Timing Diagram

Operation and Application Description

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into discharge load capacitor; a capacitor must be placed between the VIN and GND pins. A high-value CIN capacitor can be used to reduce the voltage drop in high-current applications.

Output Capacitor

An output capacitor should be placed between the VOUT and GND pins. This capacitor prevents parasitic board inductance from forcing VOUT below ground when the switch is on. This capacitor also prevents reverse inrush current from creating a voltage spike that could damage the device in the case of a VOUT short.

Fault Reporting

Upon the detection of an over-voltage, over-current, or over-temperature condition, the FLAGB signals the fault by activating LOW.

Under-Voltage Lockout (UVLO)

The under-voltage lockout turns the switch off if the input voltage drops below the lockout threshold. With the ON pin active, the input voltage rising above the UVLO threshold releases the lockout and enables the switch.

Over-Voltage Lockout (OVLO)

The OVLO pin sets the over-voltage lockout trip point with a resistor-divider network. OVLO adjustment is set by R1 and R2 and is compared to $1.2\text{ V} - V_{IN} \times R2 / (R1+R2) > 1.2\text{ V}$. when $V_{IN} > V_{OVLO}$ the switch turns off to ensure protection to devices connected to VOUT. A 1 MΩ or larger resistor is recommended on R1 to reduce standby power consumption. To use the default values of 6.5 V for VOVLO, connect the OVLO pin directly to GND.

Package Specific Dimensions

D	E	X	Y
1.300±0.030	1.050±0.030	0.325	0.250

Reverse-Current Blocking (RCB)

The reverse-current blocking feature protects the input source against current flow from output to input. When the load switch is OFF, no current flows from the output to input.

Thermal Shutdown (TSD)

Thermal shutdown protects the die from internally or externally generated excessive temperature. During an over-temperature condition, the switch is turned off. The switch automatically turns on again if the temperature of the die drops below the threshold temperature.

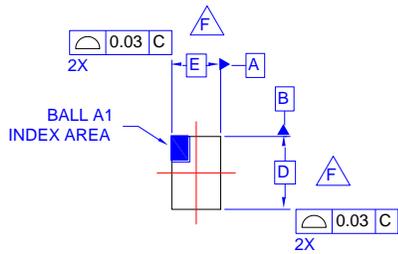
Current Limit

The current limit ensures that the current flow through the switch doesn't exceed a maximum value, which can damage the device. If the current flow through the switch exceeds the trip point, the switch turns off and enters the blanking time. After the blanking time, the switch is re-enabled and checks if the fault still exists.

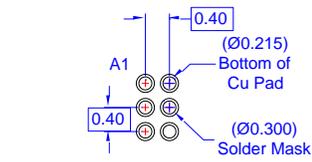
Board Layout

For best performance, all traces should be as short as possible. The input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, GND minimizes parasitic electrical effects along with minimizing the case-to-ambient thermal impedance.

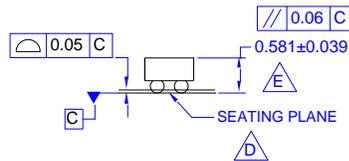
Physical Dimensions



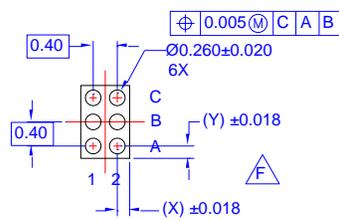
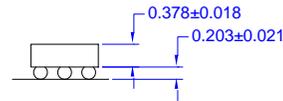
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 581 ± 39 MICRONS (542-620 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC006AR REV1.

Figure 5. 6-Ball, Wafer-Level Chip-Scale Package (WLCSP), 2x3 Array, 0.4 mm Pitch

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