



# FQN1N60C 600V N-Channel MOSFET

#### **Features**

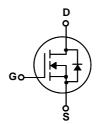
- 0.3 A, 600 V,  $R_{DS(on)}$  = 11.5  $\Omega$  @  $V_{GS}$  = 10 V
- Low gate charge (typical 4.8 nC)
- Low Crss (typical 3.5 pF)
- · Fast switching
- 100 % avalanche tested
- · Improved dv/dt capability

## **Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.





# **Absolute Maximum Ratings**

Symbol	Parameter			FQN1N60C	Units
V <sub>DSS</sub>	Drain-Source V	Drain-Source Voltage		600	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		25°C)	0.3	A
		- Continuous (T <sub>C</sub> = 1	100°C)	0.18	A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	1.2	A
$V_{GSS}$	Gate-Source Vo	ource Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed A	Single Pulsed Avalanche Energy (Note 2)		33	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)		(Note 1)	0.3	A
E <sub>AR</sub>	Repetitive Avala	Lepetitive Avalanche Energy (Note 1)		0.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		(Note 3)	4.5	V/ns
$P_{D}$	Power Dissipation (T <sub>A</sub> = 25°C)			1	W
	Power Dissipation (T <sub>L</sub> = 25°C)			3	W
	- Derate above 25°C			0.02	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		Range	-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		ing purposes,	300	°C

#### **Thermal Characteristics**

Symbol	Parameter		Тур	Max	Units
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	(Note 6a)		50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 6b)		140	°C/W

# **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1N60C	FQN1N60C	TO-92			2000ea

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter Test Conditions		Min.	Тур.	Max.	Units
Off Characte	ristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	600			V
ΔBV <sub>DSS</sub> / ΔΤ <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.6		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V			50	μΑ
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C			250	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Characte	ristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.15 A		9.3	11.5	Ω
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 0.3 \text{ A}$ (Note 4)		0.75		S
Dynamic Cha				ı	ı	T
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$		130	170	pF
C <sub>oss</sub>	Output Capacitance	- 1.5 Will 2		19	25	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			3.5	6	pF
Switching Ch	naracteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 1.1 A,		7	24	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		21	52	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		1	13	36	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4, 5)		27	64	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 1.1 A,		4.8	6.2	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		0.7		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4, 5)		2.7		nC
Drain-Source	e Diode Characteristics and Maximum R	atings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				0.3	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				1.2	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.3 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.1 A,		190		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s \qquad (Note 4)$		0.53		μС

- 1. Repetitive Rating : Pulse width limited by maximum junction temperature
- 2. L = 59mH, I  $_{AS}$  = 1.1A, V  $_{DD}$  = 50V, R  $_{G}$  = 25  $\Omega,$  Starting  $\,$  T  $_{J}$  = 25  $^{\circ}C$
- $3.~I_{SD} \leq 0.3A,~di/dt \leq 200A/\mu s,~V_{DD} \leq BV_{DSS,}~Starting~~T_J = 25^{\circ}C$
- 4. Pulse Test : Pulse width  $\leq 300 \mu s, \ Duty \ cycle \leq 2\%$
- 5. Essentially independent of operating temperature

- 6. a) Reference point of the R<sub>0,IL</sub> is the drain lead
  b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment
  (R<sub>0,JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance. R<sub>0</sub>CA is determined by the user's board design)

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

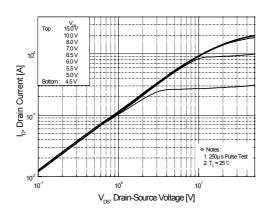


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

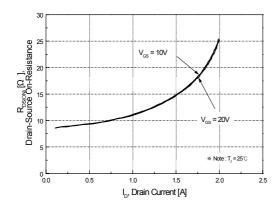


Figure 5. Capacitance Characteristics

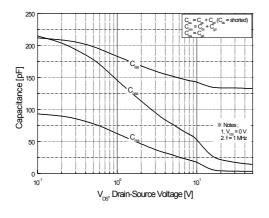


Figure 2. Transfer Characteristics

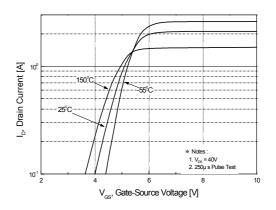
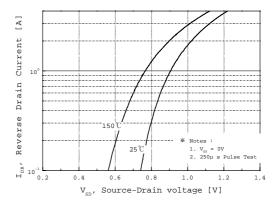
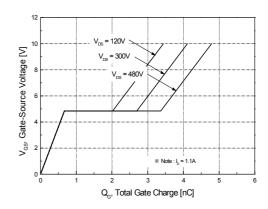


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue



**Figure 6. Gate Charge Characteristics** 



# **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

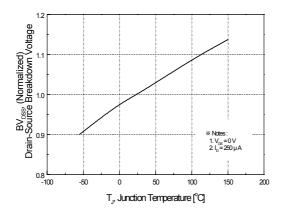


Figure 9. Maximum Safe Operating Area

Figure 8. On-Resistance Variation vs. Temperature

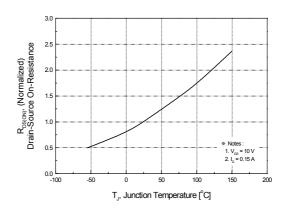
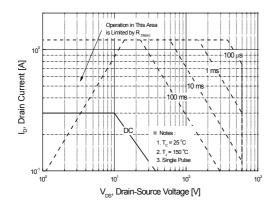


Figure 10. Maximum Drain Current vs. Case Temperature



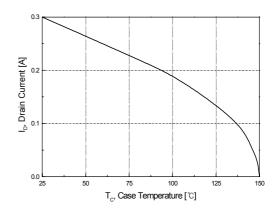
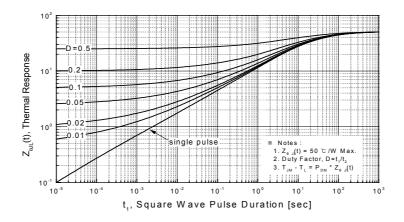
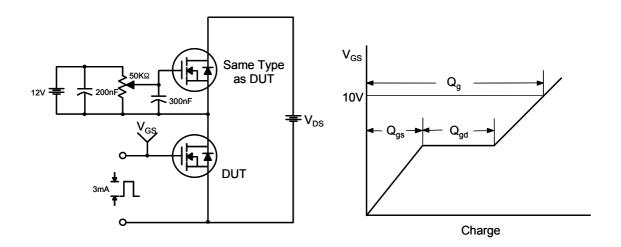


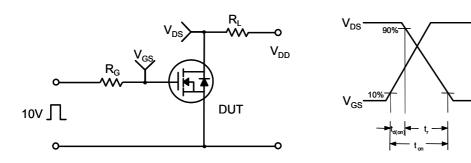
Figure 11. Transient Thermal Response Curve



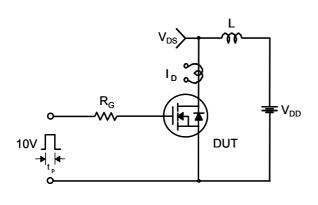
## **Gate Charge Test Circuit & Waveform**

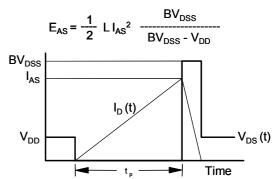


#### **Resistive Switching Test Circuit & Waveforms**

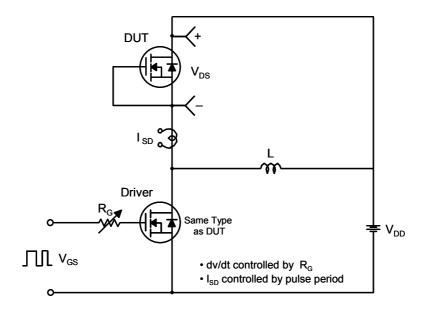


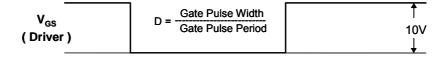
#### **Unclamped Inductive Switching Test Circuit & Waveforms**

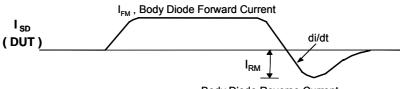




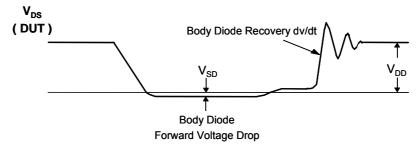
## Peak Diode Recovery dv/dt Test Circuit & Waveforms





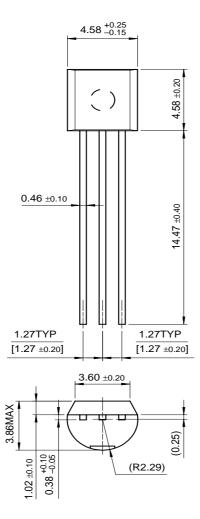


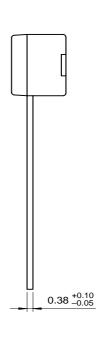
**Body Diode Reverse Current** 



## **Mechanical Dimensions**

**TO-92** 





Dimensions in Millimeters

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