FAIRCHILD SEMICONDUCTOR®

March 2008

QFET®

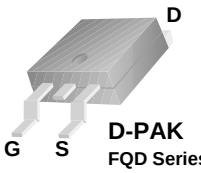
FQD3N50C / FQU3N50C
500V N-Channel MOSFET

Features

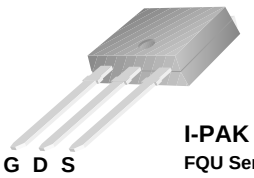
- 2.5A, 500V, $R_{DS(on)}$ = 2.5Ω @V_{GS} = 10 V
- Low gate charge (typical 10 nC)
- Low Crss (typical 8.5pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

Description

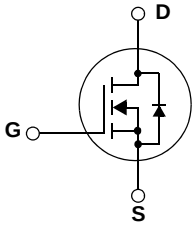
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



D-PAK
FQD Series



I-PAK
FQU Series



Absolute Maximum Ratings

Symbol	Parameter		FQD3N50C/FQU3N50C	Units
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_C = 25°C)		2.5	A
	- Continuous (T_C = 100°C)		1.5	A
I_{DM}	Drain Current - Pulsed	(Note 1)	10	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	200	mJ
I_{AR}	Avalanche Current	(Note 1)	2.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		35	W
	- Derate above 25°C		0.28	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD3N50C	FQD3N50CTM	D-PAK	380mm	16mm	2500
FQD3N50C	FQD3N50CTF	D-PAK	380mm	16mm	2500
FQU3N50C	FQU3N50CTU	I-PAK	-	-	70

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.7	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.25 A	--	2.1	2.5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 1.25 A (Note 4)	--	1.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	280	365	pF
C_{oss}	Output Capacitance		--	50	65	pF
C_{rss}	Reverse Transfer Capacitance		--	8.5	11	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 2.5A, R_G = 25 Ω (Note 4, 5)	--	10	30	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
t_f	Turn-Off Fall Time		--	25	60	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 2.5A, V_{GS} = 10 V (Note 4, 5)	--	10	13	nC
Q_{gs}	Gate-Source Charge		--	1.5	--	nC
Q_{gd}	Gate-Drain Charge		--	5.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.5 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 3 A, dI_F / dt = 100 A/μs (Note 4)	--	170	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.7	--	μC

NOTES:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 58mH, I_{AS} =2.5A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 2.5A, di/dt ≤200A/μs, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

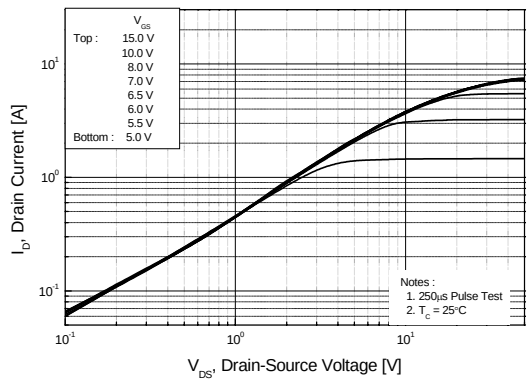


Figure 2. Transfer Characteristics

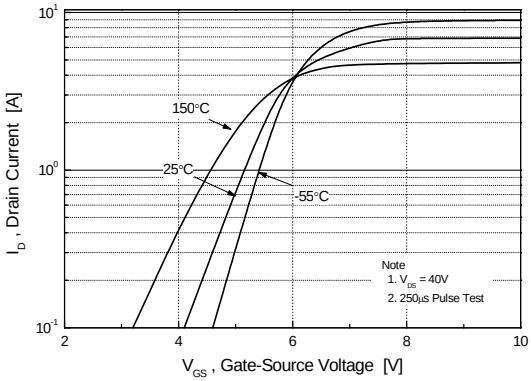


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

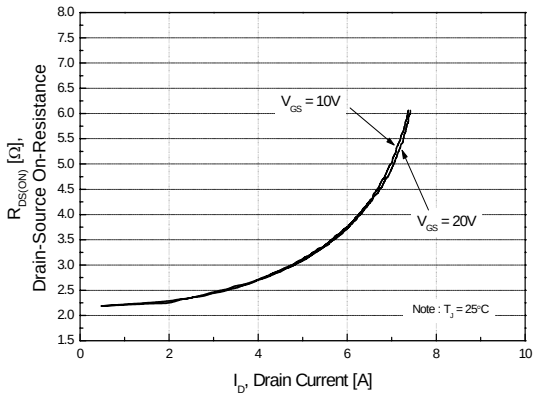


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

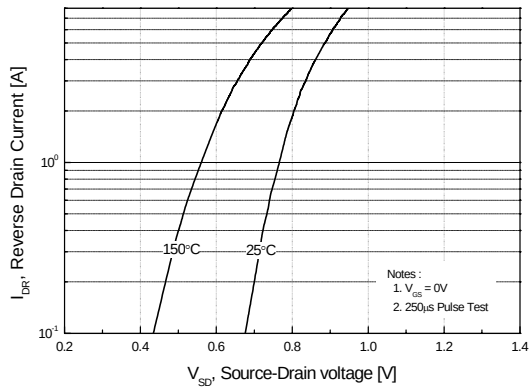


Figure 5. Capacitance Characteristics

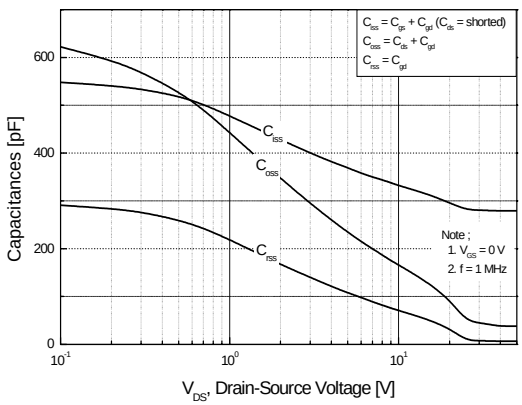
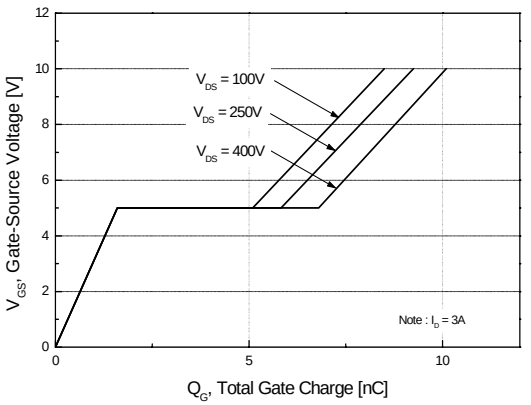


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

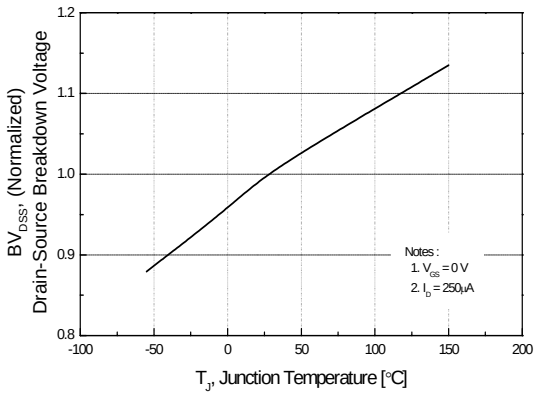


Figure 8. On-Resistance Variation vs. Temperature

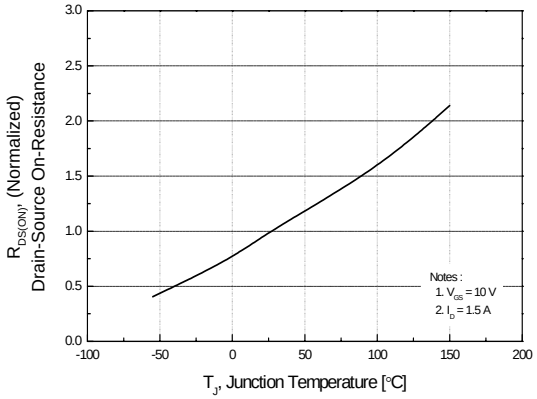


Figure 9. Maximum Safe Operating Area

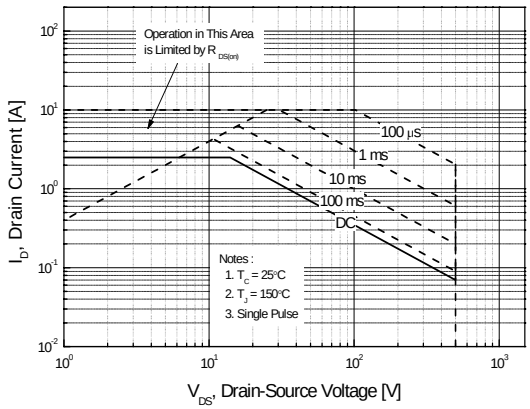


Figure 10. Maximum Drain Current vs. Case Temperature

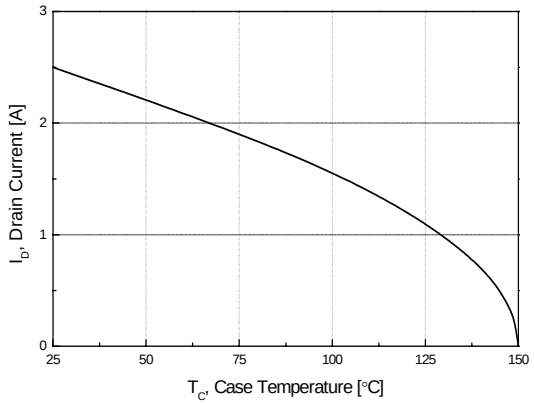
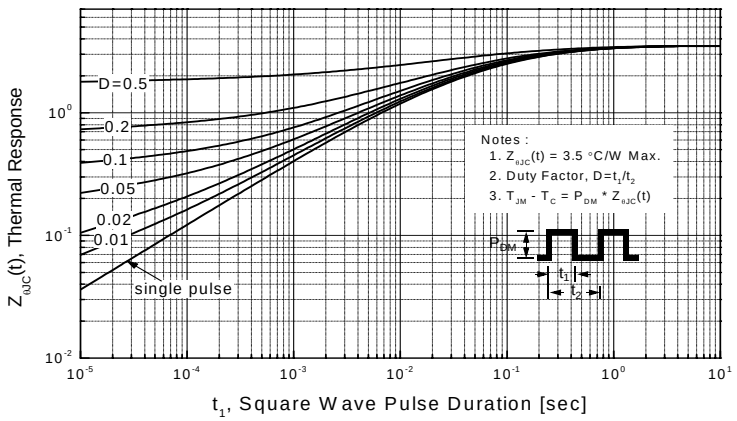
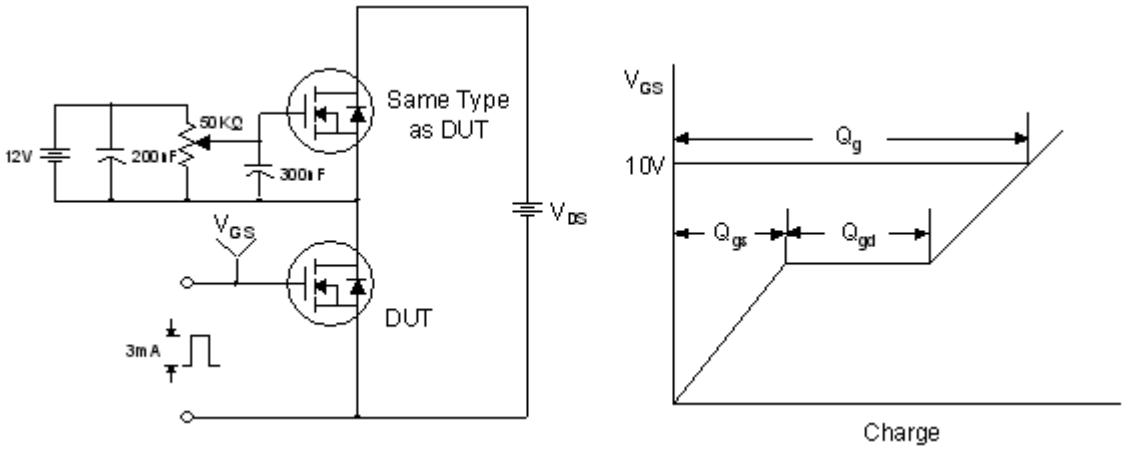


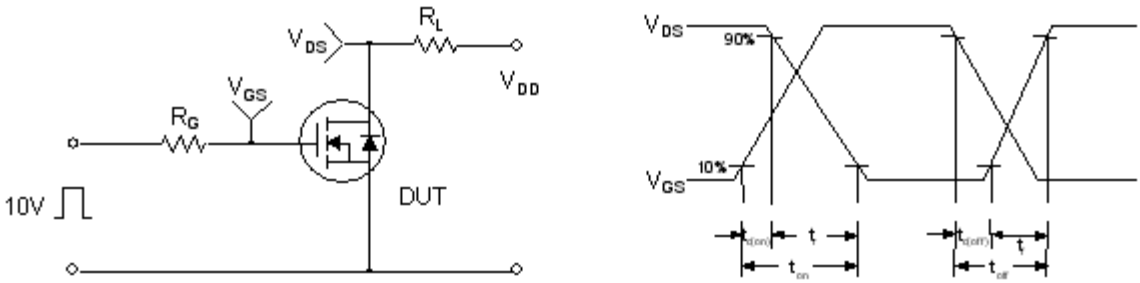
Figure 11. Transient Thermal Response Curve



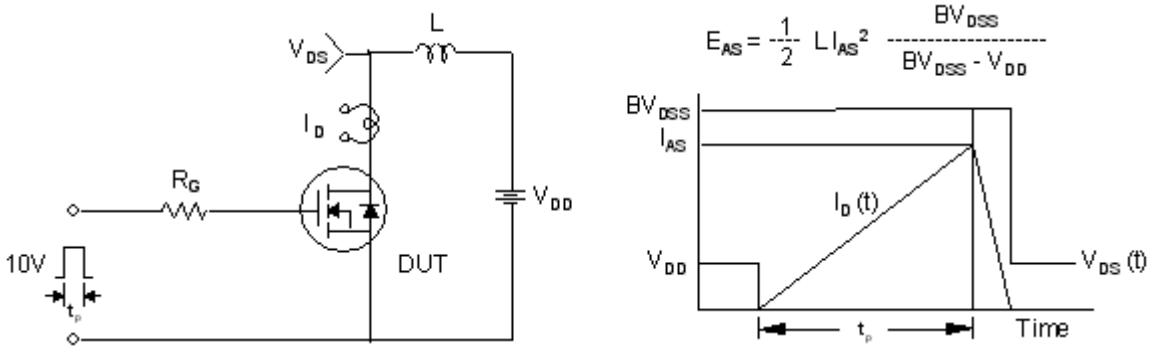
Gate Charge Test Circuit & Waveform



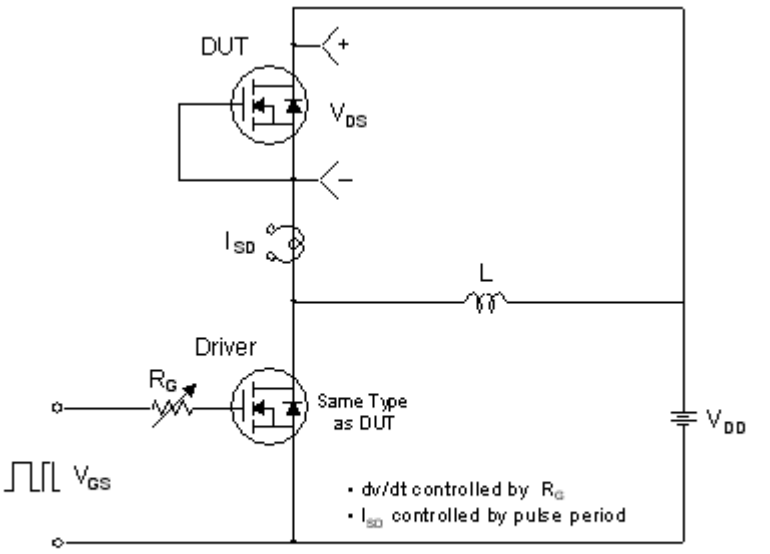
Resistive Switching Test Circuit & Waveforms

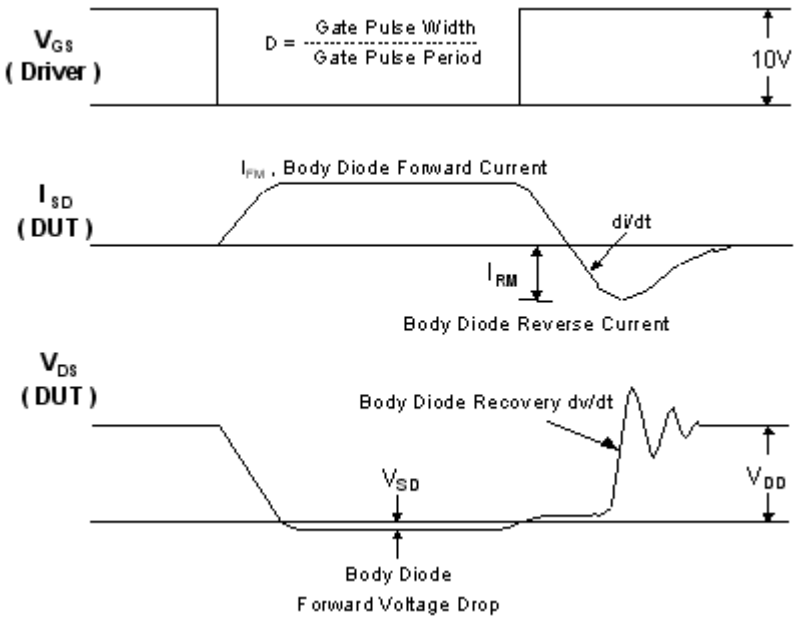


Unclamped Inductive Switching Test Circuit & Waveforms



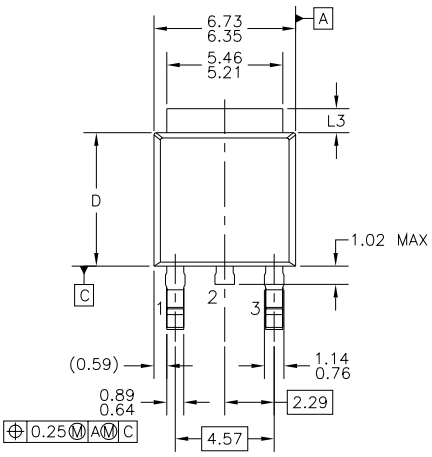
Peak Diode Recovery dv/dt Test Circuit & Waveforms

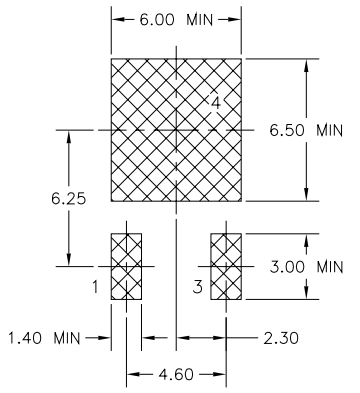




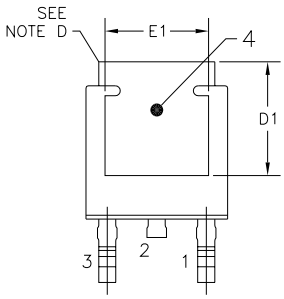
Mechanical Dimensions

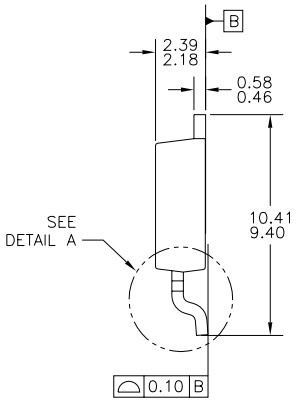
D-PAK

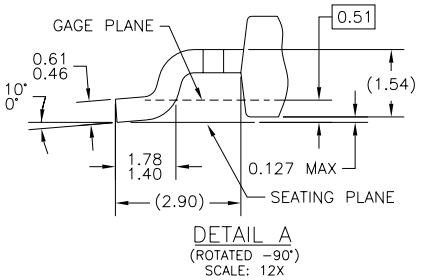




LAND PATTERN RECOMMENDATION







DETAIL A
(ROTATED −90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

E) DIMENSIONS L3,D,E1&D1 TABLE:

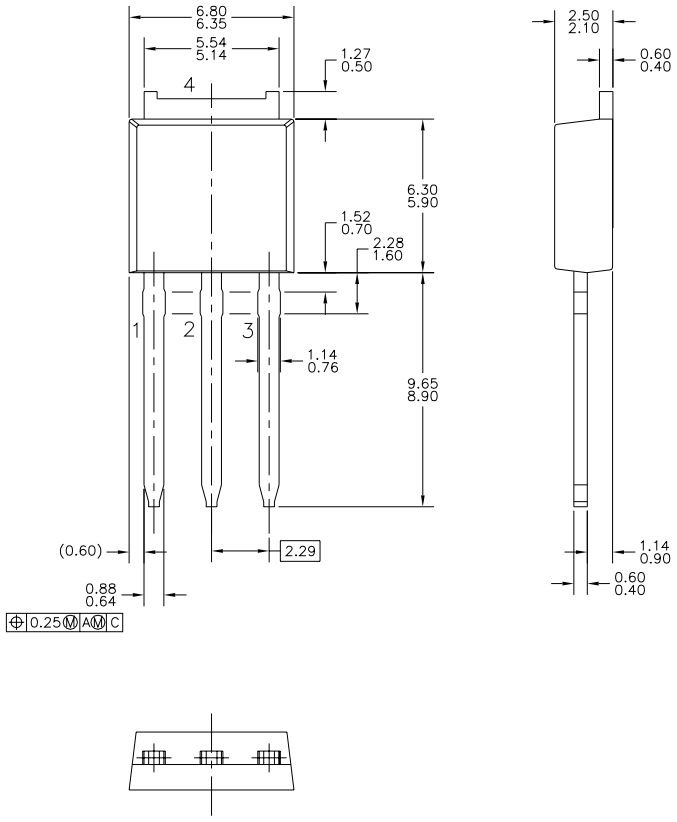
	OPTION AA	OPTION AB
L3	0.89−1.27	1.52−2.03
D	5.97−6.22	5.33−5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

Mechanical Dimensions (Continued)

I-PAK



Dimensions in Millimeters

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidianries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter® *
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world 1mW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SuperMOS™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34