



August 2009

# FSA2567 — Low-Power, Dual SIM Card Analog Switch

### **Features**

- Low On Capacitance for Data Path: 10pF Typical
- Low On Resistance for Data Path: 6Ω Typical
- Low On Resistance for Supply Path: 0.4Ω Typical
- Wide V<sub>CC</sub> Operating Range: 1.65V to 4.3V
- Low Power Consumption: 1µA Maximum
  - 15 $\mu$ A Maximum I<sub>CCT</sub> Over Expanded Voltage Range (V<sub>IN</sub>=1.8V, V<sub>CC</sub>=4.3V)
- Wide -3db Bandwidth: > 160MHz
- Packaged in:
  - Pb-free 16-Lead MLP & 16-Lead UMLP
- 3kV ESD Rating, >12kV Power/GND ESD Rating

# **Applications**

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

### **Description**

The FSA2567 is a bi-directional, low-power, dual double-pole, double-throw (4PDT) analog switch targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

The FSA2567 is compatible with the requirements of SIM cards and features a low on capacitance ( $C_{ON}$ ) of 10pF to ensure high-speed data transfer. The  $V_{SIM}$  switch path has a low  $R_{ON}$  characteristic to ensure minimal voltage drop in the dual SIM card supply paths.

The FSA2567 contains special circuitry that minimizes current consumption when the control voltage applied to the SEL pin is lower than the supply voltage ( $V_{\text{CC}}$ ). This feature is especially valuable in ultra-portable applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

### **IMPORTANT NOTE:**

For additional information, please contact <a href="mailto:analogswitch@fairchildsemi.com">analogswitch@fairchildsemi.com</a>.

# **Ordering Information**

Part Number	Top Mark	Operating Temperature Range	Eco Status	Package
FSA2567MPX	FSA2567	-40 to +85°C	Green	16-Lead, Molded Leadless Package (MLP) Quad, JEDEC MO-220, 3mm Square
FSA2567UMX	GX	-40 to +85°C	Green	16-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6mm

For Fairchild's definition of Eco Status, please visit: <a href="http://www.fairchildsemi.com/company/green/rohs\_green.html">http://www.fairchildsemi.com/company/green/rohs\_green.html</a>.

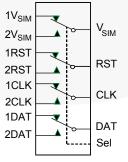


Figure 1. Analog Symbol

# **Pin Assignments**

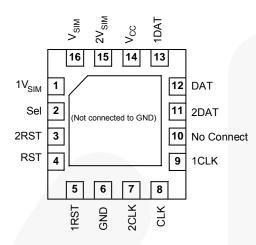


Figure 2. Pad Assignment MLP16 (Top Through View)

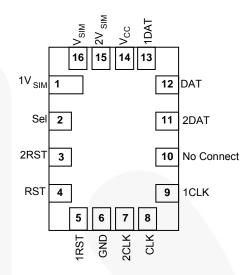


Figure 3. Pad Assignment UMLP16 (Top Through View)

# **Pin Definitions**

Pin	Description
nDAT, nRST, nCLK	Multiplexed Data Source Inputs
nV <sub>SIM</sub>	Multiplexed SIM Supply Inputs
V <sub>SIM</sub> , DAT, RST, CLK	Common SIM Ports
Sel	Switch Select

# **Truth Table**

Sel	Function
Logic LOW	1DAT = DAT, 1RST = RST, 1CLK = CLK, 1V <sub>SIM</sub> = V <sub>SIM</sub>
Logic HIGH	2DAT = DAT, 2RST = RST, 2CLK = CLK, 2V <sub>SIM</sub> = V <sub>SIM</sub>

# **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage		-0.5	+5.5	V
V <sub>CNTRL</sub>	DC Input Voltage (Sel) <sup>(1)</sup>		-0.5	Vcc	V
V <sub>SW</sub>	DC Switch I/O Voltage <sup>(1)</sup>		-0.5	V <sub>CC</sub> + 0.3	V
I <sub>IK</sub>	DC Input Diode Current		-50		mA
I <sub>SIM</sub>	DC Output Current - V <sub>SIM</sub>			350	mA
I <sub>OUT</sub>	DC Output Current – DAT, CLK, RST			35	mA
T <sub>STG</sub>	Storage Temperature		-65	+150	°C
	Human Body Model, JEDEC: JESD22-A114	All Pins		3	
ESD	Tiulian Bouy Wouel, JEDEC. JESD22-ATT4	I/O to GND		12	kV
	Charged Device Model, JEDEC: JESD22-C101			2	la .

#### Note:

 The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

# **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage	1.65	4.30	V
V <sub>CNTRL</sub>	Control Input Voltage (Sel) <sup>(2)</sup>	0	V <sub>CC</sub>	V
$V_{SW}$	Switch I/O Voltage	-0.5	Vcc	V
I <sub>SIM</sub>	DC Output Current - V <sub>SIM</sub>		150	mA
I <sub>OUT</sub>	DC Output Current – DAT, CLK, RST	A	25	mA
T <sub>A</sub> Operating Temperature		-40	+85	°C

#### Note:

2. The control input must be held HIGH or LOW; it must not float.

# **DC Electrical Characteristics**

All typical values are at 25°C, 3.3V V<sub>CC</sub> unless otherwise specified.

Cumbal	Danamatan	O am distinue	V 00	T <sub>A</sub> =- 40°C to +85°C			I I mit a
Symbol	mbol Parameter Conditions	V <sub>CC</sub> (V)	Min.	Тур.	Max.	Units	
VıK	Clamp Diode Voltage	I <sub>IN</sub> = -18mA	2.7			-1.2	V
			1.65 to 2.3	1.1			
$V_{IH}$	Input Voltage High		2.7 to 3.6	1.3			V
			4.3	1.7			
			1.65 to 2.3			0.4	
$V_{IL}$	Input Voltage Low		2.7 to 3.6			0.5	V
			4.3			0.7	
I <sub>IN</sub>	Control Input Leakage	V <sub>SW</sub> = 0 to V <sub>CC</sub>	4.3	-1		1	μΑ
I <sub>nc(off),</sub> I <sub>no(off),</sub>	Off State Leakage	nRST, nDAT, nCLK, nV <sub>SIM</sub> = 0.3V or 3.6V Figure 10	4.3	-60		60	nA
В	Data Path Switch On	$V_{SW} = 0$ , 1.8V, $I_{ON} = -20$ mA Figure 9	1.8		7.0	12.0	Ω
KOND	Resistance <sup>(3)</sup>	V <sub>SW</sub> = 0, 2.3V, I <sub>ON</sub> = -20mA Figure 9	2.7		6.0	10.0	52
Б	V <sub>SIM</sub> Switch	V <sub>SW</sub> = 0, 1.8V, I <sub>ON</sub> = -100mA Figure 9	1.8		0.5	0.7	
R <sub>ONV</sub>	On Resistance <sup>(3)</sup>	V <sub>SW</sub> = 0, 2.3V, I <sub>ON</sub> = -100mA Figure 9	2.7		0.4	0.6	Ω
$\Delta R_{\text{OND}}$	Data Path Delta On Resistance <sup>(4)</sup>	V <sub>SW</sub> = 0V, I <sub>ON</sub> = -20mA	2.7		0.2		Ω
Icc	Quiescent Supply Current	V <sub>CNTRL</sub> = 0 or V <sub>CC</sub> , I <sub>OUT</sub> = 0	4.3			1.0	μA
	Increase in I <sub>CC</sub>	V <sub>CNTRL</sub> = 2.6V, V <sub>CC</sub> = 4.3V	4.3		5.0	10.0	μA
I <sub>CCT</sub>	Current Per Control Voltage and V <sub>CC</sub>	V <sub>CNTRL</sub> = 1.8V, V <sub>CC</sub> = 4.3V	4.3		7.0	15.0	μA

### Notes:

- Measured by the voltage drop between nDAT, nRST, nCLK and relative common port pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the relative ports. Guaranteed by characterization.

# **AC Electrical Characteristics**

All typical value are for  $V_{\text{CC}}$ =3.3V at 25°C unless otherwise specified.

Symbol	ymbol Parameter Conditions	O an diti an a	V 00	T <sub>A</sub> =- 40°C to +85°C			Units
Symbol		V <sub>CC</sub> (V)	Min.	Тур.	Max.	Units	
t <sub>OND</sub>	Turn-On Time Sel to Output	$R_L = 50\Omega$ , $C_L = 35pF$ $V_{SW} = 1.5V$	1.8 <sup>(5)</sup>		65	95	ns
TOND	(DAT,CLK,RST)	Figure 11, Figure 12	2.7 to 3.6		42	60	ns
t <sub>OFFD</sub>	Turn-Off Time Sel to Output	$R_L = 50\Omega$ , $C_L = 35pF$ $V_{SW} = 1.5V$	1.8 <sup>(5)</sup>		30	50	ns
TOTTE	(DAT,CLK,RST)	Figure 11, Figure 12	2.7 to 3.6		20	40	ns
t <sub>ONV</sub>	Turn-On Time	$R_L = 50\Omega, C_L = 35pF$ $V_{SW} = 1.5V$	1.8 <sup>(5)</sup>		55	80	ns
UNV	Sel to Output (V <sub>SIM</sub> )	Figure 11, Figure 12	2.7 to 3.6		35	55	ns
t <sub>OFFV</sub>	Turn-Off Time	$R_L = 50\Omega$ , $C_L = 35pF$ $V_{SW} = 1.5V$ Figure 11, Figure 12	1.8 <sup>(5)</sup>		35	50	
OFFV	Sel to Output (V <sub>SIM</sub> )		2.7 to 3.6		22	40	ns
t <sub>PD</sub>	Propagation Delay <sup>(5)</sup> (DAT,CLK,RST)	$C_L$ = 35 pF, $R_L$ = 50 $\Omega$ Figure 11, Figure 13	3.3		0.25		ns
t <sub>BBMD</sub>	Break-Before-Make <sup>(5)</sup> (DAT,CLK,RST)	$R_L = 50\Omega$ , $C_L = 35pF$ $V_{SW1} = V_{SW2} = 1.5V$ Figure 15	2.7 to 3.6	3	18		ns
t <sub>BBMV</sub>	Break-Before-Make <sup>(5)</sup> (V <sub>SIM</sub> )	$R_L = 50\Omega$ , $C_L = 35pF$ $V_{SW1} = V_{SW2} = 1.5V$ Figure 15	2.7 to 3.6	3	12		ns
Q	Charge Injection (DAT,CLK,RST)	$C_L = 50 pF$ , $R_{GEN} = 0\Omega$ , $V_{GEN} = 0V$	2.7 to 3.6		10		рС
O <sub>IRR</sub>	Off Isolation (DAT,CLK,RST)	$R_L = 50\Omega$ , $f = 10MHz$ Figure 17	2.7 to 3.6		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk (DAT,CLK,RST)	$R_L = 50\Omega$ , $f = 10MHz$ Figure 18	2.7 to 3.6		-60	, i	dB
BW	-3db Bandwidth (DAT,CLK,RST)	$R_L = 50\Omega$ , $C_L = 5pF$ Figure 16	2.7 to 3.6		475		MHz

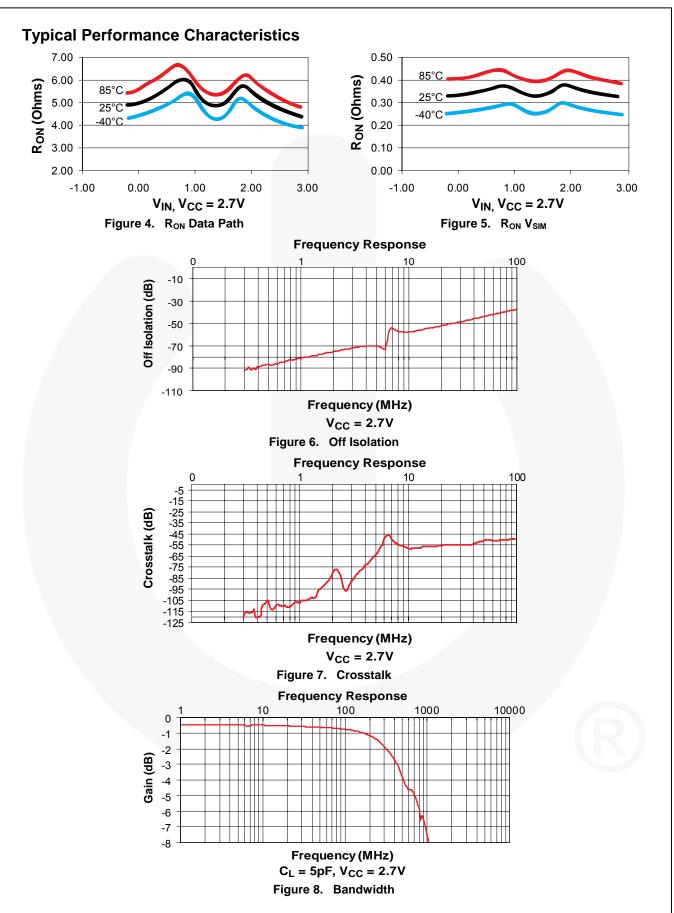
### Note:

5. Guaranteed by characterization.

# Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> =- 40°C to +85°C			Units
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Ullits
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 0V		1.5		
C <sub>OND</sub>	RST, CLK, DAT On Capacitance <sup>(6)</sup>	V <sub>CC</sub> = 3.3V, f = 1MHz Figure 20		10	12	
C <sub>ONV</sub>	V <sub>SIM</sub> On Capacitance <sup>(6)</sup>	V <sub>CC</sub> = 3.3V, f = 1MHz Figure 20		110	150	pF
C <sub>OFFD</sub>	RST, CLK, DAT Off Capacitance	V <sub>CC</sub> = 3.3V Figure 19		3		
C <sub>OFFV</sub>	V <sub>SIM</sub> Off Capacitance	V <sub>CC</sub> = 3.3V Figure 19		40		

Note:
6. Guaranteed by characterization.



# **Test Diagrams**

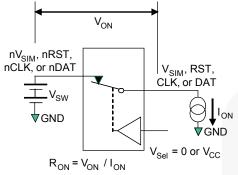
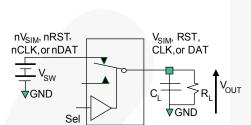


Figure 9. On Resistance



 $\rm R_L$  and  $\rm C_L$  are functions of the application environment (see tables for specific values).  $\rm C_l$  includes test fixture and stray capacitance.

Figure 11. AC Test Circuit Load

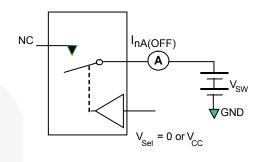


Figure 10. Off Leakage

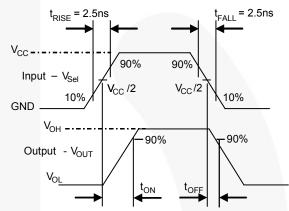


Figure 12. Turn-On / Turn-Off Waveforms

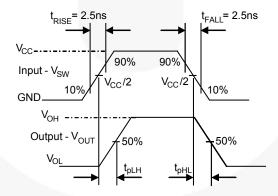


Figure 13. Propagation Delay

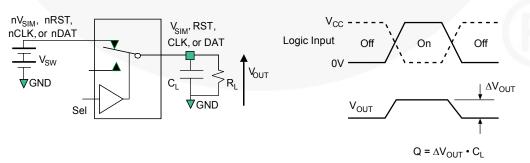
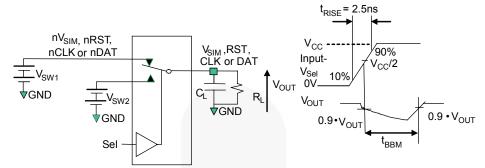


Figure 14. Charge Injection

### Test Diagrams (Continued)



 $R_L$  and  $C_L$  are functions of the application environment (see tables for specific values).  $C_L$  includes test fixture and stray capacitance.

Figure 15. Break-Before-Make Interval Timing

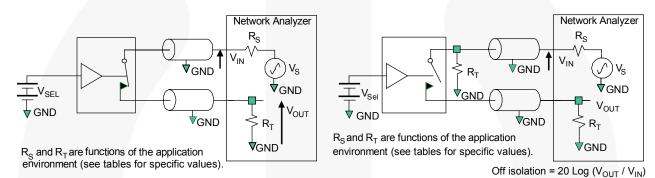


Figure 16. Bandwidth

Figure 17. Channel Off Isolation

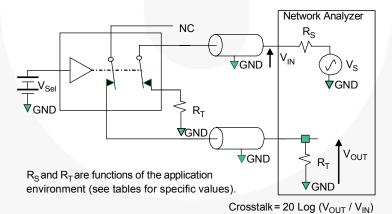


Figure 18. Non-Adjacent Channel-to-Channel Crosstalk

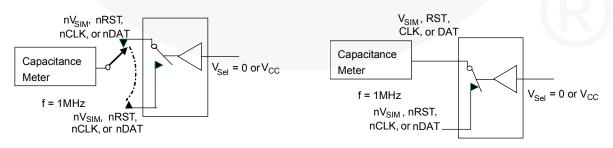
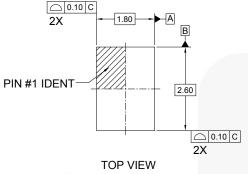
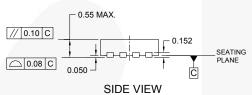


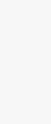
Figure 19. Channel Off Capacitance

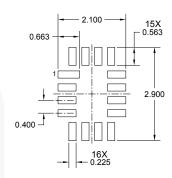
Figure 20. Channel On Capacitance

# **Physical Dimensions**



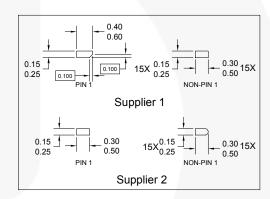


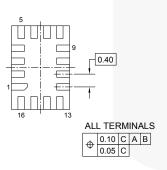




RECOMMENDED LAND PATTERN

#### TERMINAL SHAPE VARIANTS





**BOTTOM VIEW** 

### NOTES:

- A. THIS PACKAGE IS NOT CURRENTLY REGISTERED WITH ANY STANDARDS COMMITTEE
- **B. DIMENSIONS ARE IN MILLIMETERS**
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
  D. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS
- E. LAND PATTERN IS A MINIMAL TOE DESIGN
- F. DRAWING FILE NAME: UMLP16AREV3

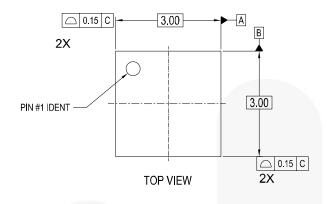
### Figure 21. 16-Lead Ultrathin Molded Leadless Package (UMLP)

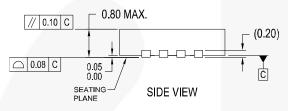
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

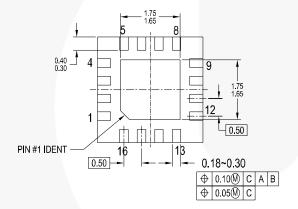
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area: http://www.fairchildsemi.com/packaging/3x3MLP16 Pack TNR.pdf.

# **Physical Dimensions**







**BOTTOM VIEW** 

### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WEED-Pending, DATED pending
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

### MLP16BrevB

Figure 22. 16-Terminal Molded Leadless Package (MLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: <a href="http://www.fairchildsemi.com/packaging/">http://www.fairchildsemi.com/packaging/</a>.

RECOMMENDED LAND PATTERN





#### TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
Auto-SPM™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™

CTL™
Current Transfer Logic™
EcoSPARK®
EfficientMax™
EZSWITCH™

Fairchild<sup>®</sup>
Fairchild Semiconductor<sup>®</sup>
FACT Quiet Series™
FACT<sup>®</sup>
FAST<sup>®</sup>

FastyCore™
FETBench™
FlashWriter®\*

FPSTM F-PFSTM FRFET® Global Power Resource<sup>SM</sup>

GTO™.

Green FPS™ Green FPS™ e-Series™ Gmax™

IntelliMAXTM
ISOPLANARTM
MegaBuckTM
MICROCOUPLERTM
MicroFETTM
MicroPakTM
MillerDriveTM
MotionMaxTM
Motion-SPMTM
OPTOLOGIC®

PDP SPM™ Power-SPM™

OPTOPLANAR®

PowerTrench® PowerXS™

Programmable Active Droop™

OFET®

OS™

Quiet Series™

RapidConfigure™

O™

Saving our world, 1mWWW/kW at a time™ SignalWise™

SmartMaxTM
SMART STARTTM
SPM®
STEALTHTM
SuperSOTTM-3
SuperSOTTM-8
SuperSOTTM-8
SuperSOTTM-8
SuperSOTTM-8
SyncFETTM
SyncFeTTM
SyncLockTM
SyncLockTM
EggmerAL

The Power Franchise

the Franchise

TinyBuck™
TinyCalc™
TinyLogic®
TiNYOPTO™
TinyPower™
TinyPWT™
TinyPWT™
TinyPWIT™
TinyWire™
TiriAult Detect™

TRUECURRENT"

LSerDesTM
SerDes
UHC®
Ultra FRFETTM
UniFETTM
VCXTM
VisualMaxTM
XSTM

#### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

### As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

### PRODUCT STATUS DEFINITIONS

#### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 142

<sup>\*</sup> Trademarks of System General Corporation, used under license by Fairchild Semiconductor.