



ON Semiconductor®

April 2018

FSL156MRIN Green-Mode Power Switch (FPS™)

Features

- Advanced Soft Burst Mode for Low Standby Power and Low Audible Noise
- Random Frequency Fluctuation (RFF) for Low EMI
- Pulse-by-Pulse Current Limit
- Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output-Short Protection (OSP), and Under-Voltage Lockout (UVLO) with Hysteresis, Line Over Voltage Protection (LOVP)
- Low Operating Current (0.4mA) in Burst Mode
- Internal Startup Circuit
- Internal High-Voltage SenseFET: 650V
- Built-in Soft-Start: 15ms
- Auto-Restart Mode

Description

The FSL156MRIN is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switched Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Line-Over Voltage Protection (LOVP), Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSL156MRIN reduces total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost-effective design of a flyback converter.

Applications

- Power Supply for Home Appliances, LCD Monitors, STBs, and DVD Players

Ordering Information

Part Number	Package ⁽¹⁾	Operating Junction Temperature	Current Limit (Typ.)	R _{DS(ON)} (Max.)	Output Power Table ⁽²⁾			
					230V _{AC} ±15%		85-265V _{AC}	
					Adapter ⁽³⁾	Open Frame ⁽⁴⁾	Adapter ⁽³⁾	Open Frame ⁽⁴⁾
FSL156MRIN	8-DIP	-40°C ~ +125°C	1.6A	2.2Ω	26W	40W	20W	30W

Notes:

1. Lead-free package per JEDEC J-STD-020B.
2. The junction temperature can limit the maximum output power.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.

Application Circuit

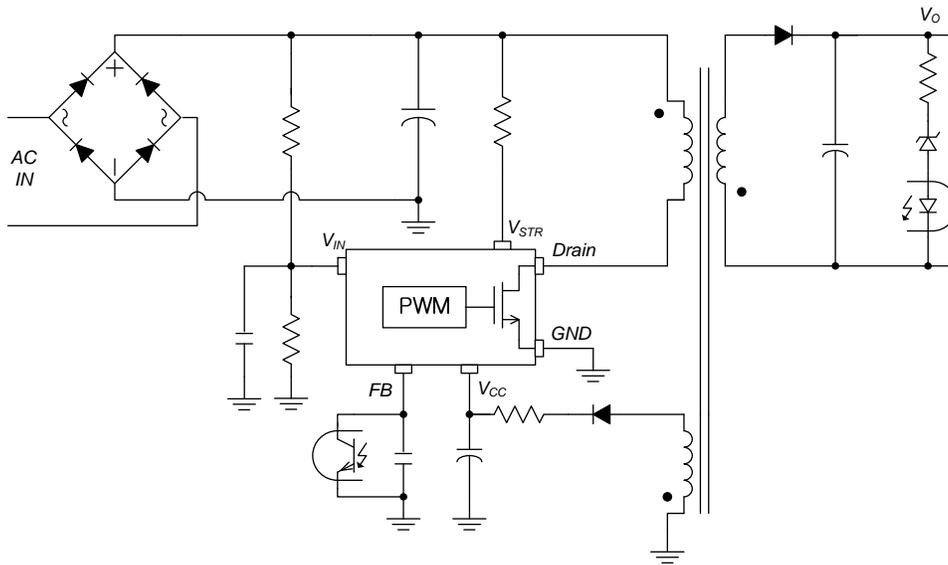


Figure 1. Typical Application Circuit

Internal Block Diagram

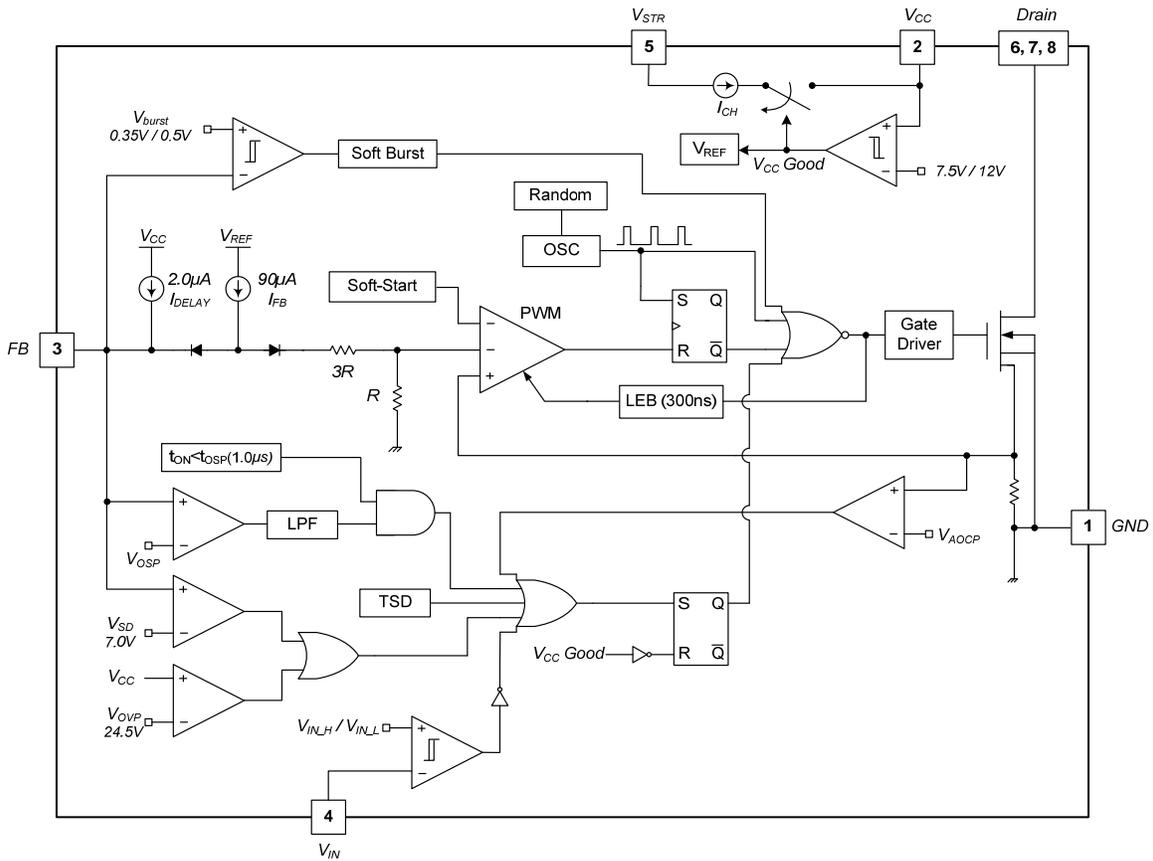


Figure 2. Internal Block Diagram

Pin Configuration

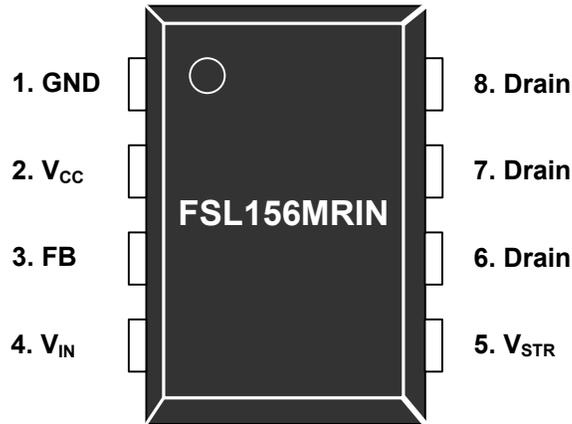


Figure 3. Pin Assignments (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	Ground. This pin is the control ground and the SenseFET source.
2	V_{CC}	Power Supply. This pin is the positive supply input, which provides the internal operating current for both startup and steady-state operation.
3	FB	Feedback. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7V, the overload protection triggers, which shuts down the FPS.
4	V_{IN}	Line Over-Voltage Input. This pin is the input pin of line voltage. The voltage, which is divided by resistors, is the input of this pin. If this pin voltage is higher than V_{INH} voltage, the LOVP triggers, which shuts down the FPS. Do not leave this pin floating. If LOVP is not used, this pin should be directly connected to the GND.
5	V_{STR}	Startup. This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source (I_{CH}) is disabled.
6	Drain	SenseFET Drain. High-voltage power SenseFET drain connection.
7		
8		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{STR}	V _{STR} Pin Voltage		650	V
V _{DS}	Drain Pin Voltage		650	V
V _{CC}	V _{CC} Pin Voltage		26	V
V _{FB}	Feedback Pin Voltage	-0.3	10.0	V
V _{IN}	V _{IN} Pin Voltage	-0.3	10.0	V
I _{DM}	Drain Current Pulsed		4	A
I _{DS}	Continuous Switching Drain Current ⁽⁵⁾	T _C =25°C	1.90	A
		T _C =100°C	1.27	
E _{AS}	Single-Pulsed Avalanche Energy ⁽⁶⁾		190	mJ
P _D	Total Power Dissipation (T _C =25°C) ⁽⁷⁾		1.5	W
T _J	Maximum Junction Temperature		150	°C
	Operating Junction Temperature ⁽⁸⁾	-40	+125	°C
T _{STG}	Storage Temperature	-55	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	4.5	kV
		Charged Device Model, JESD22-C101	2.0	

Notes:

- Repetitive peak switching current when the inductive load is assumed: limited by maximum duty (D_{MAX}=0.73) and junction temperature (see Figure 4).
- L=45mH, starting T_J=25°C.
- Infinite cooling condition (refer to the SEMI G30-88).
- Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

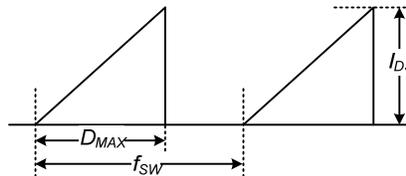


Figure 4. Repetitive Peak Switching Current

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ _{JA}	Junction-to-Ambient Thermal Impedance ⁽⁹⁾	85	°C/W
ψ _{JL}	Junction-to-Lead Thermal Impedance ⁽¹⁰⁾	11	°C/W

Notes:

- JEDEC recommended environment, JESD51-2, and test board, JESD51-10, with minimum land pattern.
- Measured on drain pin #7, close to the plastic interface.

Electrical Characteristics

T_J = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
SenseFET Section							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{CC} =0V, I _D =250μA	650			V	
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} =520V, T _A =125°C			250	μA	
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =1A		1.8	2.2	Ω	
C _{ISS}	Input Capacitance ⁽¹¹⁾	V _{DS} =25V, V _{GS} =0V, f=1MHz		515		pF	
C _{OSS}	Output Capacitance ⁽¹¹⁾	V _{DS} =25V, V _{GS} =0V, f=1MHz		75		pF	
t _r	Rise Time	V _{DS} =325V, I _D =4A, R _G =25Ω		26		ns	
t _f	Fall Time	V _{DS} =325V, I _D =4A, R _G =25Ω		25		ns	
t _{d(on)}	Turn-On Delay	V _{DS} =325V, I _D =4A, R _G =25Ω		14		ns	
t _{d(off)}	Turn-Off Delay	V _{DS} =325V, I _D =4A, R _G =25Ω		32		ns	
Control Section							
f _S	Switching Frequency ⁽¹¹⁾	V _{CC} =14V, V _{FB} =4V	61	67	73	kHz	
Δf _S	Switching Frequency Variation ⁽¹¹⁾	-25°C < T _J < 125°C		±5	±10	%	
D _{MAX}	Maximum Duty Ratio	V _{CC} =14V, V _{FB} =4V	61	67	73	%	
D _{MIN}	Minimum Duty Ratio	V _{CC} =14V, V _{FB} =0V			0	%	
I _{FB}	Feedback Source Current	V _{FB} =0	65	90	115	μA	
V _{START}	UVLO Threshold Voltage	V _{FB} =0V, V _{CC} Sweep	11	12	13	V	
V _{STOP}		After Turn-on, V _{FB} =0V	7.0	7.5	8.0	V	
t _{SS}	Internal Soft-Start Time	V _{STR} =40V, V _{CC} Sweep		15		ms	
V _{RECOMM}	Recommended V _{CC} Range		13		23	V	
Burst Mode Section							
V _{BURH}	Burst-Mode Voltage	V _{CC} =14V, V _{FB} Sweep	0.45	0.50	0.55	V	
V _{BURL}			0.30	0.35	0.40	V	
Hys				150		mV	
Protection Section							
I _{LIM}	Peak Drain Current Limit	di/dt=300mA/μs	1.45	1.60	1.75	A	
V _{SD}	Shutdown Feedback Voltage	V _{CC} =14V, V _{FB} Sweep	6.45	7.00	7.55	V	
I _{DELAY}	Shutdown Delay Current	V _{CC} =14V, V _{FB} =4V	1.2	2.0	2.8	μA	
t _{LEB}	Leading-Edge Blanking Time ^(11,12)			300		ns	
V _{OVP}	Over-Voltage Protection	V _{CC} Sweep	23.0	24.5	26.0	V	
V _{INH}	Line Over-Voltage Protection Threshold Voltage	V _{CC} =14V, V _{IN} Sweep	1.87	1.95	2.03	V	
V _{INHYS}	Line Over-Voltage Protection Hysteresis	V _{CC} =14V, V _{IN} Sweep		0.06		V	
t _{OSP}	Output-Short Protection ⁽¹¹⁾	Threshold Time	OSP Triggered when t _{ON} <t _{OSP} & V _{FB} >V _{OSP} (Lasts Longer than t _{OSP_FB})	0.7	1.0	1.3	μs
V _{OSP}		Threshold V _{FB}		1.8	2.0	2.2	V
t _{OSP_FB}		V _{FB} Blanking Time		2.0	2.5	3.0	μs
TSD	Thermal Shutdown Temperature ⁽¹¹⁾	Shutdown Temperature	125	135	145	°C	
T _{HYS}		Hysteresis		60		°C	

Continued on the following page...

Electrical Characteristics (Continued)T_J = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Section						
I _{OP}	Operating Supply Current, (Control Part in Burst Mode)	V _{CC} =14V, V _{FB} =0V	0.3	0.4	0.5	mA
I _{OPS}	Operating Switching Current, (Control Part and SenseFET Part)	V _{CC} =14V, V _{FB} =2V	1.1	1.5	1.9	mA
I _{START}	Start Current	V _{CC} =11V (Before V _{CC} Reaches V _{START})	85	120	155	μA
I _{CH}	Startup Charging Current	V _{CC} =V _{FB} =0V, V _{STR} =40V	0.7	1.0	1.3	mA
V _{STR}	Minimum V _{STR} Supply Voltage	V _{CC} =V _{FB} =0V, V _{STR} Sweep		26		V

Notes:

11. These parameters are guaranteed; not 100% tested in production.
12. t_{LEB} includes gate turn-on time.

Typical Performance Characteristics

Characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

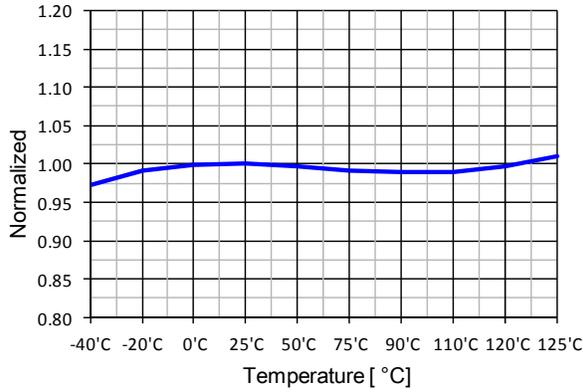


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

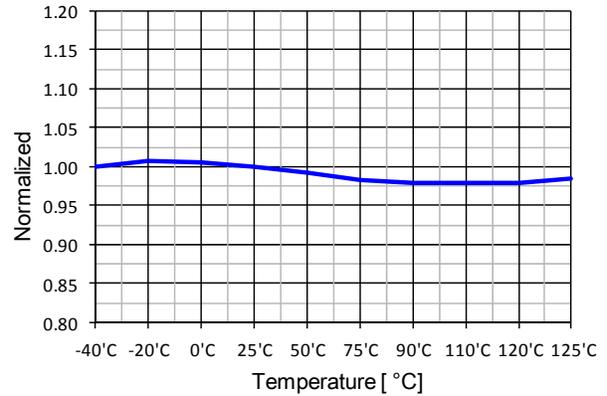


Figure 6. Operating Switching Current (I_{OPS}) vs. T_A

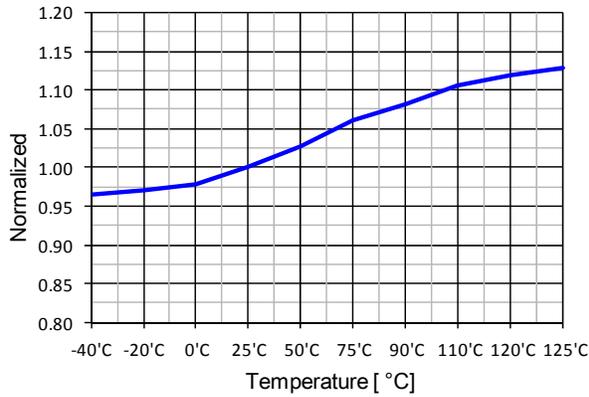


Figure 7. Startup Charging Current (I_{CH}) vs. T_A

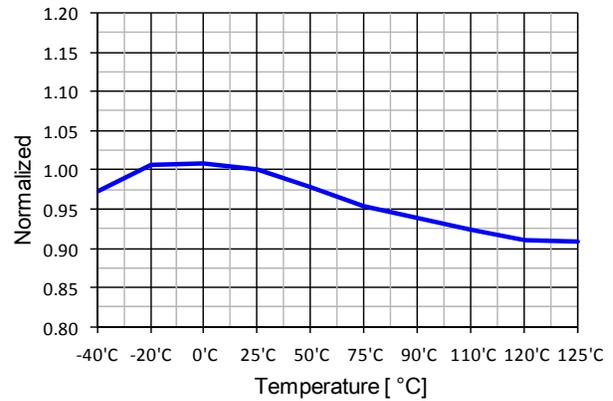


Figure 8. Peak Drain Current Limit (I_{LIM}) vs. T_A

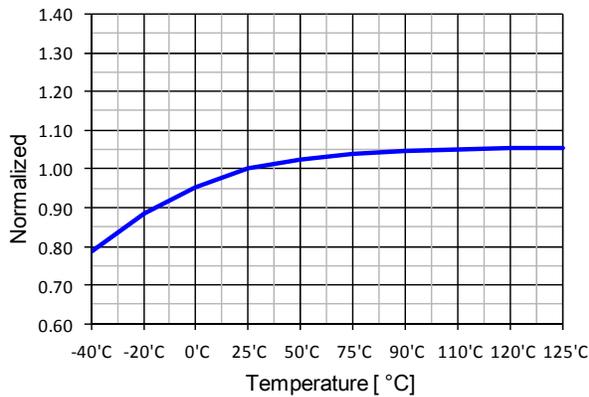


Figure 9. Feedback Source Current (I_{FB}) vs. T_A

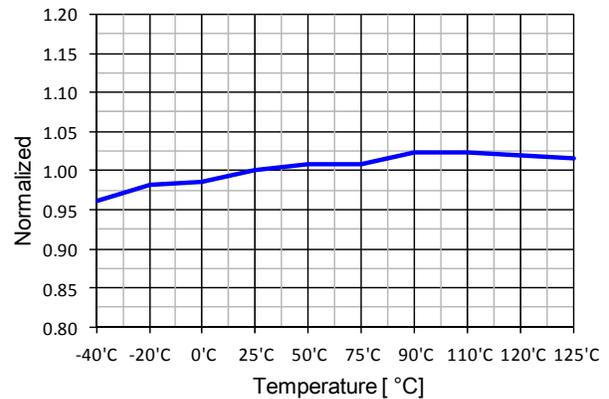


Figure 10. Shutdown Delay Current (I_{DELAY}) vs. T_A

Typical Performance Characteristics

Characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

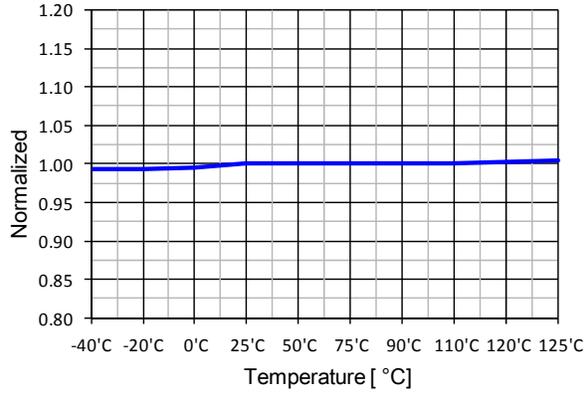


Figure 11. UVLO Threshold Voltage (V_{START}) vs. T_A

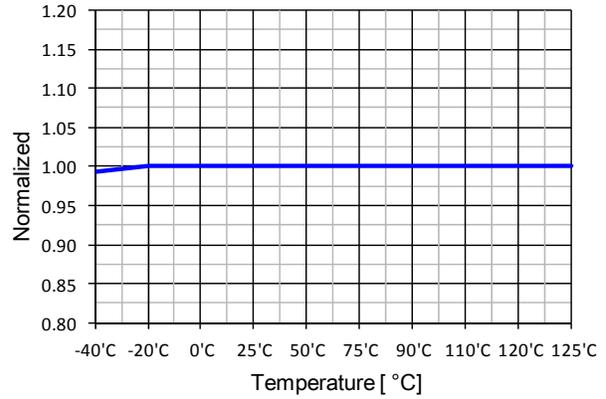


Figure 12. UVLO Threshold Voltage (V_{STOP}) vs. T_A

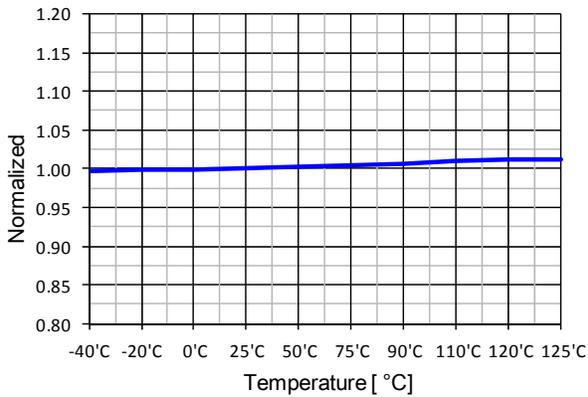


Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

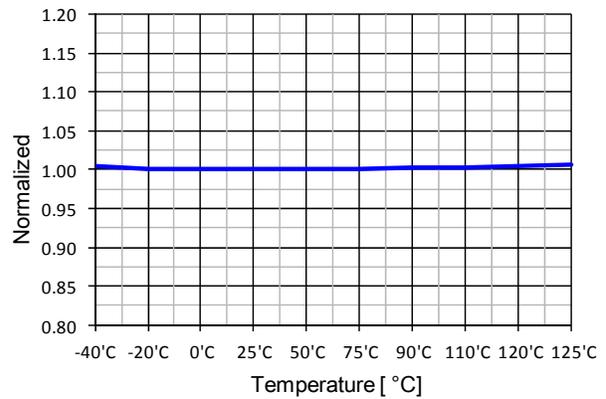


Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

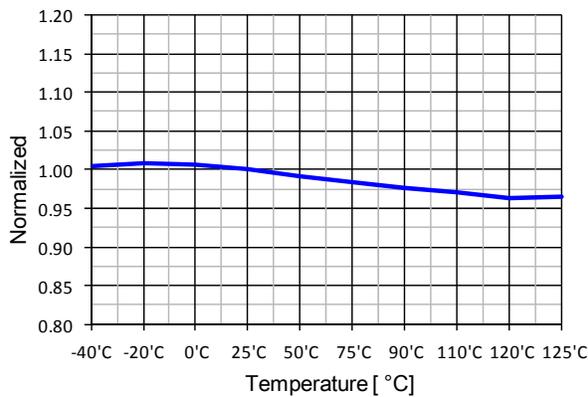


Figure 15. Switching Frequency (f_s) vs. T_A

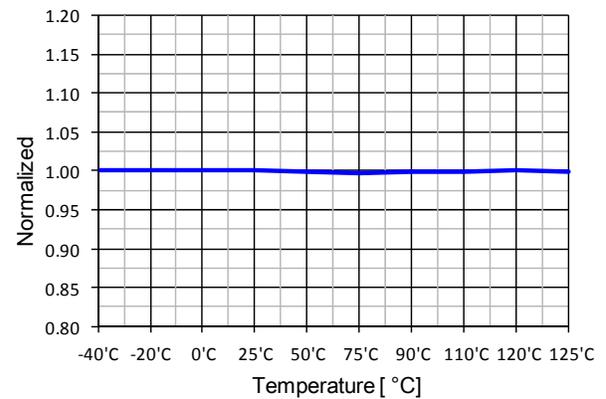


Figure 16. Maximum Duty Ratio (D_{MAX}) vs. T_A

Typical Performance Characteristics

Characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

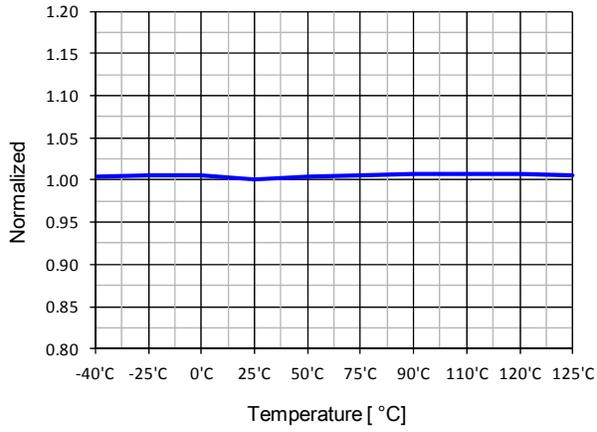


Figure 17. Line OVP (V_{INH}) vs. T_A

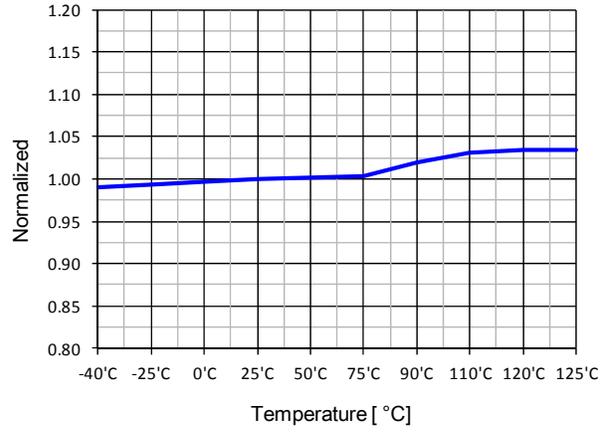


Figure 18. Hysteresis of LOVP (V_{INHYS}) vs. T_A

4. Protection Circuits: The FSL156MRIN has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Output-Short Protection (OSP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0V, normal operation resumes. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, reliability is improved without increasing cost.

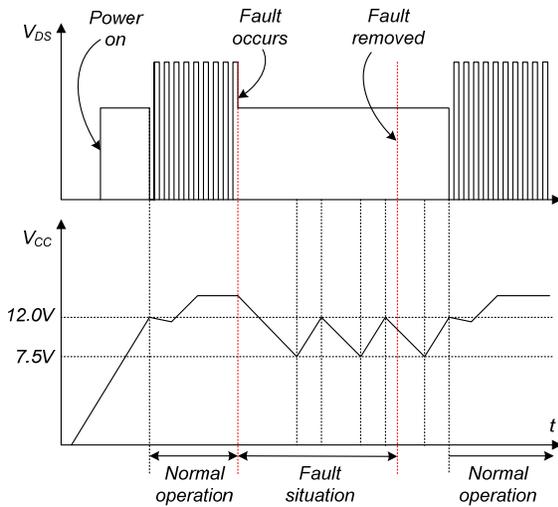


Figure 21. Auto-Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current-limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.5V, D1 is blocked and the 2.0 μ A current source starts to charge C_{FB} slowly up. In this condition, V_{FB} continues

increasing until it reaches 7.0V, when the switching operation is terminated, as shown in Figure 22. The delay for shutdown is the time required to charge C_{FB} from 2.5V to 7.0V with 2.0 μ A. A 25 ~ 50ms delay is typical for most applications. This protection is implemented as auto-restart.

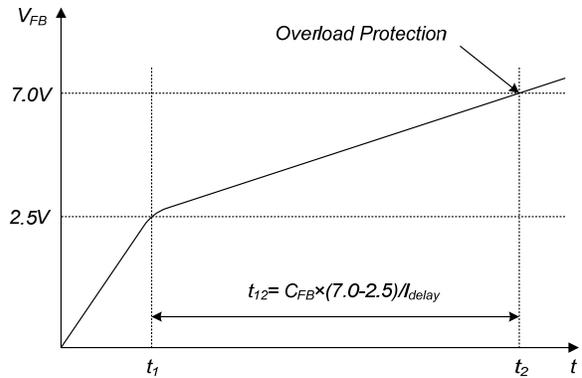


Figure 22. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Even though the FSL156MRIN has overload protection, it is not enough to protect the FSL156MRIN in that abnormal case; due to the severe current stress imposed on the SenseFET until OLP is triggered. The internal AOCP circuit is shown in Figure 23. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing-resistor voltage is greater than the AOCP level, the set signal is applied to the S-R latch, resulting in the shutdown of the SMPS.

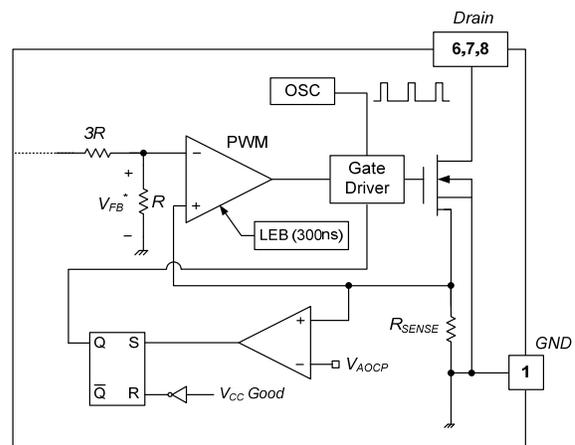


Figure 23. Abnormal Over-Current Protection

4.3. Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Such a steep current creates high-voltage stress on the drain of the SenseFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 2.0V and the SenseFET turn-on time is lower than 1.0 μ s, this condition is recognized as an abnormal error and PWM switching shuts down until V_{CC} reaches V_{START} again. An abnormal condition output short is shown in Figure 24.

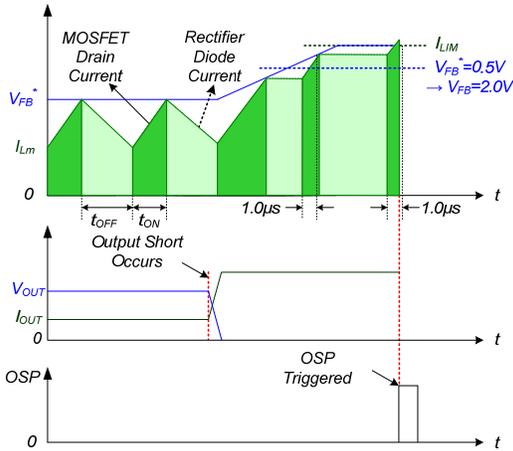


Figure 24. Output-Short Protection

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FSL156MRIN uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5V.

4.5 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package makes it easier for the control IC to detect the temperature of the SenseFET. If the temperature exceeds $\sim 135^{\circ}\text{C}$, the thermal shutdown is triggered and stops operation. The FSL156MRIN operates in Auto-Restart Mode until the temperature decreases to around 75°C , when normal operation resumes.

4.6 Line Over-Voltage Protection (LOVP): If the line input voltage is increased to an unwanted level, high line input voltage creates high-voltage stress on the entire system. To protect from this abnormal condition, LOVP is included. It is comprised of detecting V_{IN} using divided resistors. When V_{IN} is higher than 1.95V, this condition is recognized as an abnormal error and PWM switching shuts down until V_{IN} decreases to around 1.89V (60mV hysteresis).

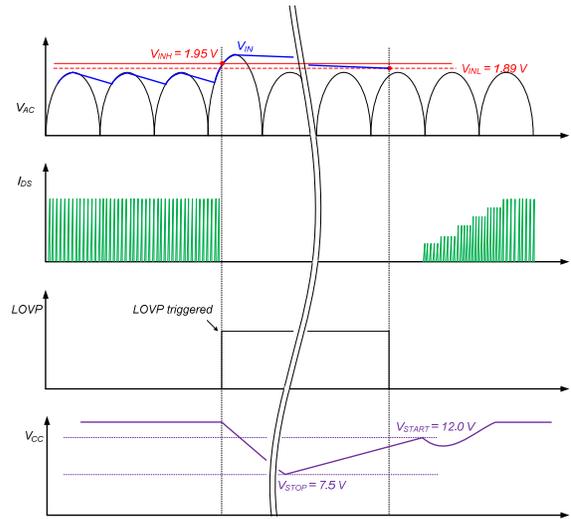


Figure 25. Line Over-Voltage Protection

5. Soft Burst Mode: To minimize power dissipation in Standby Mode, the FSL156MRIN enters Burst-Mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 22, the device automatically enters Burst Mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (500mV), switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables SenseFET switching, reducing switching loss in Standby Mode.

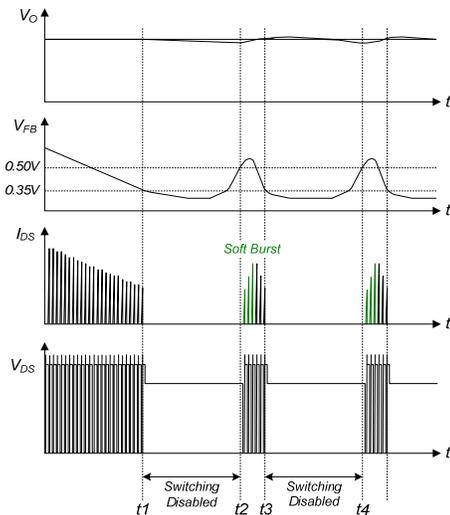


Figure 26. Burst-Mode Operation

6. Random Frequency Fluctuation (RFF): Fluctuating switching frequency of an SMPS can reduce EMI by spreading the energy over a wide frequency range. The amount of EMI reduction is directly related to the switching frequency variation, which is limited internally. The switching frequency is determined randomly by external feedback voltage and an internal free-running oscillator at every switching instant. RFF effectively scatters EMI noise around typical switching frequency (67kHz) and can reduce the cost of the input filter included to meet the EMI requirements (e.g. EN55022).

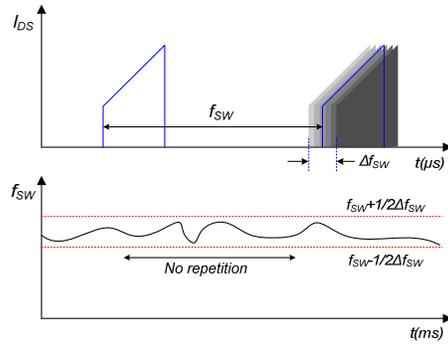
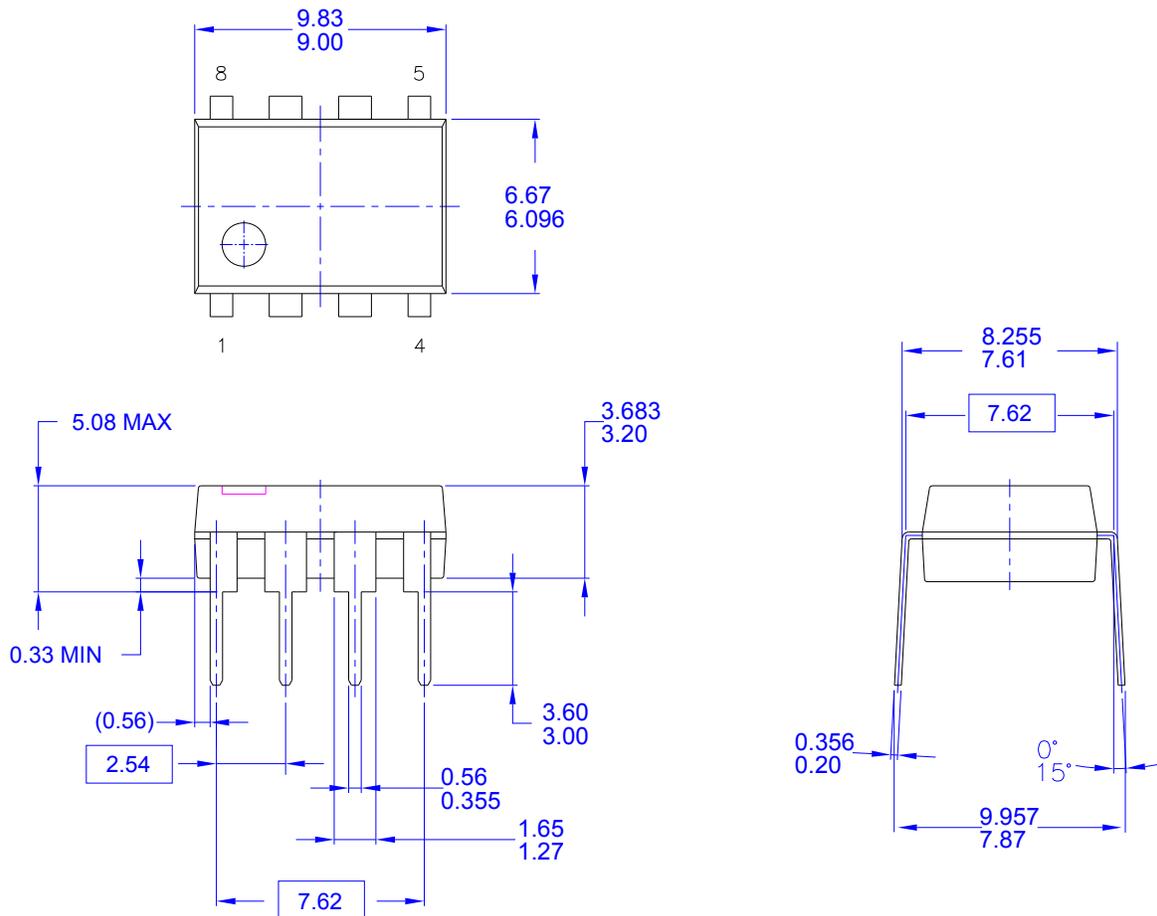


Figure 27. Random Frequency Fluctuation

Package Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994
 - E) DRAWING FILENAME AND REVISION: MKT-N08FREV2.

Figure 28. 8-Lead, MDIP, JEDEC MS-001, .300" Wide

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative