

## FST3384 10-Bit Low Power Bus Switch

### General Description

The Fairchild Switch FST3384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ( $\overline{OE}$ ) signals. When  $\overline{OE}$  is LOW, the switch is ON and Port A is connected to Port B. When  $\overline{OE}$  is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

### Features

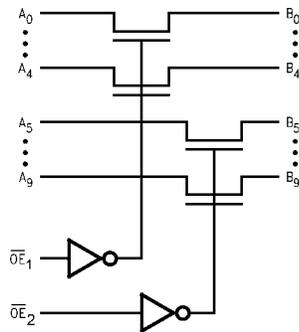
- 4 $\Omega$  switch connection between two ports
- Minimal propagation delay through the switch
- Ultra low power with < 0.1  $\mu$ A typical  $I_{CC}$
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level

### Ordering Code:

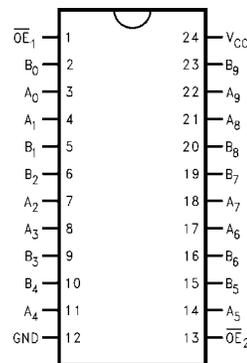
Order Number	Package Number	Package Description
FST3384WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
FST3384QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3384MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Diagram



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enable
A <sub>0</sub> -A <sub>9</sub>	Bus A
B <sub>0</sub> -B <sub>9</sub>	Bus B

### Truth Table

$\overline{OE}_1$	$\overline{OE}_2$	B <sub>0</sub> -B <sub>4</sub>	B <sub>5</sub> -B <sub>9</sub>	Function
L	L	A <sub>0</sub> -A <sub>4</sub>	A <sub>5</sub> -A <sub>9</sub>	Connect
L	H	A <sub>0</sub> -A <sub>4</sub>	HIGH-Z State	Connect
H	L	HIGH-Z State	A <sub>5</sub> -A <sub>9</sub>	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA
DC Output ( $I_{OUT}$ ) Sink Current	128 mA
DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )	+/- 100mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 3)

Power Supply Operating ( $V_{CC}$ )	4.0V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	0V to 5.5V
Input Rise and Fall Time ( $t_r, t_f$ )	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 3:** Unused control inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Units	Condition
			Min	Typ (Note 4)	Max		
$V_{IK}$	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18\text{mA}$
$V_{IH}$	HIGH Level Input Voltage	4.0-5.5	2.0			V	
$V_{IL}$	LOW Level Input Voltage	4.0-5.5			0.8	V	
$I_I$	Input Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq V_{IN} \leq 5.5\text{V}$
$I_{OZ}$	OFF-STATE Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq A, B \leq V_{CC}$
$R_{ON}$	Switch On Resistance (Note 5)	4.5		4	7	$\Omega$	$V_{IN} = 0\text{V}, I_{IN} = 64\text{mA}$
		4.5		4	7	$\Omega$	$V_{IN} = 0\text{V}, I_{IN} = 30\text{mA}$
		4.5		8	15	$\Omega$	$V_{IN} = 2.4\text{V}, I_{IN} = 15\text{mA}$
		4.0		11	20	$\Omega$	$V_{IN} = 2.4\text{V}, I_{IN} = 15\text{mA}$
$I_{CC}$	Quiescent Supply Current	5.5			3	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	5.5			2.5	$\text{mA}$	One input at 3.4V Other inputs at $V_{CC}$ or GND

**Note 4:** All typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

**Note 5:** Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$				Units	Conditions	Figure No.
		$C_L = 50\text{ pF, } R_U = R_D = 500\Omega$						
		$V_{CC} = 4.5 - 5.5\text{V}$		$V_{CC} = 4.0\text{V}$				
Min	Max	Min	Max					
$t_{PHL}, t_{PLH}$	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	$V_I = \text{OPEN}$	Figures 1, 2
$t_{PZH}, t_{PZL}$	Output Enable Time $\overline{OE}_1, \overline{OE}_2$ to $A_n, B_n$	1.0	5.7		6.2	ns	$V_I = 7\text{V}$ for $t_{PZL}$ $V_I = \text{OPEN}$ for $t_{PZH}$	Figures 1, 2
$t_{PHZ}, t_{PLZ}$	Output Disable Time $\overline{OE}_1, \overline{OE}_2$ to $A_n, B_n$	1.5	5.2		5.5	ns	$I_I = 7\text{V}$ for $t_{PLZ}$ $V_I = \text{OPEN}$ for $t_{PHZ}$	Figures 1, 2

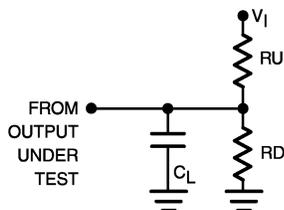
**Note 6:** This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
$C_{IN}$	Control Input Capacitance	3	6	pF	$V_{CC} = 5.0\text{V}$
$C_{I/O} (\text{OFF})$	Input/Output Capacitance	5	13	pF	$V_{CC}, \overline{OE} = 5.0\text{V}$

**Note 7:** Capacitance is characterized but not tested.

## AC Loading and Waveforms



**Note:** Input driven by 50  $\Omega$  source terminated in 50  $\Omega$

**Note:**  $C_L$  includes load and stray capacitance

**Note:** Input PRR = 1.0 MHz,  $t_W = 500\text{ nS}$

FIGURE 1. AC Test Circuit

FST3384  $V_{IN}$  vs.  $R_{ON}$  (Typ)

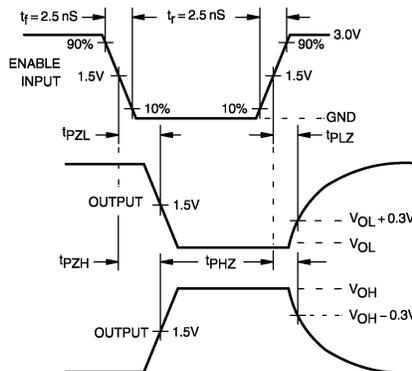
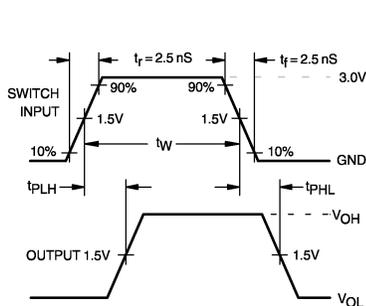
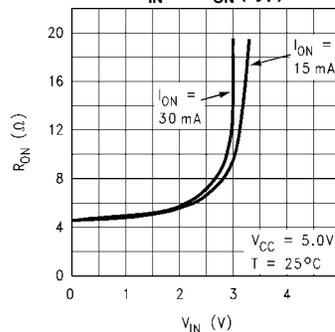


FIGURE 2. AC Waveforms



