ON Semiconductor®

FSUSB63 — 3:1 High-Speed USB 2.0 Switch / Multiplexer

Features

Switch Type	3:1 USB Switch
USB	USB 2.0 High-Speed & Full-Speed Compliant
Break-Before-Make Time	126µs
R_{ON}	6Ω Typical
C_{ON}	6pF Typical
Bandwidth	830MHz
V_{CC}	2.7 to 4.4V
V_{CNTRL}	0 to V_{CC}
Operating Temperature	-40°C to 85°C
I_{CCSLP}	<1µA
I_{CCACT}	7.5µA Typical
Package	12- Lead UMLP 1.80 x 1.80 x 0.55mm, 0.40mm pitch
Top Mark	KG
Ordering Information	FSUSB63UMX

Applications

- Cell Phone, Digital Camera, Notebook
- LCD Monitor, TV, and Set-Top Box
- Netbook, Mobile Internet Device (MID)

Description

The FSUSB63 is a bi-directional, low-power, High-Speed (HS) USB 2.0 3:1 Multiplexer (MUX). It is optimized for switching among three high-speed (480Mbps) sources or any combination of high-speed and full-speed (12Mbps) USB sources, such as an application processor, to one USB 2.0 connector.

The FSUSB63 has a break-before-make time to force re-enumeration by the host when switching between different HS USB 2.0 controllers and thus requires minimal software changes.

The FSUSB63 is compliant with the requirements of USB 2.0 and features extremely low on capacitance (C_{ON}). The wide bandwidth exceeds the requirement to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

Typical Application

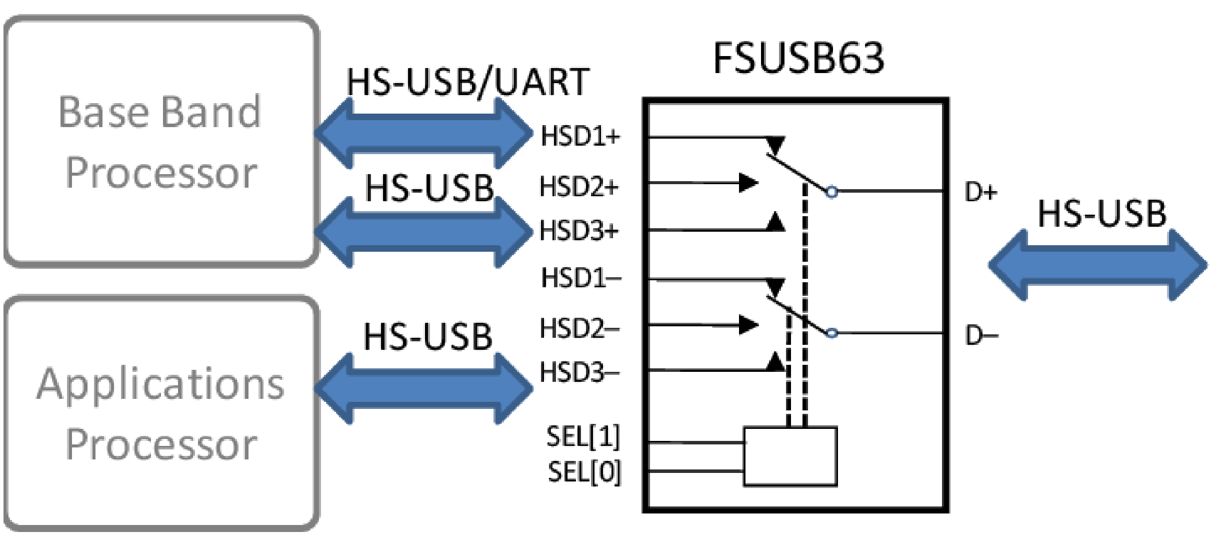


Figure 1. Analog Symbol

Pin Configuration

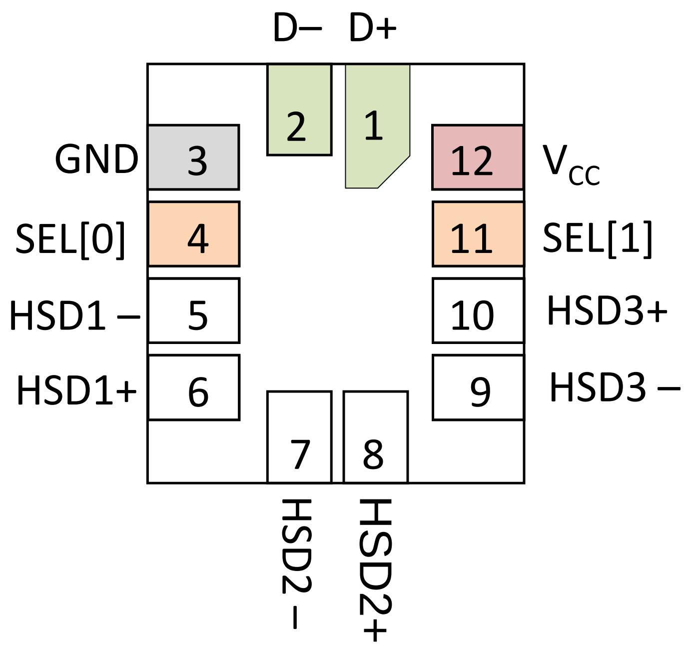


Figure 2. Pin Assignments (Top Through View)

Pin Descriptions

Pin #	Name	Description
1	D+	USB 2.0 High Speed or Full Speed Data Bus D+
2	D-	USB 2.0 High Speed or Full Speed Data Bus D-
3	GND	Ground
4	SEL[0]	Path Selection Control Inputs *(see functional table below)*
5	HSD1-	Multiplexed First Source Path for D-
6	HSD1+	Multiplexed First Source Path for D+
7	HSD2-	Multiplexed Second Source Path for D-
8	HSD2+	Multiplexed Second Source Path for D+
9	HSD3-	Multiplexed Third Source Path for D-
10	HSD3+	Multiplexed Third Source Path for D+
11	SEL[1]	Path Selection Control Inputs *(see functional table below)*
12	V_{CC}	Supply Voltage

Functional Table

Mode	SEL[1]	SEL[0]	Function
Sleep Mode	0	0	D+, D- Switch Paths Open
USB Port 1	0	1	D+=HSD1+, D-=HSD1-
USB Port 2	1	0	D+=HSD2+, D-=HSD2-
USB Port 3	1	1	D+=HSD3+, D-=HSD3-

Eye Compliance

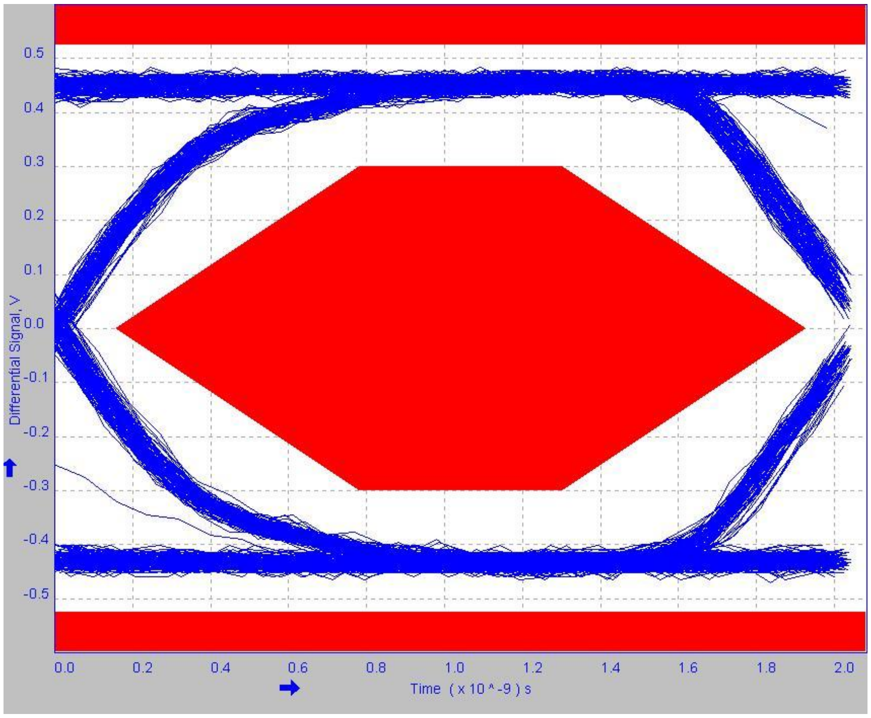


Figure 3. USB 2.0 HS-USB Eye Compliance Pass Through (without Switch)

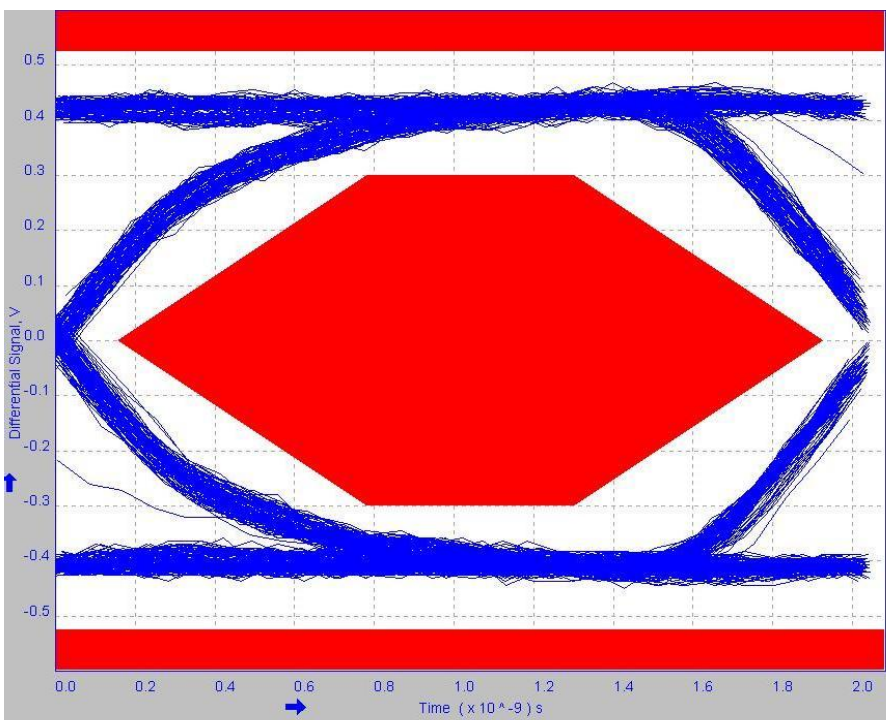


Figure 4. USB 2.0 HS-USB Eye Compliance with Switch

Notes:
1. Figure 3 indicates the HS-USB eye compliance of the source across a characterization board proir to the implementation of the sw tich.
2. Figure 4 show s the total impact the sw ich has on HS-USB eye compliance w hen compared to Figure 3

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.50	5.25	V
V_{CNTRL}	DC Input Voltage (SEL[1:0])[3]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[3]		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Switch Current			50	mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	Level
ESD	IEC61000-4-2 System on USB Connector Pins D+ & D-	Air Gap	15.0		kV
		Contact	8.0		
	Human Body Model, JEDEC: JESD22-A114	Power to GND	16.0		
		I/O to GND	5.0		
		All Pins	5.0		
	Charged Device Model, JEDEC: JESD22-C101		1.5		

Note:

3. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	4.4	V
V_{CNTRL}[4]	Control Input Voltage (SEL[1:0])	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	4.3	V
T_A	Operating Temperature	-40	+85	°C

Note:

4. The control input must be held HIGH or LOW and it must not float.

DC Electrical Characteristics

All typical values are for V_{CC}=3.3V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18mA	2.7			-1.2	V
V_{IH}	Input Voltage High	SEL[1], SEL[0] Inputs	2.7 to 4.3	1.0			V
V_{IL}	Input Voltage Low	SEL[1], SEL[0] Inputs	2.7 to 4.3			0.35	V
I_{IN}	Control Input Leakage	All Combinations of SEL[1] & SEL[0] in the Truth Table (LOW=0V & HIGH=V_{CC})	4.3			1	µA
I_{OZ}	Off-State Leakage	0 ≤ D_n, $HSD1_n$, $HSD2_n$, $HSD3_n$ ≤ 3.6V	4.3	-2		2	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}=0V to 4.3V, V_{CC}=0V, Figure 7	0	-2		2	µA
R_{ON}(5)	HS Switch On Resistance	V_{SW}=0.4V, I_{ON}=-8mA, Figure 6	3.0		6.0	7.8	Ω
ΔR_{ON}	HS Delta R_{ON}(6)	V_{SW}=0.4V, I_{ON}=-8mA	3.0		0.50		Ω
I_{CCSLP}	Sleep Mode Supply Current	SEL[1]=SEL[0]=0	3.6			1	µA
I_{CCACT}	Active Mode Supply Current	V_{CNTRL}=0 or V_{CC}, I_{OUT}=0	2.7		7.5	15.0	µA
			3.6		8.5	16.0	µA
I_{CCT}	Increase in I_{CC} Current per Control Input and V_{CC}	V_{CNTRL}=1.8V	3.6		1.5	4.0	µA
		V_{CNTRL}=1.2V	3.6		3.0	5.0	µA

Notes:

5. Measured by the voltage drop between HSD_n and D_n pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSD_n or D_n ports).
6. Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for V_{CC}=3.3V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time when Switching from One USB Path (or Disabled i.e. SEL=00) to Another USB Path	R_L=50Ω, C_L=35pF V_{SW}=0.8V Figure 8, Figure 9	3.0 to 3.6	126		400	µs
t_{OFF}	Turn-Off Time SEL≠00 (Any of the Three USB Paths Active) to SEL=00 (Disabled)	R_L=50Ω, C_L=35pF V_{SW}= 0.8V Figure 8, Figure 9	3.0 to 3.6			45	ns
t_{PD}	Propagation Delay(7)	C_L=5pF, R_L=50Ω Figure 8, Figure 10	3.3		0.25		ns
t_{BBM}	Break-Before-Make Time	R_L=50Ω, C_L=35pF V_{SW1}=V_{SW2}= 0.8V, Figure 12	3.0 to 3.6	126		400	µs
O_{IRR}	Off Isolation(7)	R_L=50Ω, f=240MHz Figure 14	3.0 to 3.6		-42		dB
Xtalk	Non-Adjacent Channel Crosstalk(7)	R_L=50Ω, f=240MHz Figure 15	3.0 to 3.6		-33		dB
BW	-3db Bandwidth(7)	R_L=50Ω, C_L=0pF Figure 13	3.0 to 3.6		830		MHz
		R_L=50Ω, C_L=5pF Figure 13	3.0 to 3.6		510		MHz

Note:

7. Guaranteed by characterization.

USB High-Speed Related AC Electrical Characteristics

Symbol	Parameter	Conditions	Vcc (V)	TA=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	Pulse Skew [8]	V_{SW}=0.2Vdiff$_{PP}$, Figure 11, C_L=5pF	3.0 to 3.6		10		ps
$t_{SK(I)}$	Skew Between Differential Signals within a Pair[8]	V_{SW}=0.2Vdiff$_{PP}$, Figure 11, C_L=5pF	3.0 to 3.6		10		ps

Capacitance

Symbol	Parameter	Conditions	T_A=- 40ºC to +85ºC			Units
			Min.	Typ.	Max.	
C_{IN}	SEL[1:0] Input Capacitance[8]	V_{CC}=0V		3		pF
C_{ON}	D+/D- On Capacitance[8]	V_{CC}=3.3V, Any of the Three Switch Paths Enabled, f=1MHz, Figure 17		6		
		V_{CC}=3.3V, Any of the Three Switch Paths Enabled, f=240MHz[9]		5		
C_{OFF}	$HSD1_n$, $HSD2_n$, $HSD3_n$ Off Capacitance[8]	V_{CC}=0V or (V_{CC}=3.3V and SEL[1]=SEL[0]=0V) Figure 16		2		

Notes:

8. Guaranteed by characterization.
9. Effective capacitance measured on a network analyzer.

Reference Schematic

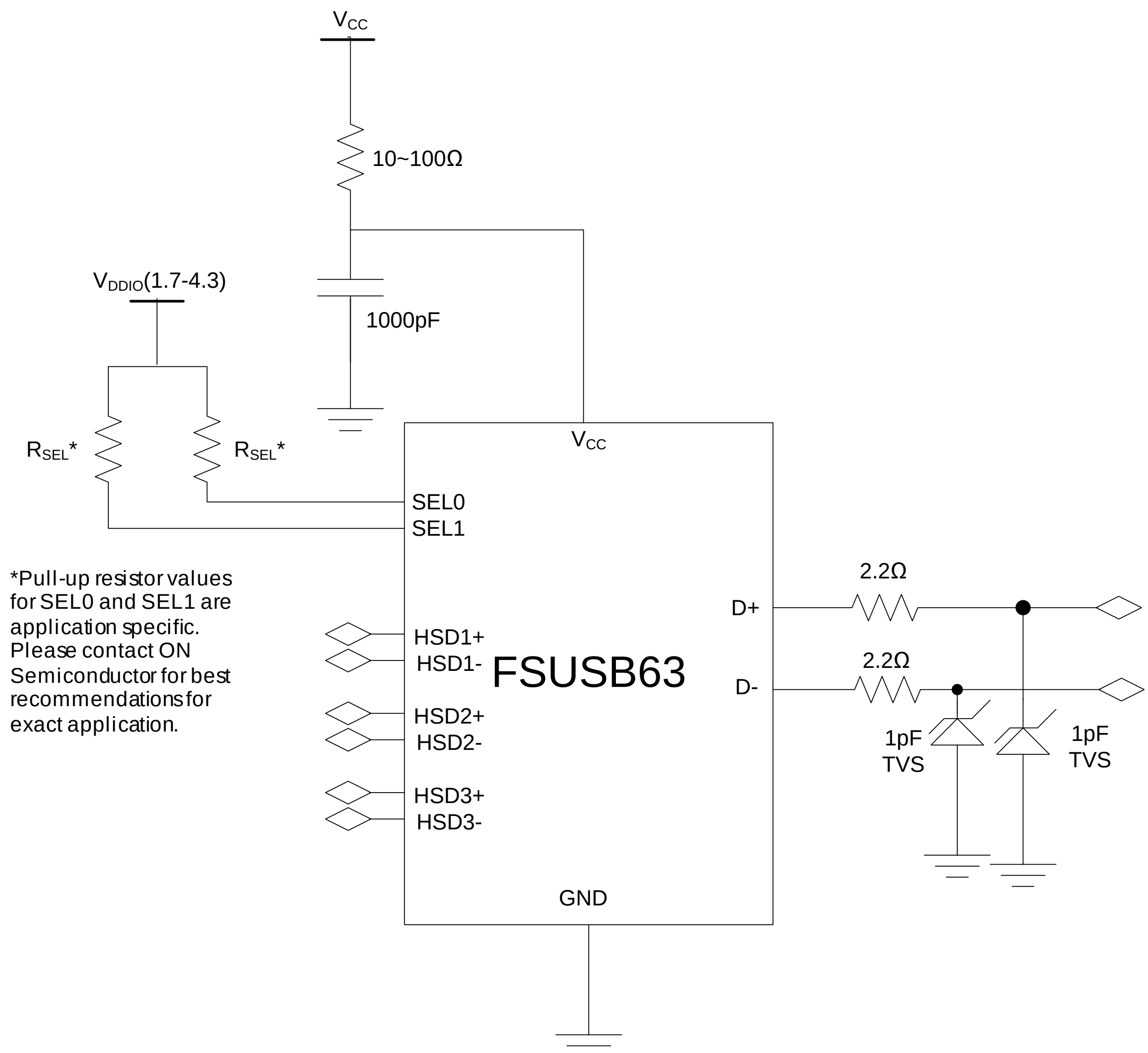


Figure 5. Reference Schematic

Test Diagrams

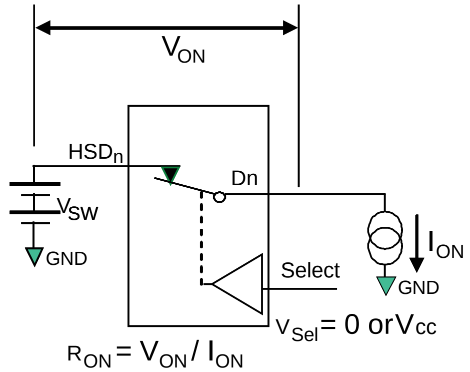
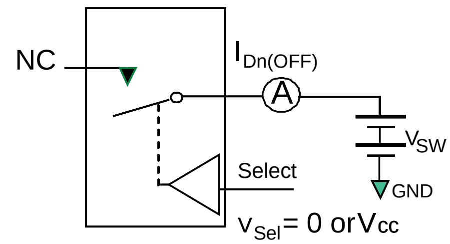
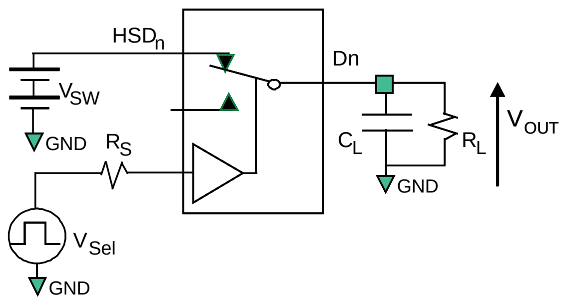


Figure 6. On Resistance



**Each switch port is tested separately

Figure 7. Off Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 8. AC Test Circuit Load

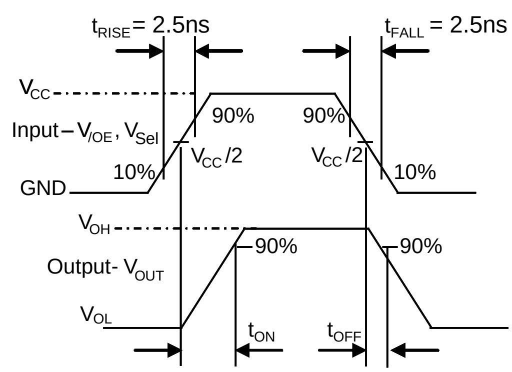


Figure 9. Turn-On / Turn-Off Waveforms

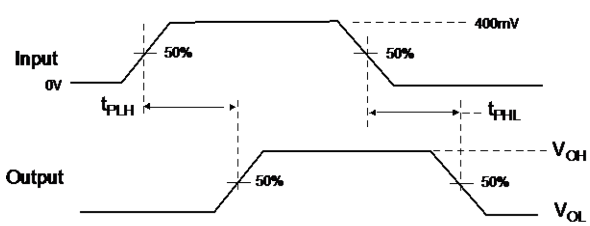


Figure 10. Propagation Delay ($t_R t_F$ – 500ps)

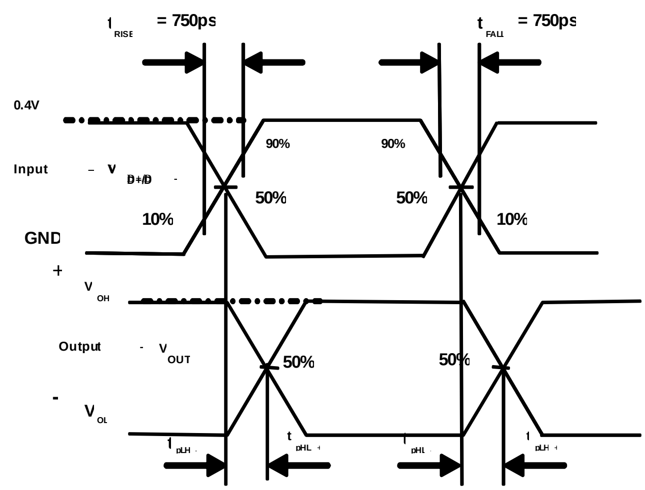
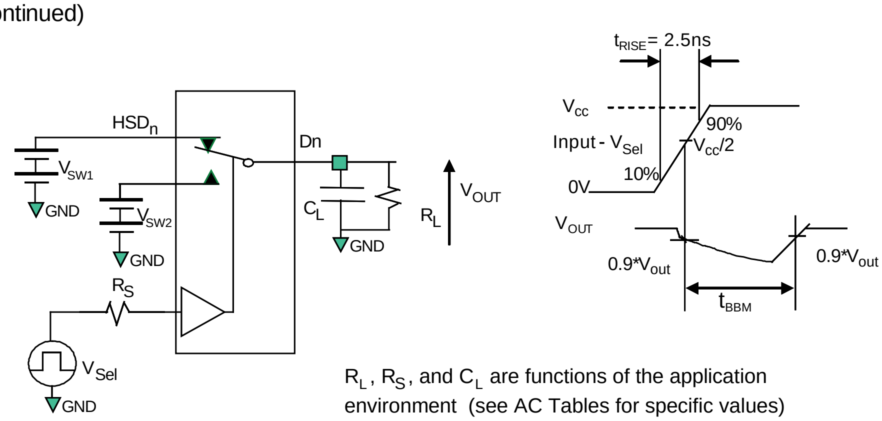


Figure 11. Skew Test Waveforms

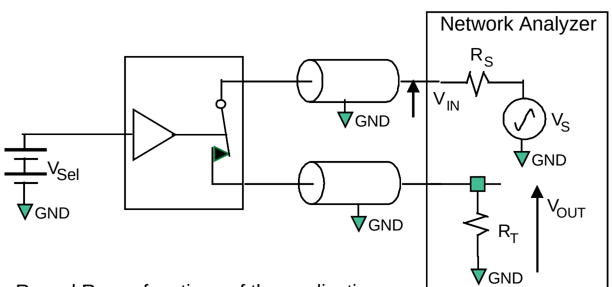
$t_{SK(P)}$=| t_{PLH-} – t_{PHL-} | or | t_{PLH+} – t_{PHL+} |
$t_{SK(I)}$=| t_{PLH-} – t_{PHL+} | or | t_{PLH+} – t_{PHL-} |

Test Diagrams (Continued)



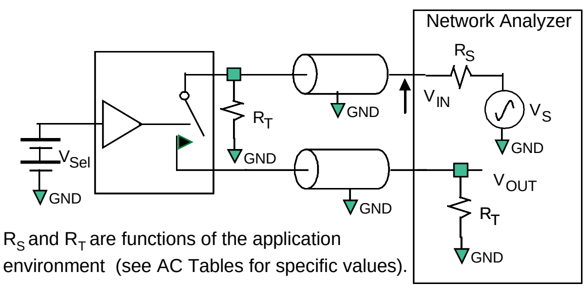
R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 12. Break-Before-Make Interval Timing



R_S and R_T are functions of the application environment (see AC Tables for specific values).

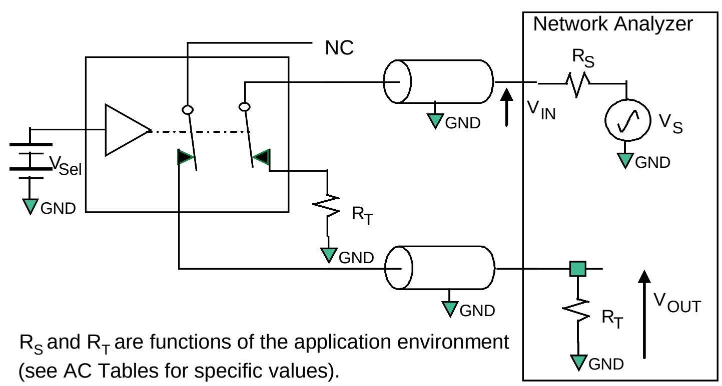
Figure 13. Bandwidth



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log (V_{OUT} / V_{IN})

Figure 14. Channel Off Isolation



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 15. Non-Adjacent Channel-to-Channel Crosstalk

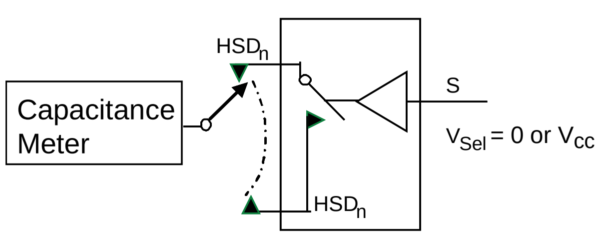


Figure 16. Channel Off Capacitance

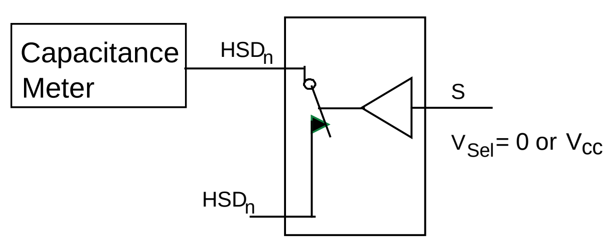
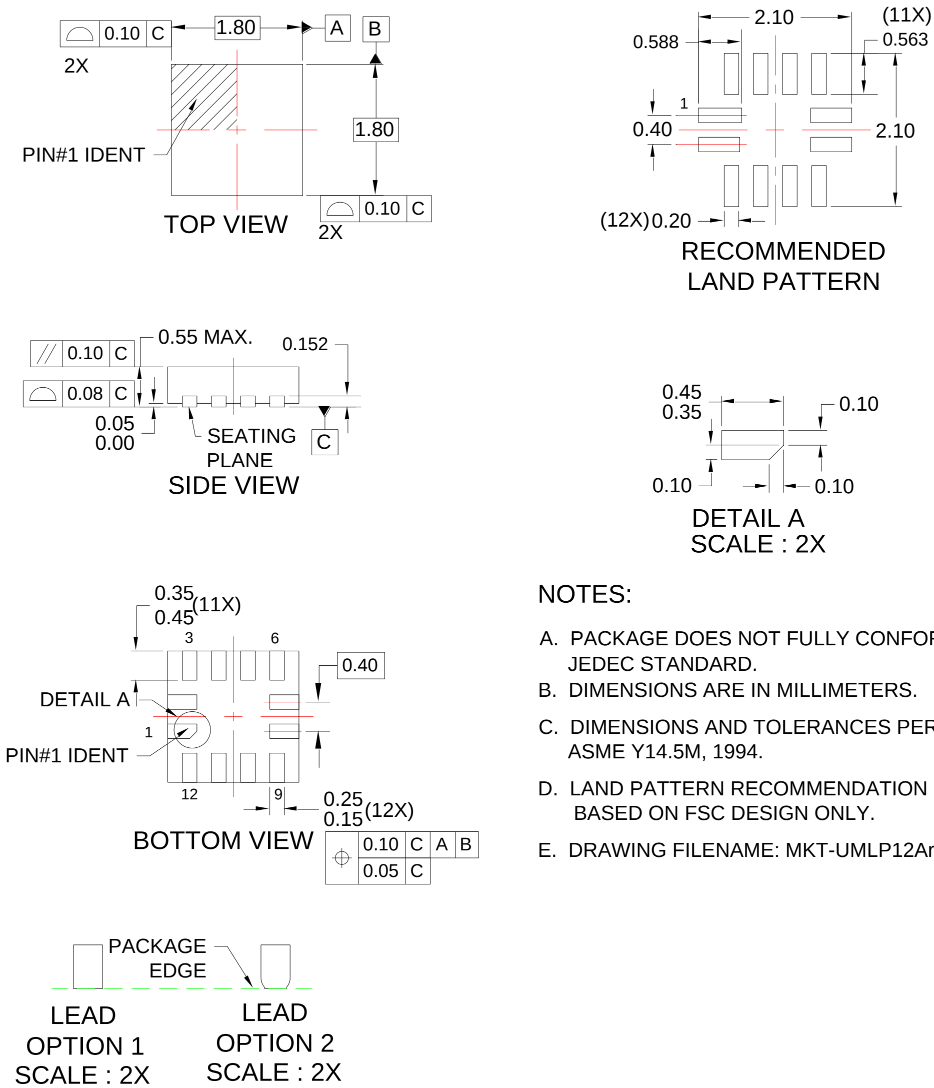


Figure 17. Channel On Capacitance

Physical Dimensions



NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.

E. DRAWING FILENAME: MKT-UMLP12Arev4.

Figure 18. 12-Lead, Ultrathin Molded Leadless Package (UMLP)

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSUSB63UMX	KG	-40 to +85°C	12-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8mm x 1.8mm x 0.55mm, 0.4mm pitch

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor's worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.

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