Data Sheet | September 1998 | File Number 2893.3

12MHz, High Input Impedance, Operational Amplifier

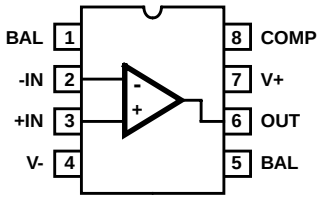
HA-2515 is a high performance operational amplifier which sets the standards for maximum slew rate, highest accuracy and widest bandwidths for internally compensated devices. In addition to excellent dynamic characteristics, this dielectrically isolated amplifier also offers low offset current and high input impedance.

The ±60V/µs slew rate and 250ns (0.1%) settling time of this amplifier is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in RF and video applications. For accurate signal conditioning this amplifier also provides 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

MIL-STD-883 product and data sheets available upon request.

Pinout

HA-2515
(PDIP, CERDIP)
TOP VIEW



Features

- Slew Rate 60V/µs
- Fast Settling 250ns
- Full Power Bandwidth 1MHz
- Gain Bandwidth 12MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA
- Internally Compensated for Unity Gain Stability

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HA3-2515-5	0 to 75	8 Ld PDIP	E8.3
HA7-2515-5	0 to 75	8 Ld CERDIP	F8.3A

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 15V
Peak Output Current 50mA

Operating Conditions

Temperature Range
HA-2515-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	96	N/A
CERDIP Package	135	50

Maximum Junction Temperature (Hermetic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$

PARAMETER	TEMP (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	25	-	5	10	mV
	Full	-	-	14	mV
Offset Voltage Average Drift	Full	-	30	-	$\mu V/^oC$
Bias Current	25	-	125	250	nA
	Full	-	-	500	nA
Offset Current	25	-	20	50	nA
	Full	-	-	100	nA
Input Resistance (Note 2)	25	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 3, 6)	25	7.5	15	-	kV/V
	Full	5	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	74	90	-	dB
Gain Bandwidth Product (Note 5)	25	-	12	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 3)	Full	±10.0	±12.0	-	V
Output Current (Note 6)	25	±10	±20	-	mA
Full Power Bandwidth (Notes 6, 11)	25	600	1000	-	kHz
TRANSIENT RESPONSE					
Rise Time (Notes 3, 7, 8, 9)	25	-	25	50	ns
Overshoot (Notes 3, 7, 8, 9)	25	-	25	50	%
Slew Rate (Notes 3, 7, 9, 12)	25	±40	±60	-	V/µs
Settling Time to 0.1% (Notes 3, 7, 9, 12)	25	-	0.25	-	µs
POWER SUPPLY CHARACTERISTICS					
Supply Current	25	-	4	6	mA
Power Supply Rejection Ratio (Note 10)	Full	74	90	-	dB

NOTES:

2. This parameter value is based on design calculations.
3. $R_L = 2k\Omega$.
4. $V_{CM} = \pm10V$
5. $A_V > 10$.
6. $V_O = \pm10V$.
7. $C_L = 50pF$.
8. $V_O = \pm200mV$.
9. See Transient Response Test Circuits and Waveforms.
10. $\Delta V = \pm5V$.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/$2\pi V_{PEAK}$.
12. $V_{OUT} = \pm5V$.

Test Circuits and Waveforms

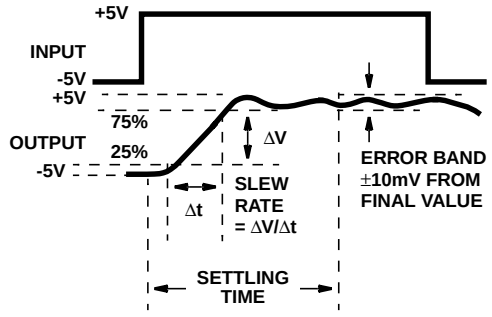
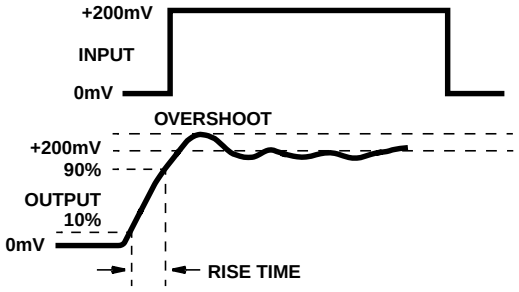


FIGURE 1. SLEW RATE AND SETTLING TIME



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE

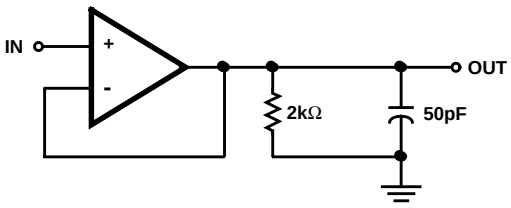
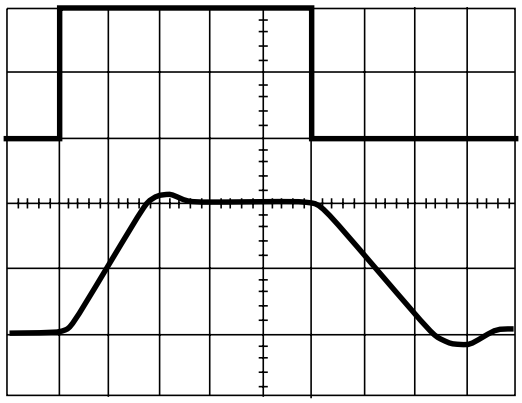
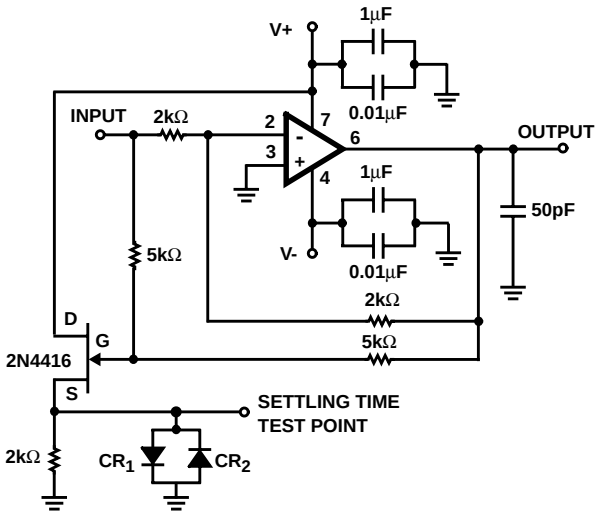


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE



R_L = 2kΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output
Vertical = 5V/Div.
Horizontal = 200ns/Div.
$T_A = 25^oC$, V_S = ±15V

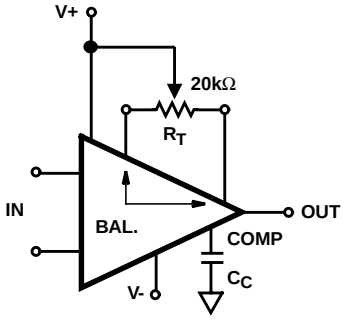
FIGURE 4. VOLTAGE FOLLOWER PULSE RESPONSE



NOTES:

13. A_V = -1.
14. Feedback and summing resistor ratios should be 0.1% matched.
15. Clipping diodes CR_1 and CR_2 are optional. HP5082-2810 recommended.

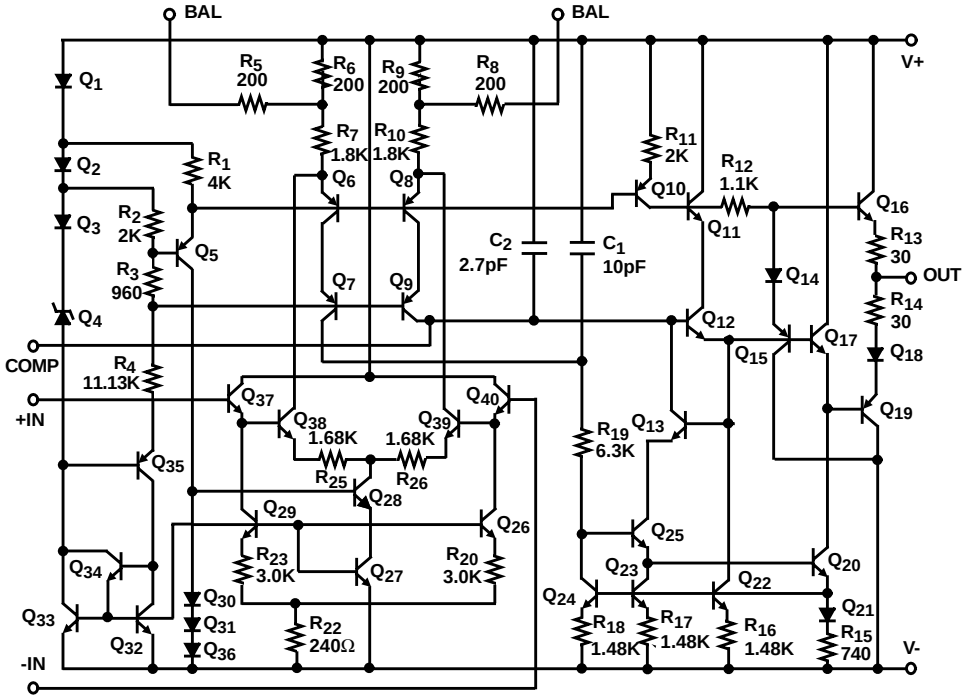
FIGURE 5. SETTLING TIME TEST CIRCUIT



NOTE: Tested offset adjustment range is IVOS + 1mVI minimum referred to output. Typical ranges are ±6mV with R_T = 20kΩ.

FIGURE 6. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK UP

Schematic


BAL
BAL
V+
Q1
R5 200
R6 200
R9 200
R8 200
R7 1.8K
R10 1.8K
R11 2K
R12 1.1K
Q2
R1 4K
Q6
Q8
Q10
Q16
Q3
R2 2K
Q5
C2 2.7pF
C1 10pF
Q11
R13 30
OUT
R3 960
Q7
Q9
Q14
R14 30
Q4
Q12
Q17
Q18
COMP
R4 11.13K
Q15
Q37
Q40
Q19
+IN
Q38 1.68K
Q39 1.68K
R19 6.3K
Q13
Q35
R25
R26
Q28
Q29
Q26
Q25
R23 3.0K
Q27
R20 3.0K
Q23
Q20
Q34
Q22
Q24
Q21
Q33
Q30
Q31
R22 240Ω
R18 1.48K
R17 1.48K
R16 1.48K
R15 740
Q32
Q36
-IN
V-

Typical Performance Curves

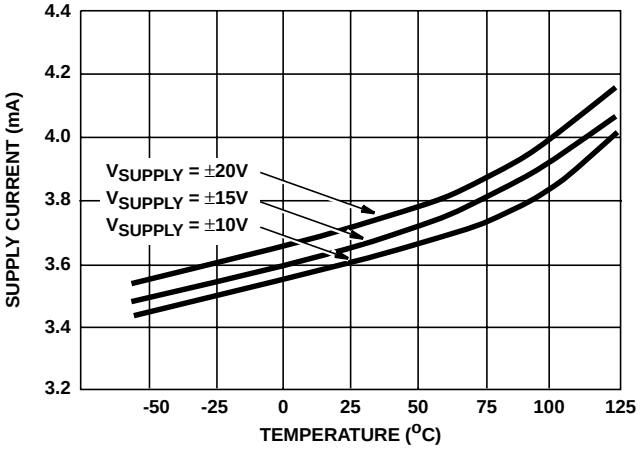


FIGURE 7. POWER SUPPLY CURRENT vs TEMPERATURE

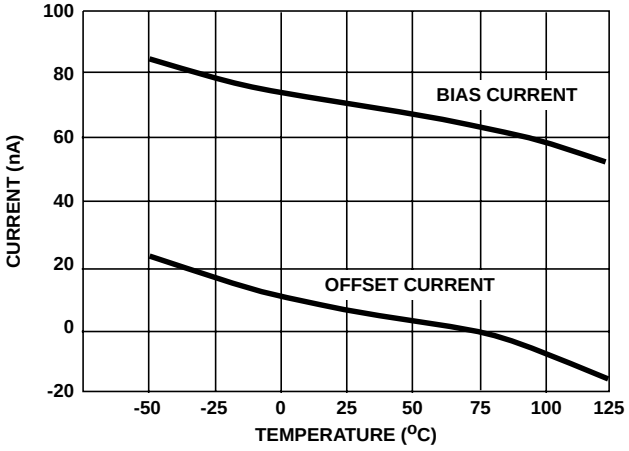


FIGURE 8. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

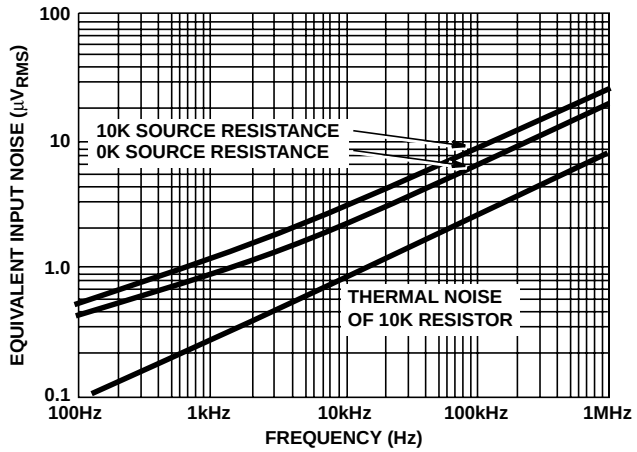


FIGURE 9. EQUIVALENT INPUT NOISE vs BANDWIDTH (WITH 10Hz HIGH PASS FILTER)

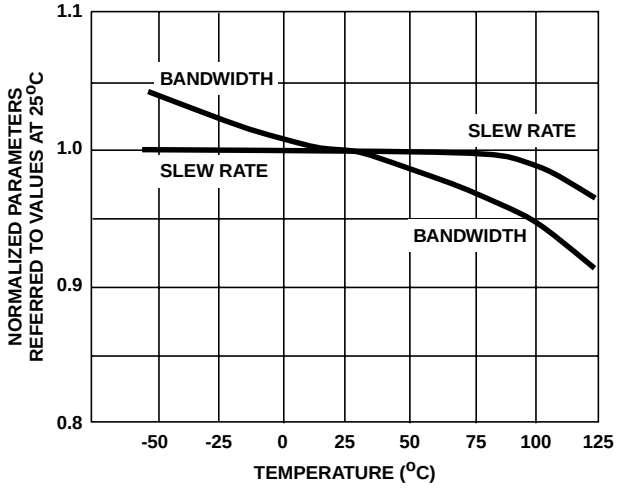


FIGURE 10. NORMALIZED AC PARAMETERS vs TEMPERATURE

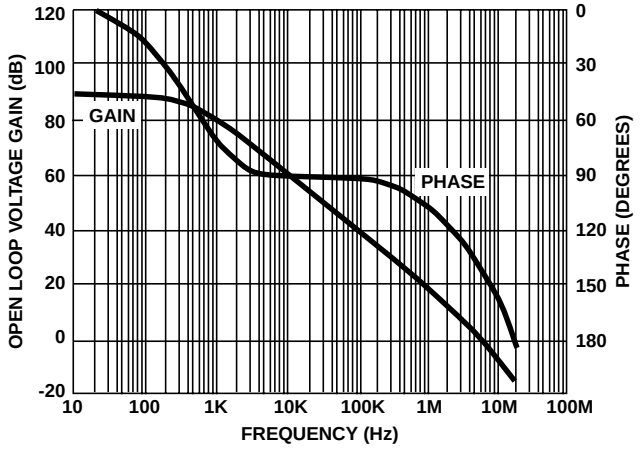


FIGURE 11. OPEN LOOP GAIN AND PHASE RESPONSE

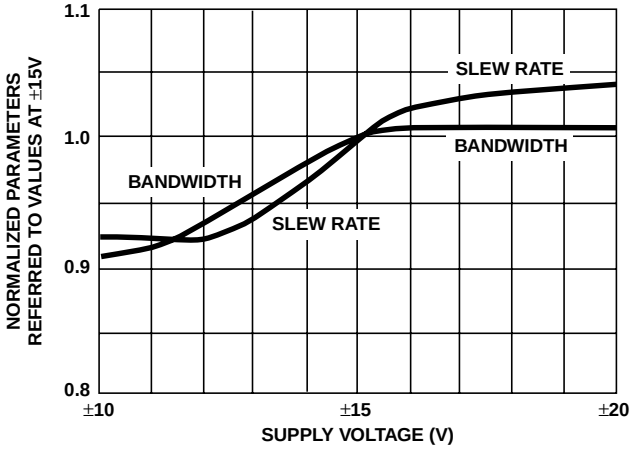


FIGURE 12. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT 25°C

Typical Performance Curves (Continued)

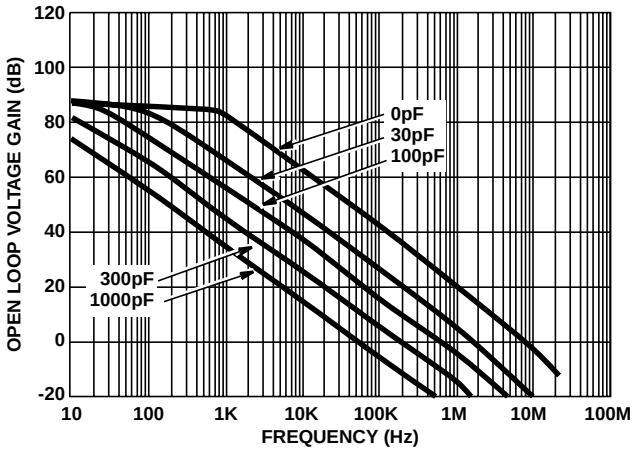


FIGURE 13. OPEN LOOP GAIN RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

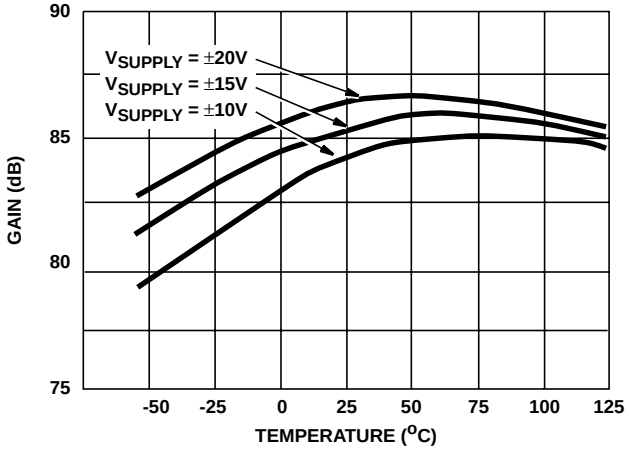


FIGURE 14. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

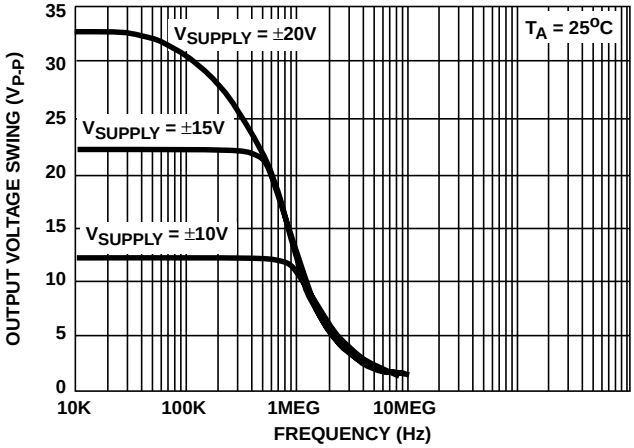


FIGURE 15. OUTPUT VOLTAGE SWING vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

65 mils x 57 mils x 19 mils
1650µm x 1450µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

Unbiased

TRANSISTOR COUNT:

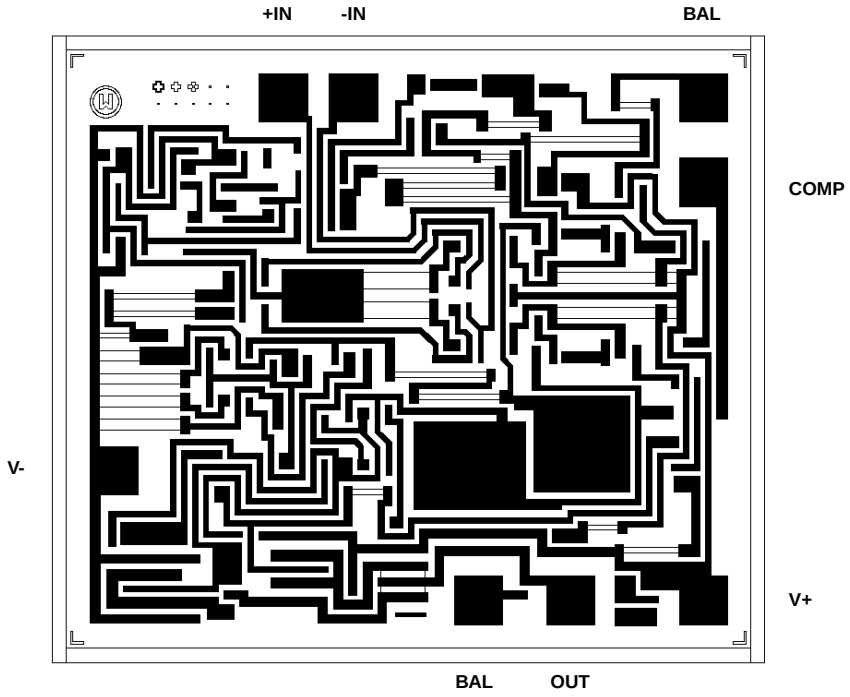
40

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2515



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