January 1999 FN2923.4

100MHz Current Feedback Amplifier

The HA-5004 current feedback amplifier is a video/wideband amplifier optimized for low gain applications. The design is based on current-mode feedback which allows the amplifier to achieve higher closed loop bandwidth than voltage-mode feedback operational amplifiers. Since feedback is employed, the HA-5004 can offer better gain accuracy and lower distortion than open loop buffers. Unlike conventional op amps, the bandwidth and rise time of the HA-5004 are nearly independent of closed loop gain. The 100MHz bandwidth at unity gain reduces to only 65MHz at a gain of 10. The HA-5004 may be used in place of a conventional op amp with a significant improvement in speed power product.

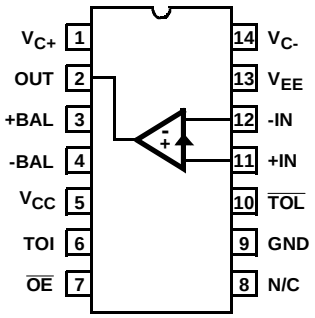
Several features have been designed in for added value. A thermal overload feature protects the part against excessive junction temperature by shutting down the output. If this feature is not needed, it can be inhibited via a TTL input (TOI). A TTL chip enable/disable ($\overline{OE}$) is also provided; when the chip is disabled its output is high impedance. Finally, an open collector output flag ($\overline{TOL}$) is provided to indicate the status of the chip. The status flag goes low to indicate when the chip is disabled due to either the internal Thermal Overload shutdown or the external disable.

In order to maximize bandwidth and output drive capacity, internal current limiting is not provided. However, current limiting may be applied via the V_C+ and V_C- pins which provide power separately to the output stage.

For Military grade product refer to the HA-5004/883 data sheet.

Pinout

HA-5004
(CERDIP)
TOP VIEW



Features

- Slew Rate 1200V/µs
- Output Current . . . . . ±100mA
- Drives . . . . . ±9V into 100Ω
- V_{SUPPLY} . . . . . ±5V to ±18V
- Thermal Overload Protection and Output Flag
- Bandwidth Nearly Independent of Gain
- Output Enable/Disable

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- High Speed Peak Detector
- Fiber Optic Transmitters
- Zero Insertion Loss Transmission Line Drivers
- Current to Voltage Converter
- Radar Systems

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA1-5004-5	0 to 70	14 Ld CERDIP	F14.3

TRUTH TABLE

INPUTS		TEMP	$\overline{TOL}$ OUTPUT (OPEN COLLECTOR)	OPERATION
$\overline{OE}$	TOI	T_J		
0	0	Normal	1	Normal
0	0	High (Note)	0	Auto Shutdown, HI-Z OUT
0	1	X	1	Normal
1	X	X	0	Manual Shutdown, HI-Z OUT

NOTE: >180^{o}C Typical

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 40V
Differential Input Voltage 5V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Output Current . . . . . ±120mA Max (≤25% Duty Cycle)

Operating Conditions

Temperature Range
HA-5004-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20

Maximum Junction Temperature (Note 1) . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including load condition, must be designed to maintain the junction temperature below 175^oC. See Thermal Resistances in the "Thermal Information" section.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE}$ = 0.8V, TOI = 0.8V or 2.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		25	-	1	5	mV
		Full	-	-	20	mV
Average Offset Voltage Drift		Full	-	10	-	$\mu V/^oC$
Bias Current (+Input Only) (Note 3)		25	-	2	5	µA
		Full	-	-	20	µA
Input Resistance (-Input)		25	-	6.5	-	Ω
Input Resistance (+Input)		25	-	3	-	MΩ
Input Capacitance		25	-	3	-	pF
Common Mode Range		Full	±10	-	-	V
DISTORTION AND NOISE						
Total Harmonic Distortion ($2V_{P-P}$, 200kHz)	A_{VCL} = +1	25	-	-72	-	dBc
	A_{VCL} = +2	25	-	-70	-	dBc
	A_{VCL} = +5	25	-	-68	-	dBc
Input Noise Voltage	10Hz to 1MHz	25	-	15	-	μV_{P-P}
Input Noise Voltage Density (Note 4)	f = 10kHz	25	-	2.2	-	$nV/\sqrt{Hz}$
	f = 100kHz	25	-	2.2	-	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 4)	f = 10kHz	25	-	6	-	$pA/\sqrt{Hz}$
	f = 100kHz	25	-	4	-	$pA/\sqrt{Hz}$
DIGITAL I/O CHARACTERISTICS						
Logic Inputs (OE and TO)	V_{IH}	Full	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	V
	I_{IH} at V_I = 2.4V	Full	-	-	1	µA
	I_{IH} at V_I = 0.4V	Full	-	-	10	µA
Logic Output (TOL) (Open Collector)	V_{OL} at 800µA	Full	-	0.05	0.4	V

Electrical Specifications $V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE} = 0.8V$, TOI = 0.8V or 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS						
DC Gain Error (Note 5)	Small Signal (±100mV)	25	-	0.25	0.43	%
		Full	-	0.25	0.75	%
	Large Signal (±10V) ($R_L = 1k\Omega$)	25	-	0.25	0.43	%
		Full	-	0.25	0.75	%
DC Voltage Gain	Small and Large Signal	25	233	400	-	V/V
		Full	133	400	-	V/V
DC Transimpedance (Note 6)		25	-	100	-	V/mA
		Full	33	100	-	V/mA
-3dB Bandwidth (Note 7)	$A_V = +1$	25	-	100	-	MHz
Gain Flatness	DC to 5MHz	25	-	0.03	-	dB
	DC to 10MHz	25	-	0.05	-	dB
Differential Gain (Notes 7, 8, 9, 3.58MHz)	$A_{VCL} = +1$	25	-	0.035	-	%
	$A_{VCL} = +2$	25	-	0.058	-	%
Differential Gain (Notes 7, 8, 9, 4.43MHz)	$A_{VCL} = +1$	25	-	0.035	-	%
	$A_{VCL} = +2$	25	-	0.058	-	%
Differential Phase (Notes 7, 8, 3.58MHz)	$A_{VCL} = +1$	25	-	0.15	-	Degrees
	$A_{VCL} = +2$	25	-	0.23	-	Degrees
Differential Phase (Notes 7, 8, 4.43MHz)	$A_{VCL} = +1$	25	-	0.17	-	Degrees
	$A_{VCL} = +2$	25	-	0.24	-	Degrees
Common Mode Rejection Ratio	$V_{CM} = \pm10V$	Full	-	58	-	dB
Minimum Stable Gain		Full	1	-	-	V/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$R_L = 100\Omega$	25	±9.0	±9.5	-	V
	$R_L = 1k\Omega$	25	±11.5	±11.8	-	V
	$R_L = 100\Omega$	Full	±8.0	±9.5	-	V
	$R_L = 1k\Omega$	Full	±10.5	±11.8	-	V
Full Power Bandwidth	$A_V = +1$, $V_{OUT} = 4V_{P-P}$	25	-	50	-	MHz
Output Resistance, Open Loop		25	-	5	-	Ω
Output Current		25	±90	±100	-	mA
		Full	±80	±100	-	mA
Output Enable Time	HI-Z to ±2V	Full	-	100	-	ns
Output Disable Time	±2V to HI-Z	Full	-	3	-	µs
Output Leakage	Disabled	Full	-	-	1	µA
TRANSIENT RESPONSE						
Rise Time/Fall Time	200mV Step	25	-	6.3	-	ns
Propagation Delay	10V Step	25	-	7	-	ns
Slew Rate	10V Step	25	-	1200	-	V/µs
Settling Time	0.1%, 10V Step	25	-	50	-	ns
Overshoot		25	-	10	-	%
POWER SUPPLY CHARACTERISTICS						
Supply Current	Enabled	25	-	12	16	mA
		Full	-	-	22	mA
	Disabled	25	-	7	-	mA

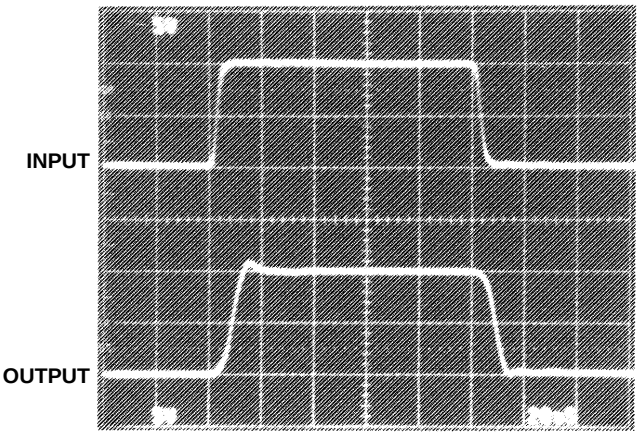
Electrical Specifications $V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE} = 0.8V$, TOI = 0.8V or 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio		Full	50	60	-	dB

NOTES:

3. The inverting input is a low impedance point; Bias Current and Offset Current, are not specified for this terminal.
4. See typical performance curves.
5. Gain Error $= \frac{1}{\text{DC Voltage Gain}} \times 100\%$.
6. DC Transimpedance $= \frac{R_F}{\text{Gain Error}}$, $R_F = 250\Omega$.
7. $V_{IN} = 300mV_{P-P}$.
8. $V_{OFFSET} = 1.0V$.
9. Differential Gain (dB) = 0.0869 Differential Gain (%).

Test Circuits and Waveforms



$A_V = +1$, $V_{SUPPLY} = \pm 15V$

Vertical Scale: 5V/Div.; Horizontal Scale: 20ns/Div.

LARGE SIGNAL RESPONSE, $A_V = +1$

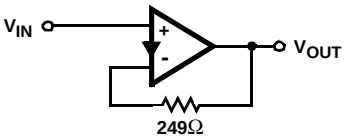
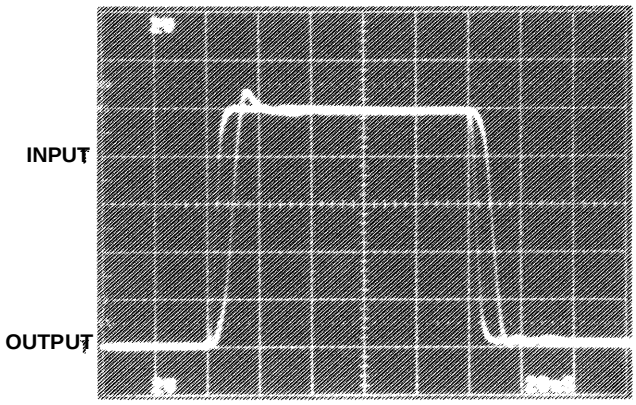


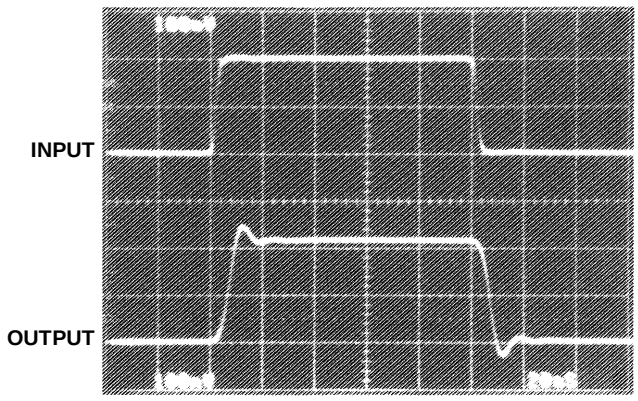
FIGURE 1. TEST CIRCUIT



$A_V = +1$, $V_{SUPPLY} = \pm 15V$

Vertical Scale: 2V/Div.; Horizontal Scale: 20ns/Div.

PROPAGATION DELAY

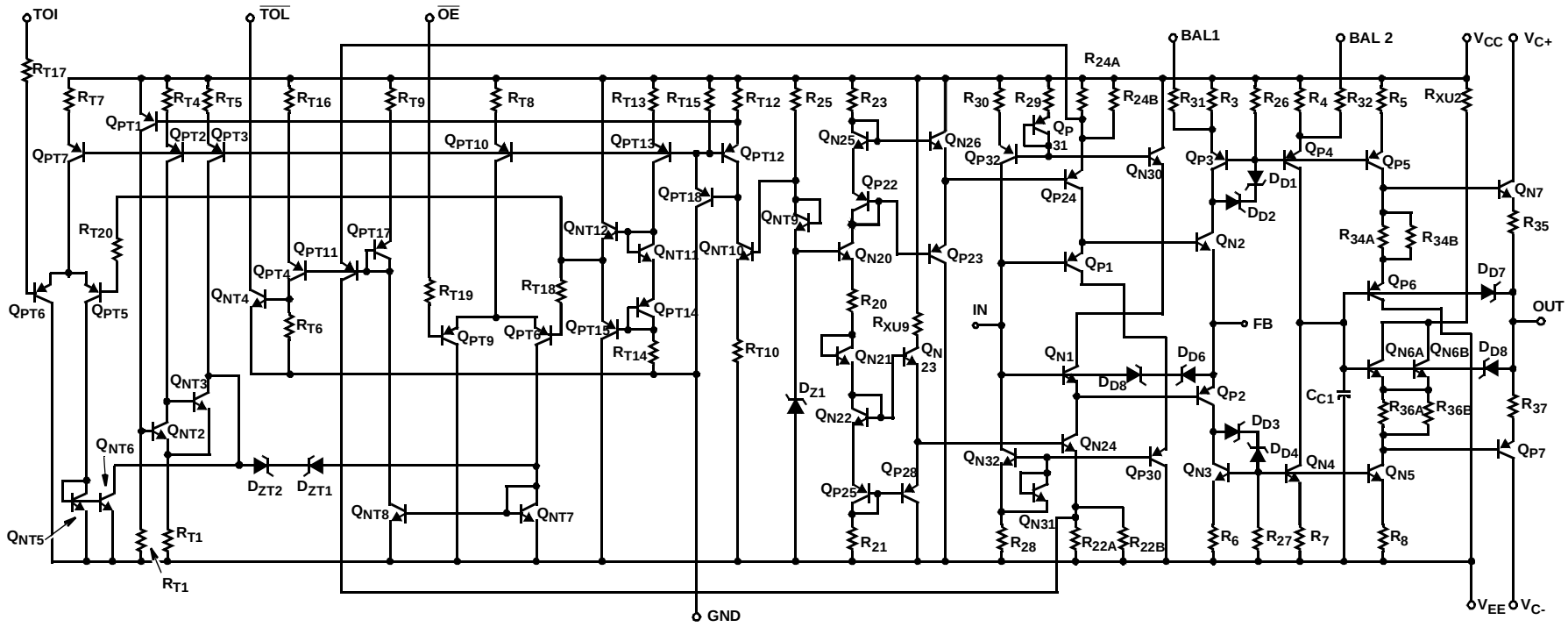


$A_V = +1$, $V_{SUPPLY} = \pm 15V$

Vertical Scale: 100mV/Div.; Horizontal Scale: 20ns/Div.

SMALL SIGNAL RESPONSE

Schematic Diagram



Application Information

Theory Of Operation

The HA-5004 is a high performance amplifier that uses current feedback to achieve its outstanding performance. Although it is externally configured like an ordinary op amp in most applications, its internal operation is significantly different.

Inside the HA-5004, there is a unity gain buffer from the non-inverting (+) input to the inverting-input (as suggested by the circuit symbol), and the inverting terminal is a low impedance point. Error currents are sensed at the inverting input and amplified; a small change in input current produces a large change in output voltage. The ratio of output voltage delta due to input current delta is the transimpedance of the device.

Steady state current at the inverting input is very small because the transimpedance is large. The voltage across the input terminals is nearly zero due to the buffer amplifier. These two properties are similar to standard op amps and likewise simplify circuit analysis.

Resistor Selection

The HA-5004 is optimized for a feedback resistor of 250Ω, regardless of gain configuration. It is important to note that this resistor is required even for unity gain applications; higher gain settings use a second resistor like regular op amp circuits as shown in Figure 2 below.

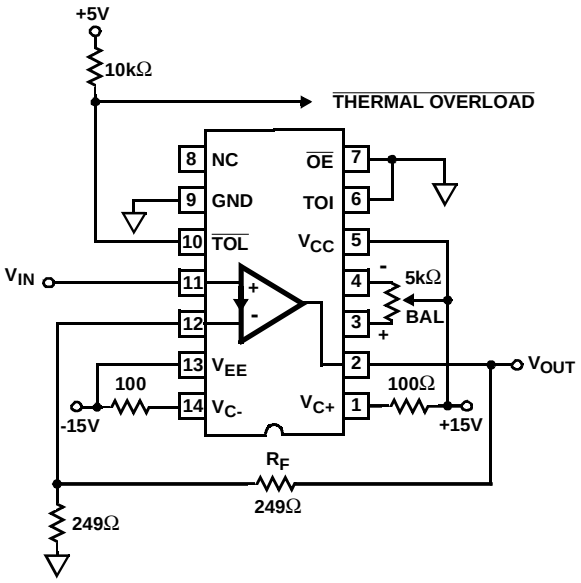


FIGURE 2. TYPICAL APPLICATION CIRCUIT, A_V = +2

Power Supplies

The HA-5004 will operate over a wide range of supply voltages with excellent performance. Supplies may be either single-ended or split, ranging from 6V (±3V) to 36V (±18V). Appropriate reduction in input and output signal excursion is necessary for operation at lower supply voltages. Bypass capacitors from each supply to ground are recommended, typically a 0.01μF ceramic in parallel with a 4.7μF electrolytic.

Current Limit

No internal current limiting is provided for the HA-5004 in order to maximize bandwidth and slew rate. However, power is supplied separately to the output stage via pins 1 (V_C+) and 14 (V_C-) so that external current limiting resistors may be used. If required, 100Ω resistors to each supply rail are recommended.

Enable/Disable and Thermal Overload Operation

The HA-5004 operates normally with a TTL low state on pin 7 ($\overline{OE}$) but it may be disabled manually by a TTL high state at this input. When disabled, the output and inverting-input go to a high impedance state and the circuit is electrically debiased, reducing supply current by about 5mA. It is important to keep the differential input voltage below the absolute maximum rating of 5V when the device is disabled.

If the power dissipation becomes excessive and chip temperature exceeds approximately 180^{o}C, the HA-5004 will automatically disable itself. The thermal overload condition will be indicated by a low state at the $\overline{TOL}$ output on pin 10. ($\overline{TOL}$ is also low for manual shutdown via pin 7). Automatic thermal shutdown can be bypassed by a TTL high state on Thermal Overload Inhibit (TOI) pin 6. See the truth table for a summary of operation.

Offset Adjustment

Offset voltage may be nulled with a 5kΩ potentiometer between pins 3 and 4, center tapped to the positive supply. Setting the slider towards pin 3 (+BAL) increases output voltage; towards pin 4 (-BAL) decreases output voltage. Offset can be adjusted by about ±10mV with a 5K pot; this range is extended with a lower resistance potentiometer.

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $T_A = 25^0C$, Unless Otherwise Specified

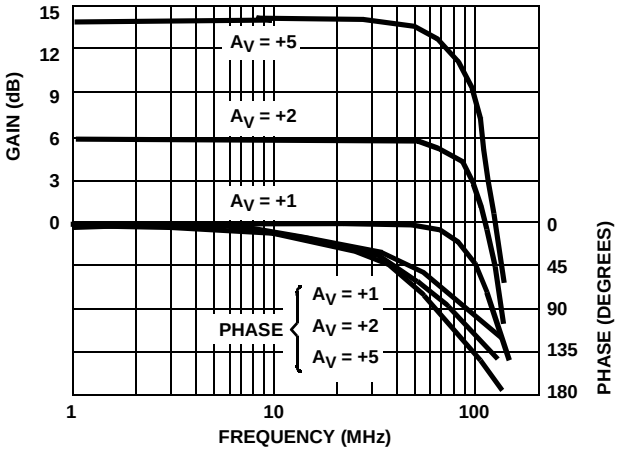


FIGURE 3. GAIN AND PHASE vs FREQUENCY

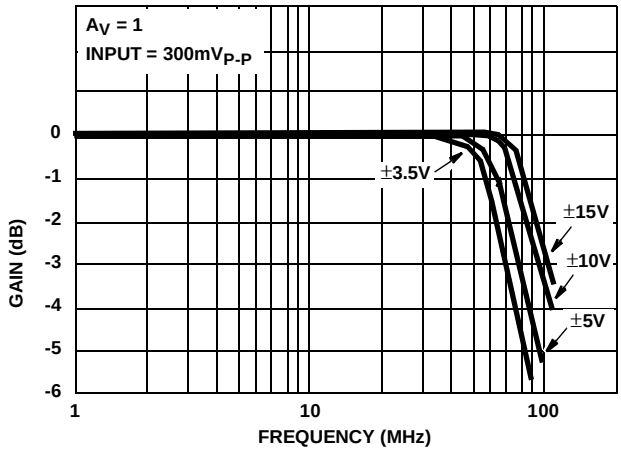


FIGURE 4. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

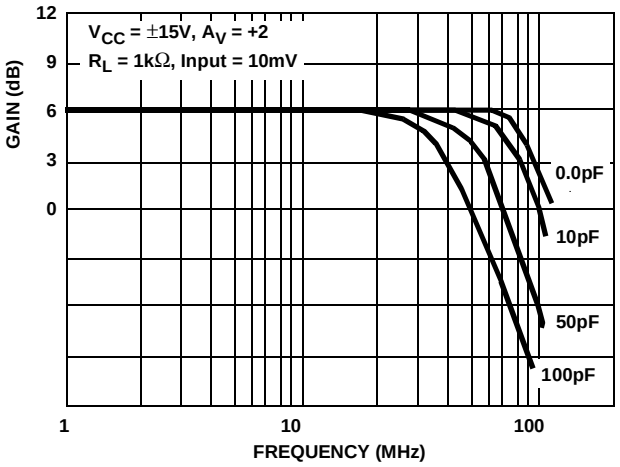


FIGURE 5. FREQUENCY RESPONSE vs C_L

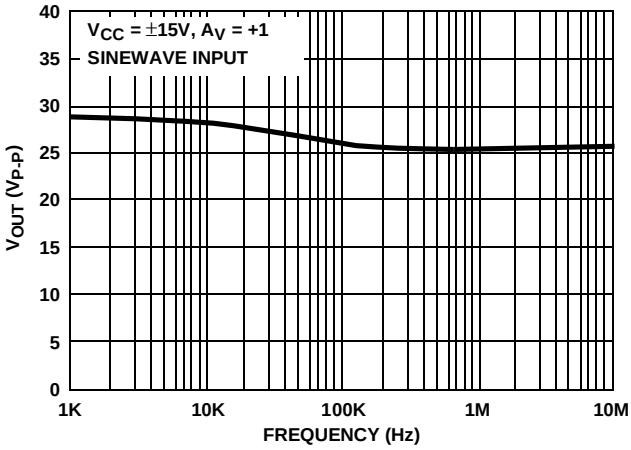


FIGURE 6. MAXIMUM UNDISTORTED SINEWAVE OUTPUT vs FREQUENCY

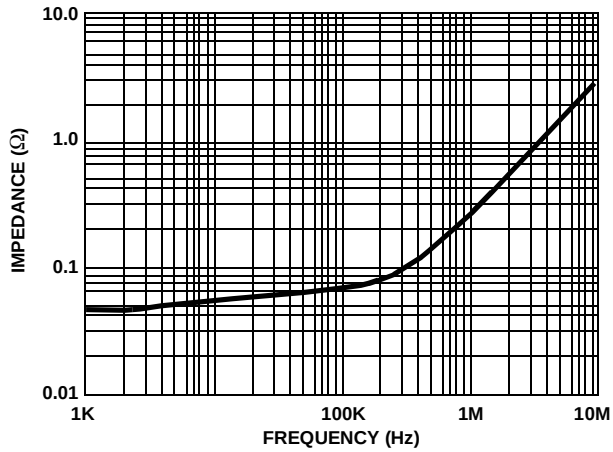


FIGURE 7. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

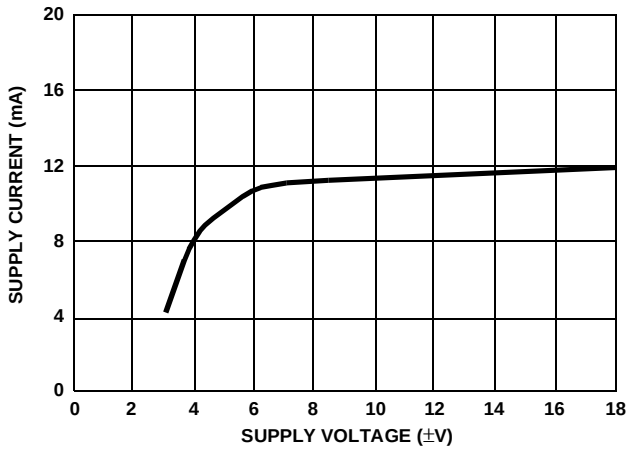


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

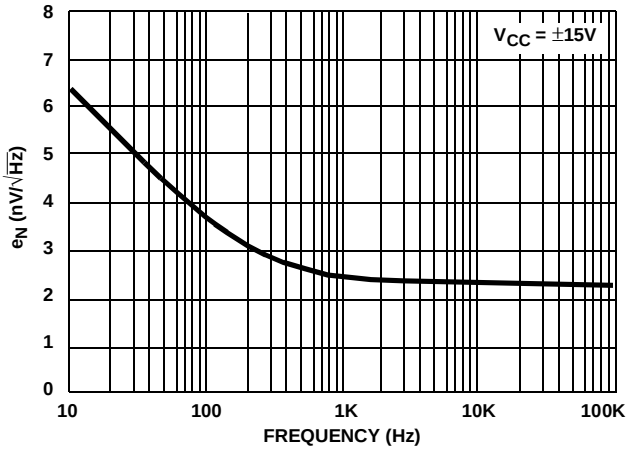


FIGURE 9. NOISE VOLTAGE vs FREQUENCY

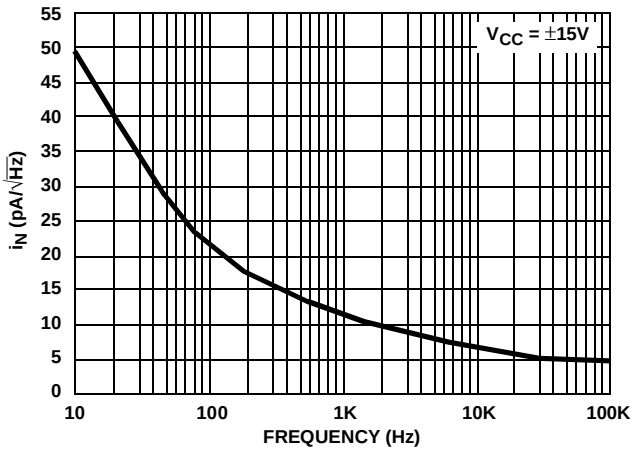


FIGURE 10. NOISE CURRENT vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

63 mils x 93 mils x 19 mils
1600µm x 2370µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over (Silox, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V_{EE}

TRANSISTOR COUNT:

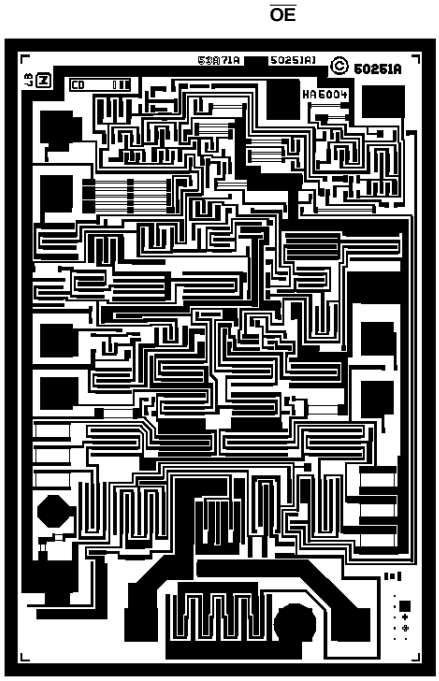
64

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5004



Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
7585 Irvine Center Drive
Suite 100
Irvine, CA 92618
TEL: (949) 341-7000
FAX: (949) 341-7123

Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7946

EUROPE

Intersil Europe Sarl
Ave. William Graisse, 3
1006 Lausanne
Switzerland
TEL: +41 21 6140560
FAX: +41 21 6140579

ASIA

Intersil Corporation
Unit 1804 18/F Guangdong Water Building
83 Austin Road
TST, Kowloon Hong Kong
TEL: +852 2723 6339
FAX: +852 2730 1433