October 1999 FN3738.1

Continuously Variable Slope Delta-Modulator (CVSD)

The HC-55564/883 is a half duplex modulator/demodulator CMOS intergrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/demodulation.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization. The device may be easily configured with the National TP3040 PCM/CVSD filter.

The HC-55564/883 is usable from 9k bits/sec to above 64kbps. For more applications information, see Application Notes AN576 and AN607.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC1-55564/883	-55^{o}C to +125^{o}C	14 Lead CerDIP
HC4-55564/883	-55^{o}C to +125^{o}C	20 Lead Ceramic LCC

Features

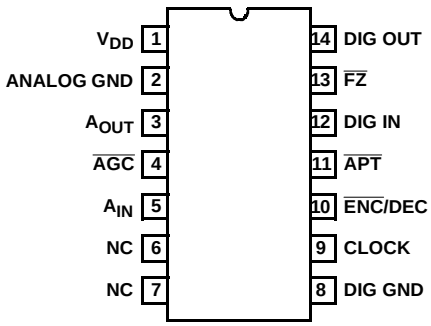
- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.Requires Few External Parts
- All Digital
- Requires Few External Parts
- Low Power Drain
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems: Automatic Offset Adjustment
- Half Duplex Operation Under Digital Control
- Filter Reset Under Digital Control
- Automatic Overload Recovery
- Automatic “Quiet” Pattern Generation
- AGC Control Signal Available

Applications

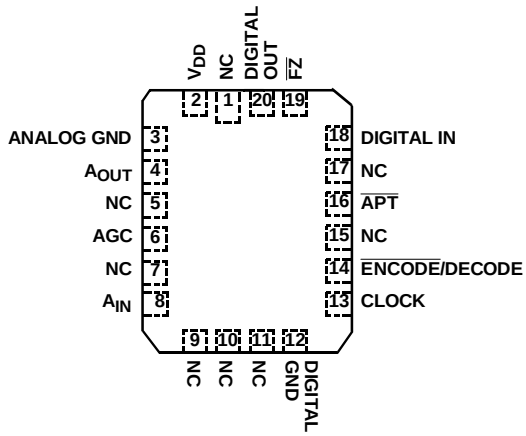
- Voice Transmission Over Data Channels (Modems)
- Voice/Data Multiplexing (Pair Gain)
- Voice Encryption/Scrambling
- Voicemail
- Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, etc.
- Pagers/Satellites
- Data Acquisition Systems
- Voice I/O for Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability

Pinouts

HC-55564/883
(CERDIP)
TOP VIEW



HC-55564/883
(CLCC)
TOP VIEW



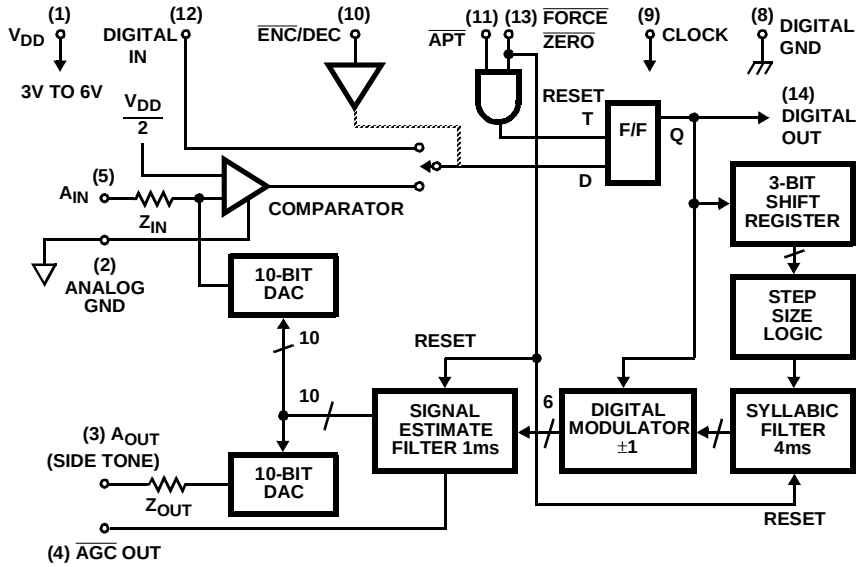
Pin Description

PIN NO. 14 LEAD DIP	PIN NO. 20 LEAD LCC	SYMBOL	DESCRIPTION
1	2	V_{DD}	Positive Supply Voltage. Voltage range is +3.2V to +6.0V.
2	3	Analog GND	Analog Ground connection to D/A ladders and comparator.
3	4	A_{OUT}	Audio Out recovered from 10-bit DAC. May be used as side tone at the transmitter. Presents approximately 75kΩ source with DC offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally AC coupled.
4	6	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	8	A_{IN}	Audio Input to comparator. Should be externally AC coupled. Presents approximately 200kΩ in series with $V_{DD}/2$.
6, 7	1, 5, 7, 9, 10, 11, 15, 17	NC	No internal connection is made to these pins.
8	12	Digital GND	Logic ground. 0V reference for all logic inputs and outputs.
9	13	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	14	$\overline{Encode}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	16	$\overline{APT}$	Alternate Plain Text input. Activating this input caused a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	18	Digital In	Input for the received digital NRZ data.
13	19	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the “quieting” condition. An alternating 1-0 pattern appears at the digital output at 1/2 the clock rate. When this is decoded by a receive CVSD, a 10mV_{P-P} inaudible signal appears at audio output. Active low.
14	20	Digital Out	Output for transmitted digital NRZ data.

NOTE:

1. No active input should be left in a “floating condition”.

Functional Diagram



Absolute Maximum Ratings

Voltage at Any Pin . . . . . GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage . . . . . +6.0V
Minimum V_{DD} Voltage . . . . . +3.2V
Junction Temperature . . . . . +175^{o}C
Storage Temperature Range . . . . . -65^{o}C to +150^{o}C
Lead Temperature (Soldering 10s) . . . . . +300^{o}C
ESD Rating . . . . . <2000V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	66^{o}C/W	16^{o}C/W
Ceramic LCC Package	65^{o}C/W	15^{o}C/W

Package Power Dissipation Limit at +75^{o}C for T_J at ≤ +175^{o}C
CerDIP Package 1.52W
Ceramic LCC Package 1.54W
Package Power Dissipation Derating Factor Above +75^{o}C
CerDIP Package . . . . . 15.2W/^{o}C
Ceramic LCC Package . . . . . 15.4W/^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Operating Temperature Range . . . . . -55^{o}C to +125^{o}C
Operating Supply Voltage (V_{DD} Range) . . . . . +3.2V to +6.0V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = +5V, fclk = 16kHz, Operating Temperature = -55^{o}C ≤ T_A ≤ +125^{o}C, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS TYP	LIMITS MAX	UNITS
Supply Current	I_{DD}	Encode Mode: A_{IN} = 0V	1	+25^{o}C	-	1.5	mA
			2, 3	+125^{o}C, -55^{o}C	-	1.5	mA
Logic Input High (Note 2)	V_{IH}	Input Level: '1' = +3.5V, '0' = +1.5V	1	+25^{o}C	3.5	-	V
			2, 3	+125^{o}C, -55^{o}C	3.5	-	V
Logic Input Low (Note 2)	V_{IL}	Input Level: '1' = +3.5V, '0' = +1.5V	1	+25^{o}C	-	1.5	V
			2, 3	+125^{o}C, -55^{o}C	-	1.5	V
Logic Output High (Note 3)	V_{OH}	I_{LOAD} = -40μA	1	+25^{o}C	4.0	-	V
			2, 3	+125^{o}C, -55^{o}C	4.0	-	V
Logic Output Low (Note 3)	V_{OL}	I_{LOAD} = +0.8mA	1	+25^{o}C	-	0.4	V
			2, 3	+125^{o}C, -55^{o}C	-	0.4	V
Quieting Pattern Amplitude (Note 8)	V_{QP}	$\overline{FZ}$ = 0; Clock Inputs Switched Statically	1	+25^{o}C	-	14	mV_{P-P}
			2, 3	+125^{o}C, -55^{o}C	-	14	mV_{P-P}
AGC Threshold (Note 9)	V_{ATH}	Encode Mode	1	+25^{o}C	0.45	0.65	F.S.
			2, 3	+125^{o}C, -55^{o}C	0.45	0.65	F.S.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank.

TABLE 3. ELECTRICL PERFORMANCE CHARACTERISTICS

Devices Characterized at: V_{DD} = +5.0V, T_A = +25^{o}C, Operating Temperature, fclk = 16kHz Clock Sampling Rate.
$\overline{ENC}$/DDC = $\overline{ENC}$ = Encode Mode, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS TYP	LIMITS MAX	UNITS
Sampling Rate	CLK	A_{IN} = 0.775 V_{RMS} at 20Hz	1, 12	+25^{o}C	9	64	kBS
				+125^{o}C, -55^{o}C	9	64	kBS
CLK Duty Cycle		A_{IN} = 0.775 V_{RMS} at 100Hz	12	+25^{o}C	30	70	%
				+125^{o}C, -55^{o}C	30	70	%

TABLE 3. ELECTRICL PERFORMANCE CHARACTERISTICS (Continued)

Devices Characterized at: V_{DD} = +5.0V, T_A = +25°C, Operating Temperature, fclk = 16kHz Clock Sampling Rate. $\overline{ENC}$/DDC = $\overline{ENC}$ = Encode Mode, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					TYP	MAX	
Audio Input Voltage	A_{IN}	A_{IN} = 100Hz	4, 12	+25°C	-	1.2	V_{RMS}
				+125°C, -55°C	-	1.2	V_{RMS}
Audio Output Voltage	A_{OUT}	A_{IN} = 100Hz	5, 12	+25°C	-	1.2	V_{RMS}
				+125°C, -55°C	-	1.2	V_{RMS}
Input Impedance	Z_{IN}	A_{IN} = 100Hz	6, 12	+25°C	150	500	kΩ
				+125°C, -55°C	150	500	kΩ
Output Impedance	Z_{OUT}	A_{IN} = 100Hz	6, 12	+25°C	35	25	kΩ
				+125°C, -55°C	35	25	kΩ
Transfer Gain	A_{E-D}	A_{IN} = 0.775 V_{RMS} at 100Hz	11, 12	+25°C	-2	+2	dB
				-55°C, +125°C	-2	+2	dB
Resolution	RES	A_{IN} at 100Hz. Note 8	12, 13	+25°C	0.3	-	% of Supply
MIN Step Size	MSS		7, 12	+25°C	0.10	0.14	% of Supply
Clamping Threshold	V_{CTH}		10, 12	+25°C	0.70	0.90	F.S.

NOTES:

1. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground; however, the short circuit duty cycle must not exceed 5% in order to maintain an acceptable current density level. Digital data output is NRZ and changes with negative clock transitions. Each output will drive one LS TTL loads.
4. Recommended voice input range for best voice performance. Should be externally AC coupled.
5. May be used for side-tone in encode mode. Should be externally AC coupled.
6. Presents series impedance with audio signal. Zero signal reference is approximately $V_{DD}/2$. Varies with audio input level by ±2dB.
7. The minimum audio output voltage change that can be produced by the internal DAC.
8. The “quieting” pattern or idle-channel audio output steps at 1/2 the bit rate, changing state on negative clock transitions.
9. A logic “0” will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e. at $V_{DD}/2$ ±25% of V_{DD}.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).
11. No load condition measured from audio in to audio out.
12. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
13. The minimum audio input voltage above which encoding is guaranteed to take place.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
82 x 147 x 20 ± 1 mils

METALLIZATION:
Type: AlSi
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: Silane, 3% Phosphorous
Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
2.0 x 105A/cm2

TRANSISTOR COUNT: 1896

PROCESS: CMOS; SAJI

Metallization Mask Layout

HC-55564/883