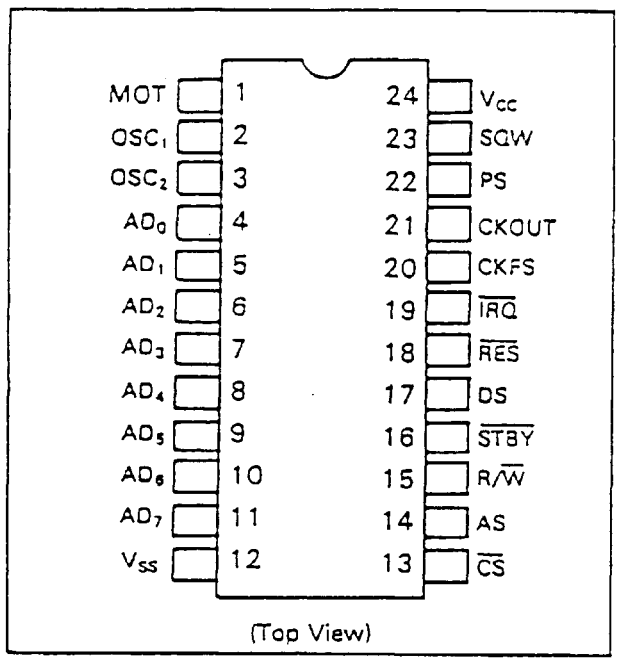
HD146818A (RTC) 403-969
(Real Time Clock Plus RAM)

The HD146818A RTC is a HMCS6800 peripheral CMOS device which includes the unique MOTEL concept for use with various microprocessors, microcomputers, and large computers.
This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM.

This device includes HD6801, HD6301 multiplexed bus interface circuit and 8085's multiplexed bus interface as well.

The real time clock plus RAM has two distinct uses. First, it is designed as battey powered CMOS part including all the common battery backed-up functions such as RAM, time, and calender. Secondly, the HD146818A may be used with a CMOS microprocessor to relieve the software of timekeeping workload and to extend the available RAM of an MPU such as the HD6301.

Pin Arrangement



(Top View)

Features

- Time-of-day clock and calendar
  - Counts seconds, minutes, and hours of the day
  - Counts days of week, date, month, and year
- Binary or BCD representation of time, calendar, and alarm
- 12 or 24 hour clock with AM and PM in 12-hour mode
- Automatic end of month recognition
- Automatic leap year compensation
- Interfaced with software as 64 RAM locations
  - 14 Bytes of clock and control register
  - 50 Bytes of general purpose RAM
- Three interrupt are separately software maskable and testable
  - Time-of-day alarm, once-per-second to once-per-day
  - Periodic rates from 30.5 μs to 500 ms
  - End-of-clock update cycle
- Programmable square-wave output signal
- Three time base input options
  - 4.194304 MHz
  - 1.048576 MHz
  - 32.768 kHz
- Clock output may be used as microprocessor clock input
  - At time base frequency ÷ 4 or ÷ 1
- Multiplexed bus interface circuit of HD6801, HD6301 and 8085
- Low-power, high-speed, high-density CMOS
- Battery backed-up operation
- Selectable between 6801 family type and 8085 family type bus timing

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HITACHI

Farnell COMPONENTS

Pin Description

Table 1 shows the names and mnemonics for the pins of the RTC.

MOT (Motel)

The MOT pin offers flexibility when choosing bus type. When tied to V_{CC}, 6801 family type timing is used. When tied to V_{SS}, 8085 family type timing is used. The MOT pin must be hard-wired to the V_{CC} or V_{SS} supply and cannot be switched during operation of the HD146818A.

CKOUT (Clock Out)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in table 2.

CKFS (Clock Out Frequency Select)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. CKFS tied to V_{CC} causes CKOUT to be the same frequency as the time base at the OSC_1 pin. When CKFS is at V_{SS}, CKOUT is the OSC_1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.
Input signal, which is not necessary for user's application, should be used fixed to high or low level.

SQW (Square Wave)

The SQW pin can output a signal from one of 15 of the 22 internal-divider stages. The frequency and output enable of the SQW may be altered by programming register A, as shown in table 6. The SQW signal may be turned on and off using a bit in register B.

Table 1. Pin Description

Symbol	Pin No.	I/O*	Name
MOT	1	I	Motel
CKOUT	21	O	Clock out
CKFS	20	I	Clock out frequency Select
SQW	23	O	Square Wave
AD_0-AD_7	4-11	I/O	Multiplexed bidirectional address/data bus
AS	14	I	Multiplexed address strobe
DS	17	I	Data strobe or Read
R/$\overline{W}$	15	I	Read/Write
$\overline{CS}$	13	I	Chip select
$\overline{IRQ}$	19	O	Interrupt request
$\overline{STBY}$	16	I	Stand-by
$\overline{RES}$	18	I	Reset
PS	22	I	Power sence
V_{CC}	24		Power supply
V_{SS}	12		Ground
OSC_1 OSC_2	2 3	I	Time base

* I: Input O: Output I/O: Input/Output

AD_0-AD_7 (Multiplexed Bidirectional Address/Data Bus)

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the HD146818A since the bus reversal from address to data is occurring during the internal RAM access time.
The address must be valid just prior to the fall of AS/ALE at which time the HD146818A latches the address from AD_0 to AD_5. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle, the HD146818A outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in the HD6801, HD6301 case or $\overline{RD}$ rises in the other case.

AS (Multiplexed Address Strobe)

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the HD146818A.

DS (Data Strobe or Read)

The DS pin has two interpretation via the MOTEL circuit. When emanating from 6801 family type processor,
DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and ϕ_2 (ϕ_2 clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.
The second interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from the 8085 type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

R/$\overline{W}$ (Read/Write)

The MOTEL circuit treats the R/$\overline{W}$ pin in one of two ways. When 6801 family type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, whereas a write cycle is a low on R/$\overline{W}$ during DS.
The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from 8085 family type processors. The MOTEL circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMs.

$\overline{CS}$ (Chip Select)

The chip-select ($\overline{CS}$) signal must be asserted for a bus cycle in which the HD146818A is to be accessed. Bus cycles which take place without asserting $\overline{CS}$ cause no actions to take place within the HD146818A. When $\overline{CS}$ is not used, it should be grounded.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an active low output of the HD146818A that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads register C. The $\overline{RES}$ pin also clears pending interrupts.
When no interrupt conditions are present, the

Table 2. Clock Output Frequencies

Time Base (OSC_1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304 MHz	High	4.194304 MHz
4.194304 MHz	Low	1.048576 MHz
1.048576 MHz	High	1.048576 MHz
1.048576 MHz	Low	262.144 kHz
32.768 kHz	High	32.768 kHz
32.768 kHz	Low	8.192 kHz

$\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor.

$\overline{RES}$ (Reset)

The $\overline{RES}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{RES}$ pin must be held low for the specified time, t_{RLH}, in order to allow the power supply to stabilize, figure 2 shows a typical representation of the $\overline{RES}$ pin circuit.
When $\overline{RES}$ is low the following occurs:

a) Periodic Interrupt Enable (PIE) bit is cleared to "0".
b) Alarm Interrupt Enable (AIE) bit is cleared to "0".
c) Update ended Interrupt Enable (UIE) bit is cleared to "0".
d) Update ended Interrupt Flag (UF) bit is cleared to "0".
e) Interrupt Request status Flag (IRQF) bit is cleared to "0".
f) Periodic Interrupt Flag (PF) bit is cleared to "0".
g) Alarm Interrupt Flag (AF) bit in cleared to "0".
h) $\overline{IRQ}$ pin is in high-impedance state. and
i) Square Wave output Enable (SQWE) bit is cleared to "0".

PS (Power Sense)

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in register D. When the PS pin is low the VRT bit is cleared to "0".
During powerup, the PS pin must be externally held low for the specified time, t_{PLH}. As power is applied the VRT bit remain low indicating that the contents of the RAM, time registers, and calendar are not guaranteed. When normal operation commences PS should be permitted to go high. Output signal from external power sence circuit will be connected to this input.
Input signal, which is not necessary for user's application, should be used fixed to high or low level.

V_{CC}, V_{SS} (Power Supply, Ground)

DC power is provided to the part on these two pins, V_{CC} being the most positive voltage. The minimum and maximum voltages are listed in the electrical characteristics tables.

OSC_1 , OSC_2 (Time Base)

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 KHz may be connected to OSC_1 as shown in figure 1. The time-base frequency to be used is chosen in register A.
The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in figure 11.

$\overline{STBY}$ (Stand-by)

The $\overline{STBY}$ pin, when active, prevents access to the HD146818A making it ideal for battery back-up applications. Stand-by operation incorporates a transparent latch. After data strobe (DS) goes low ($\overline{RD}$ or $\overline{WR}$ rises), $\overline{STBY}$ is recognized as a valid signal.
The $\overline{STBY}$ signal is totally asynchronous. Its transparent latch is opened by the falling edge of DS (rising edge of $\overline{RD}$ or $\overline{WR}$) and clocked by the rising edge of AS (ALE). Therefore, for $\overline{STBY}$ to be recognized, DS and AS shold occur in pairs. When $\overline{STBY}$ goes low before the falling edge of DS (rising edge of $\overline{WR}$ or $\overline{RD}$), the current cycle is completed at that edge and the next cycle will not be executed.

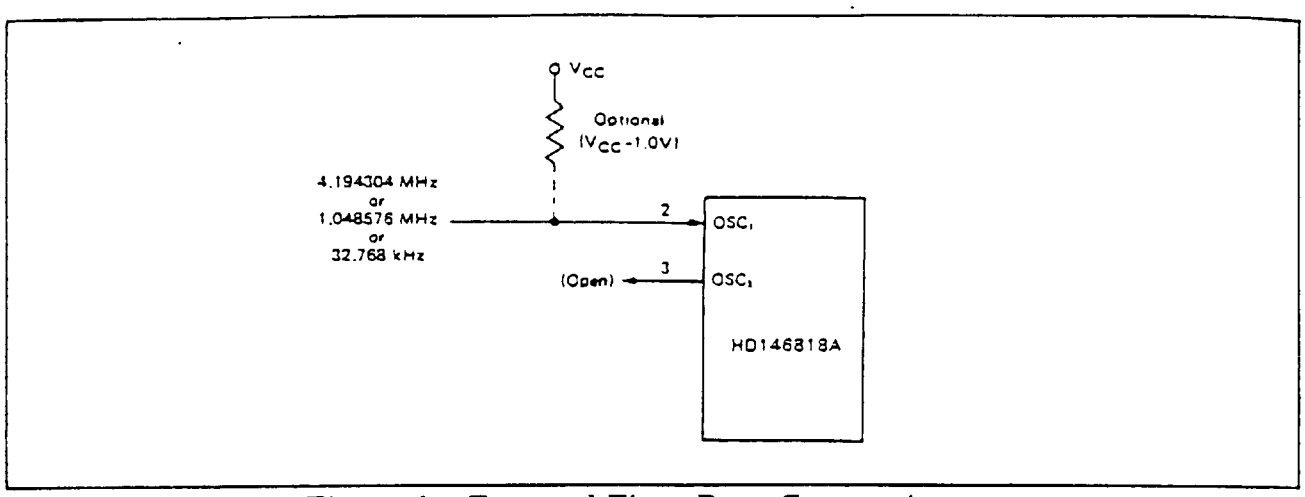


Figure 1. External Time-Base Connection

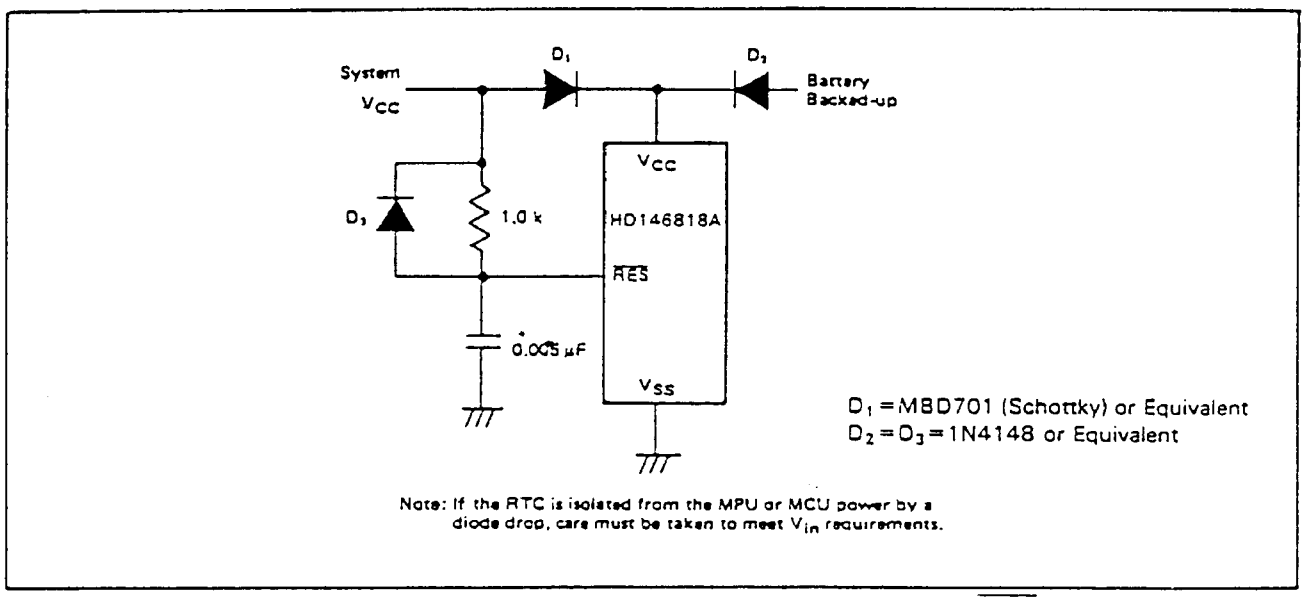


Figure 2. Typical Powerup Delay Circuit for $\overline{RES}$

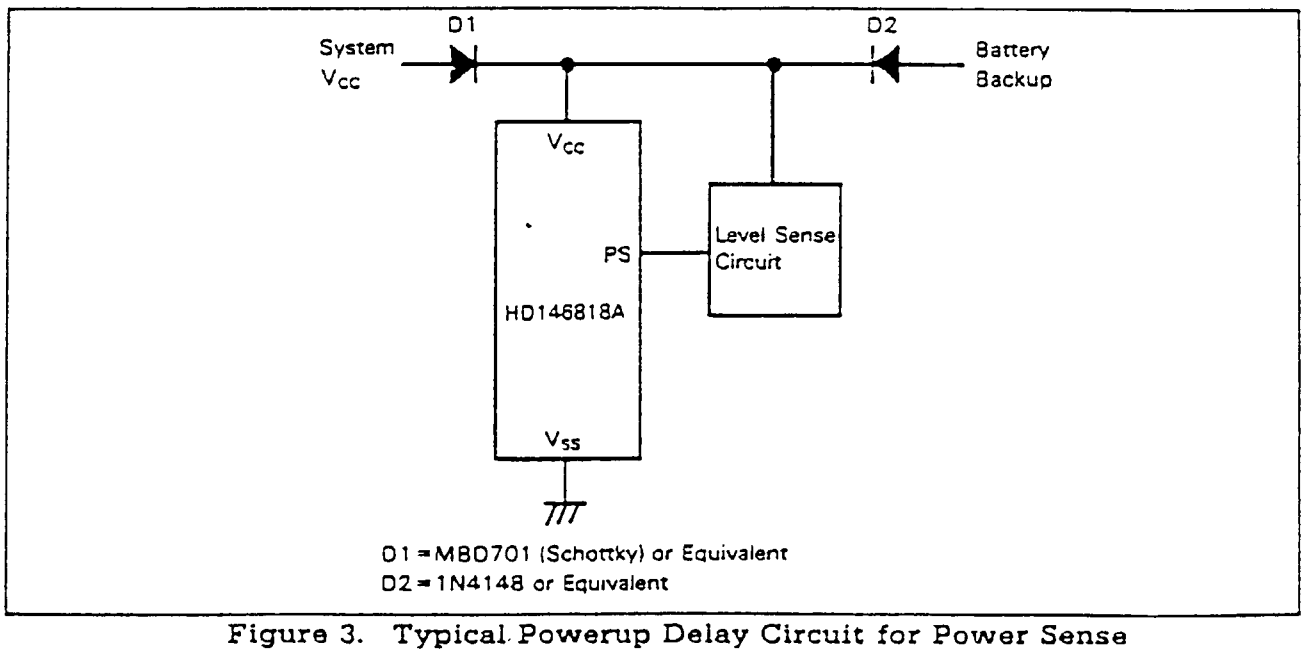


Figure 3. Typical Powerup Delay Circuit for Power Sense

Block Diagram

The block diagram in figure 4, shows the pin connection with the major internal function of the RTC.

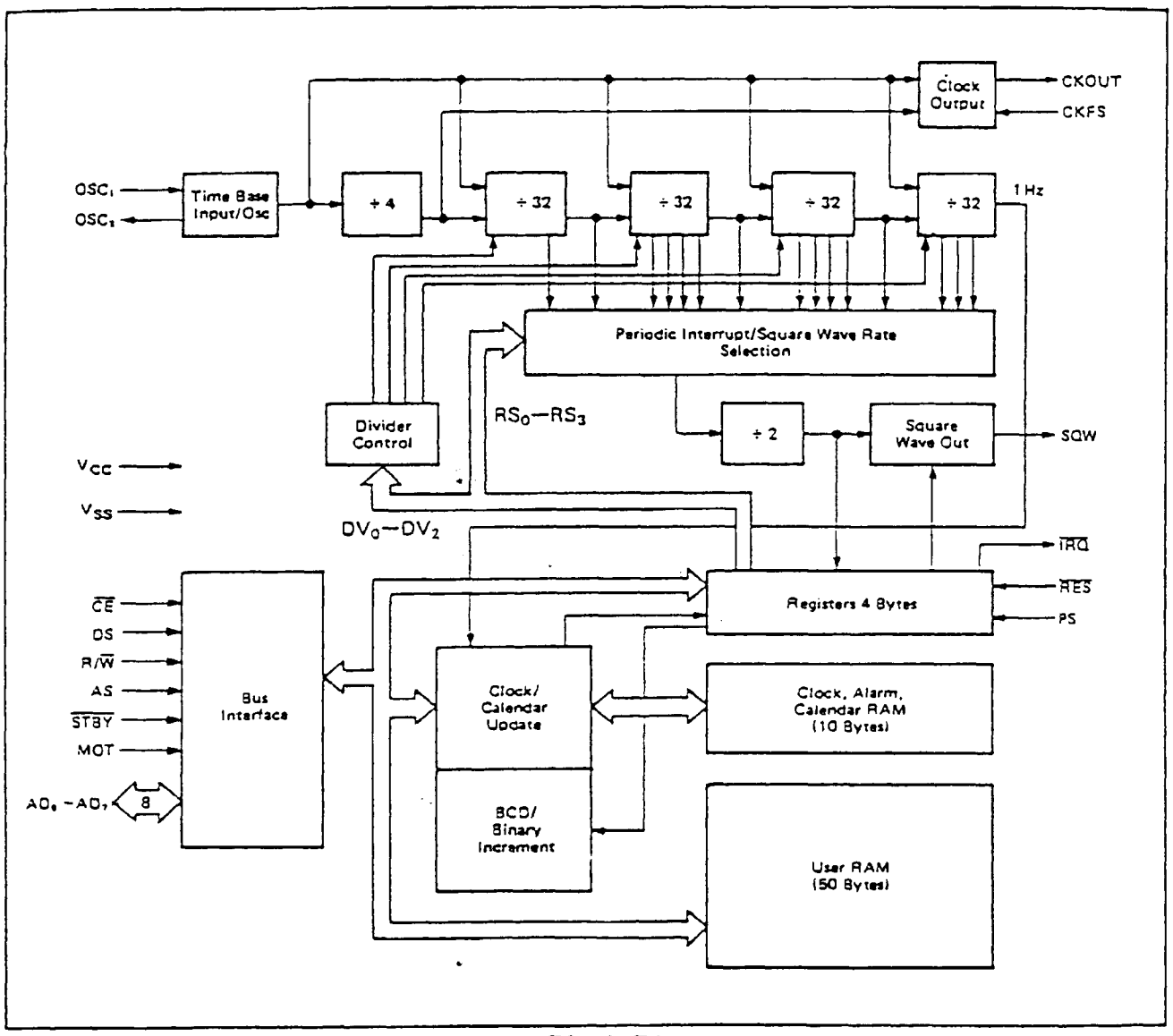


Figure 4. Block Diagram

Registers

The HD146818A has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Register A (S0A)

Figure 5 shows register A.

UIP: The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 μs (for all time bases). This is detailed in table 3. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero—it is not in transition. The UIP bit is a read-only bit, and is not affected by reset. Writing the SET bit in register B to a "1" inhibit any update cycle and then clear the UIP status bit.

DV2, DV1, DV0: Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 5 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins half a second later. These three read/write bits are never modified by the RTC and are not affected by $\overline{RES}$.

RS3, RS2, RS1, RS0: The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 6 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by $\overline{RES}$ and are never changed by the RTC.

Table 3. Update Cycle Times

UIP Bit	Time Base (OSC_1)	Update Cycle Time (t_{UC})	Minimum Time Before Update Cycle (t_{AUC})
1	4.194304 MHz	248 μs	—
1	1.048576 MHz	248 μs	—
1	32.768 kHz	1984 μs	—
0	4.194304 MHz	—	244 μs
0	1.048576 MHz	—	244 μs
0	32.768 kHz	—	244 μs

Note: t_{UC} and t_{AUC} are shown in figure 10.

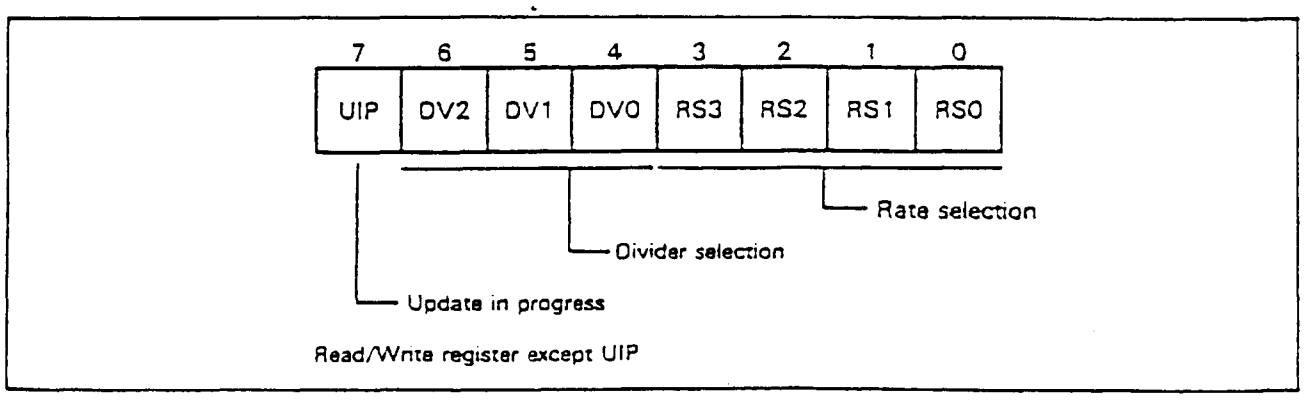


Figure 5. Register A

Register B (S0B)

Figure 6 shows register B.

SET: When the SET bit is a "0", the update cycle functions normally by abvancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by $\overline{RES}$ or internal functions of the HD146818A.

PIE: The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in register C to cause the $\overline{IRQ}$ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in control register A. A "0" in PIE blocks $\overline{IRQ}$ from being initiated by a periodic interrupt, but the periodic interrupt flag (PF) bit is still at the periodic rate. PIE is not modified by any internal HD146818A functions, but is cleared to "0" by a $\overline{RES}$.

AIE: The alarm interrupt enable (AIE) bit is read/write bit which when set so a "1" permits the alarm interrupt flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11 × × × × × ×). When the AIE bit is a "0", the AF bit does not initiate an $\overline{IRQ}$ signal. The $\overline{RES}$ pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE: The update-ended interrupt enable (UIE) bit is a read/write bit which enables the update-ended interrupt flag (UF) bit in register C to assert $\overline{IRQ}$. The $\overline{RES}$ pin going low clears the UIE bit.

SQWE: When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a "0" the SQW pin is held low . The state of SQWE is cleared by the $\overline{RES}$ pin. SQWE is a read/write bit.

DM: The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{RES}$. A "1" in DM signifies binary data, while a "0" in DM specified binary-coded-decimal (BCD) data.

24/12: The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by software.

DSE: The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

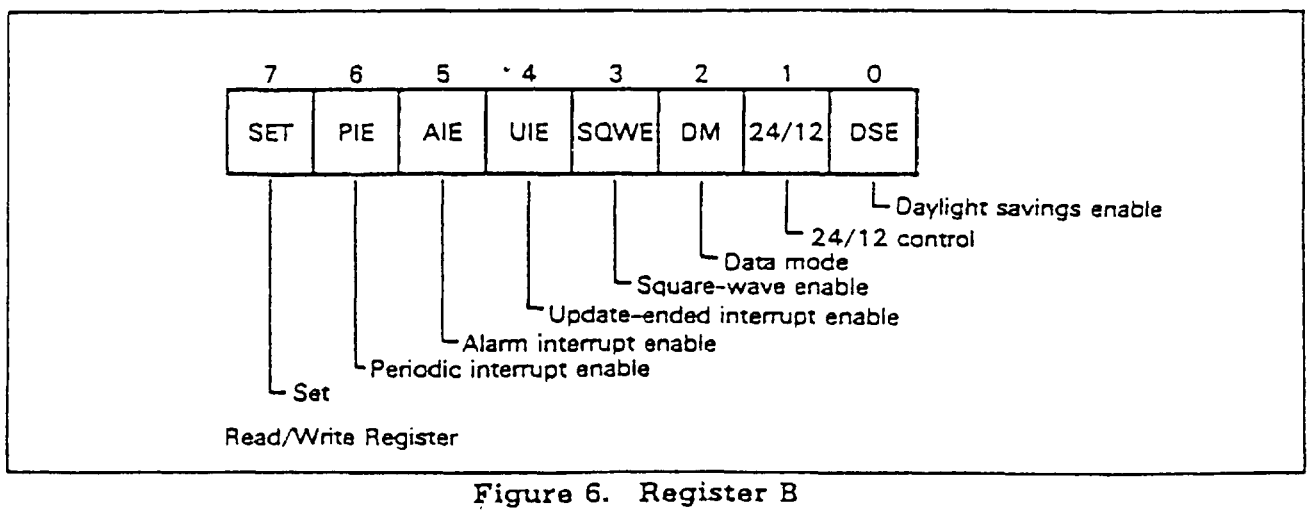


Figure 6. Register B

Register C (S0C)

Figure 7 shows register C.

IRQF: The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:
PF = PIE = "1"
AF = AIE = "1"
UF = UIE = "1"
i.e., IRQF = PF·PIE + AF·AIE + UF·UIE

Any time are IRQF bit is a "1", the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after register C is read by the program or when the $\overline{RES}$ pin is low. A program write to Register C does not modify any of the flag bits.

PF: The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{IRQ}$ signal and the IRQF bit when PIE is also a "1". The PF bit is cleared by a $\overline{RES}$ or a software read of register C.

AF: A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{IRQ}$ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A $\overline{RES}$ or a read of register C clears AF.

UF: The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{IRQ}$. UF is cleared by a register C read or a $\overline{RES}$.

b3 to b0: The unused bits of Status Register C are read as "0's". They can not be written.

Register D (S0D)

Figure 8 shows register D.

VRT: The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the $\overline{RES}$ pin. The VRT bit can only be set by reading the register D. For setting this bit, PS signal needs to be high level.

b6 to b0: The remaining bits of register D are unused. They cannot be written, but are always read as "0's".

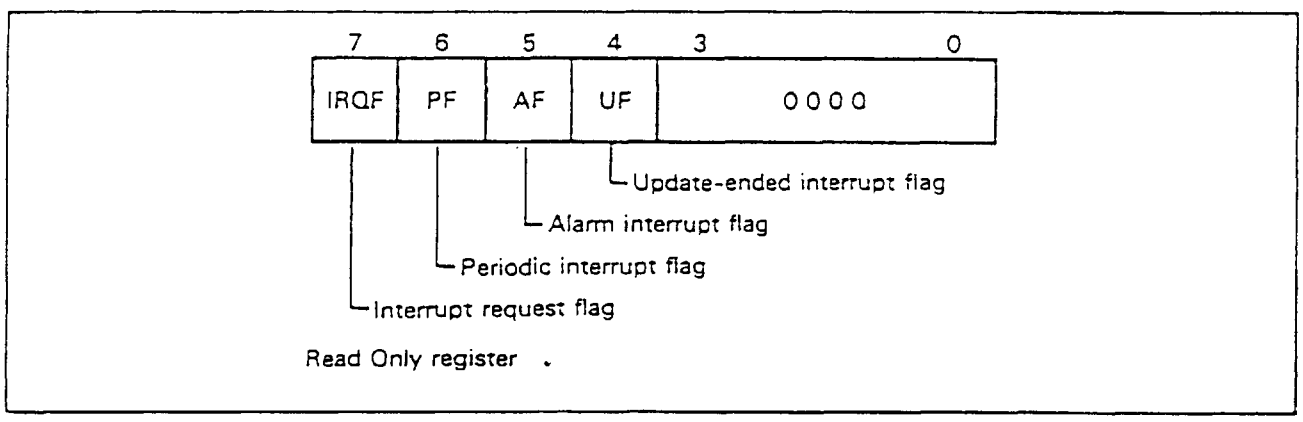


Figure 7. Register C

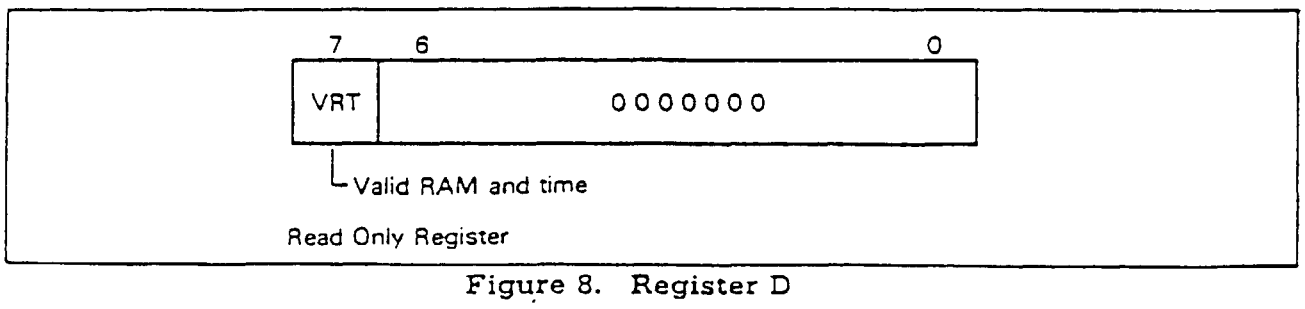


Figure 8. Register D

Address Map

Figure 9 shows the address map of the HD146818A. The memory consists of 50 general purpose RAM bytes. 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except register C and D which are read only. Bit 7 of register A and the seconds byte are also read only. Bit 7 of the seconds byte, always reads "0". The contents of the four control and status registers are described in the register section.

Time, Calendar, and Alarm Locations

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in register B should be set to a "1" to prevent time calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

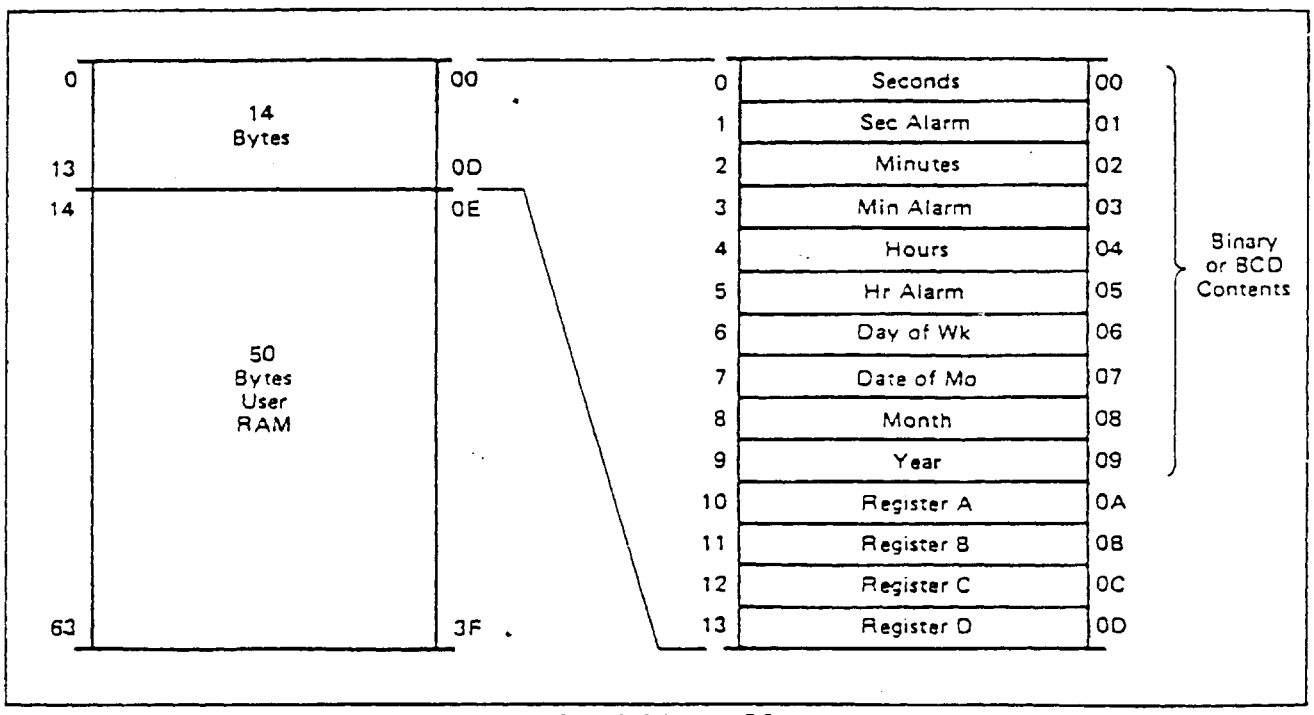


Figure 9. Address Map

Table 4 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessable by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 μs at the 4.194304 MHz and 1.048576 MHz time bases and 1984 μs for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is "1". The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two mostsignificant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Static CMOS RAM

The 50 general purpose RAM bytes are dedicated within the HD146818A. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional HD146818As may be included in the system. The time/calendar functions may be disable by holding the dividers, in register A, in the reset state by setting the SET bit in register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. Bit 7 of register A, register C and D, and the high-order bit of the seconds byte cannot effectively be used as general purpose RAM.

Table 4. Time, Calendar, and Alarm Data Modes

Address Location	Function	Decimal Range	Range		Example*	
			Binary Date Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0—59	$00~$38	$00~$59	$15	$21
1	Seconds Alarm	0—59	$00~$38	$00~$59	$15	$21
2	Minutes	0—59	$00~$38	$00~$59	$3A	$58
3	Minutes Alarm	0—59	$00~$38	$00~$59	$3A	$58
4	Hours (12 Hour Mode)	1—12	$01~$0C (AM) and $81~$8C (PM)	$01~$12 (AM) and $81~$92 (PM)	$05	$05
	Hours (24 Hour Mode)	0—23	$00~$17	$00~$23	$05	$05
5	Hours Alarm (12 Hour Mode)	1—12	$01~$0C (AM) and $81~$8C (PM)	$01~$12 (AM) and $81~$92 (PM)	$05	$05
	Hours Alarm (24 Hour Mode)	0—23	$00~$17	$00~$23	$05	$05
6	Day of the Week Sunday = 1	1—7	$01~$07	$01~$07	$05	$05
7	Day of the Month	1—31	$01~$1F	$01~$31	$0F	$15
8	Month	1—12	$01~$0C	$01~$12	$02	$02
9	Year	0—99**	$00~$63	$00~$99	$4F	$79

* Example: 5:58:21 Thursday 15th February 1979 (time is AM)

** Set the lower two digits of year in AD. If this number is multiple of 4, update applied to leap year is excuted. Note that update applied to leap year is executed when the number is "00".

Interrupts

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 μs. The update-ended interrupt may be used to indicate to the program that an up-date cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in register B enable the three interrupts. Writing a "1" to a interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{IRQ}$ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a "1" in register C. Each of the three interrupt sources have separate flag bits in register C, which are set independent of the state of the corresponding enable bits in register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read. However, there is one precaution. The flag bits in register C are cleared (record of the interrupt event is erased) when register C is read. Double latching is included with register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held after the read cycle. One, two, or three flag bits may be found to be set when register C is read. The program should inspect all utilized flag bits every time register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in register C is a "1" whenever the $\overline{IRQ}$ pin is being driven low.

The processor program can determine that the RTC initiated the interrupt by reading register C. A "1" in bit 7 (IRQF bit) indicates that one of more interrupts have been initiated by the part. The act of reading register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

Divider Stages

The HD146818A has 22 binary-divider stages following the time base as shown in figure 3. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three divider bus (DV2, DV1, and DV0) in register A.

Divider Control

The divider-control bits have three uses, as shown in table 5. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz). The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider-control bits are also used to facilitate testing the HD146818A.

Table 5. Divider Configurations

Time-Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4.194304 MHz	0	0	0	Yes	—	N = 0
1.048576 MHz	0	0	1	Yes	—	N = 2
32.768 kHz	0	1	0	Yes	—	N = 7
Any	1	1	0	No	Yes	—
Any	1	1	1	No	Yes	—

Note: Other combinations of divider bits are used for test purposes only.

Square-Wave Output Selection

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in figure 3. The first purpose of selecting a divider tap is to generate a square-wave output signal in the SQW pin. Four bits in register A establish the square-wave frequency as listed in table 6. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.
Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in register B. Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

Periodic Interrupt Selection

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500 ms to once every 30.517 μs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Table 6 shows that the periodic interrupt rate is selected with the same register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit in register B. Similarly the periodic interrupt is enabled by the PIE bit in register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of input from contact closures to serial receive bits or bytes. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 6. Periodic Interrupt Rate and Square Wave Output Frequency

Rate Select Control register 1				4.194304 or 1.048576 MHz Time Base		32.768 kHz Time Base	
RS3	RS2	RS1	RS0	Periodic Interrut Rate t_{PI}	SQW Output Frequency	Periodic Interrupt Rate t_{PI}	SQW Output Frequency
0	0	0	0	None	None*	None	None*
0	0	0	1	30.517 μs	32.768 kHz	3.90625 ms	256 Hz
0	0	1	0	61.035 μs	16.384 kHz	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8.192 kHz	122.070 μs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz	244.141 μs	4.096 kHz
0	1	0	1	488.281 μs	2.048 kHz	488.281 μs	2.048 kHz
0	1	1	0	976.562 μs	1.024 kHz	976.562 μs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz	500 ms	2 Hz

* Fix the output "high" if SQWE = "1"

Initialization of the Time and the Start Sequence.

The first update of the time occurs about 500 ms later after the SET bit of control register B is reset. So keep followings in mind when initializing and adjusting the time.
Procedure of time initialization

(1) Set the SET bit of control register B. (SET = "1")
(2) Set "1" into all the DV1, 2 bits of control register A.
(DV1 = DV2 = "1")
(3) Set the time and calendar to each RAM.
(4) Set the frequency in use into DV0, 1 and DV2.
(5) Reset the SET bit. (SET = "0")

Restriction on Time-of-day and Calendar Initialization

These are cases in HD146818A (RTC) that update is not executed correctly if time of day and calendar shown below are initialized. Therefore, initialize the RTC without using time of day shows table 7.

Table 7. Restricted Time and Date Set-up

Calendar, Time of day & Status after Update	Examples
If 29 th 23:59:59 in all the months is initialized, update to 1st in the next month is excuted. (Jan. — Dec. However except for Feb. 29th in leap year)	Mar.29th →Apr. 1st
If 30th 23:59:59 in Apr., June, Sept., and Nov. is initialized, update to 31st in each month is executed.	Apr. 30th →Apr. 31st
If Feb. 28th 23:59:59 (not in leap year) is initialized, update to Feb. 29th is executed.	Feb. 28th, 1989 →Feb. 29th, 1989
If Feb. 28th 23:59:58 (in leap year) is initialized, update to Mar. 1st is executed.	Feb. 28th, 1988 →Mar. 1st, 1988

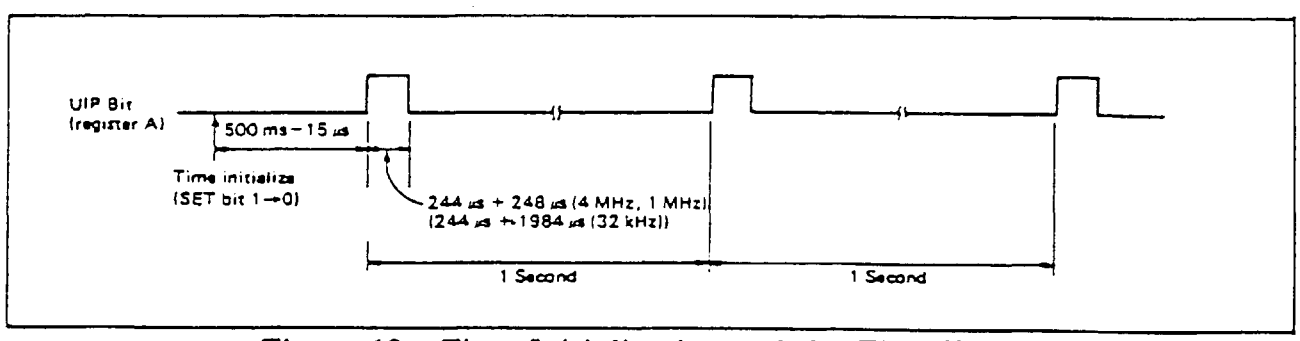


Figure 10. Time Initialization and the First Update

Update Cycle

The HD146818A executes an update cycle once-per-second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in register B is clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11 × × × × × ×) is present in all three positions.

With a 4.194304 MHz or 1.048576 MHz time base the update cycle takes 248 μs while a 32.768 kHz time base update cycle takes 1984 μs. During the update cycle, the time, calendar, and alarm bytes are not accessable by the processor program. The HD146818A protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be underfined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date imformation finds data unavailable statistically once every 4032 attempts. Three methods of accommodating nonavailability during update are usable by the program. In discussing the three methods it is assumed that at random points user-program are able to call a subroutine to obtain the time of day. The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transfered to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in register C should be cleared.

The second method uses the update-in-progress bit (UIP) in register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 μs later. Therefore, if a "0" is read on the UIP bit, the user has at least 244 μs before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time calendar data to exceed 244 μs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in register A is set high between the setting of the PF bit in register C (see figure 11). Periodic interrupts that occur at a rate of greater than $t_{BUC} + t_{UC}$ allow valid time and data information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(t_{PI} \div 2) - t_{BUC}$ to insure that data is not read during the update cycle.

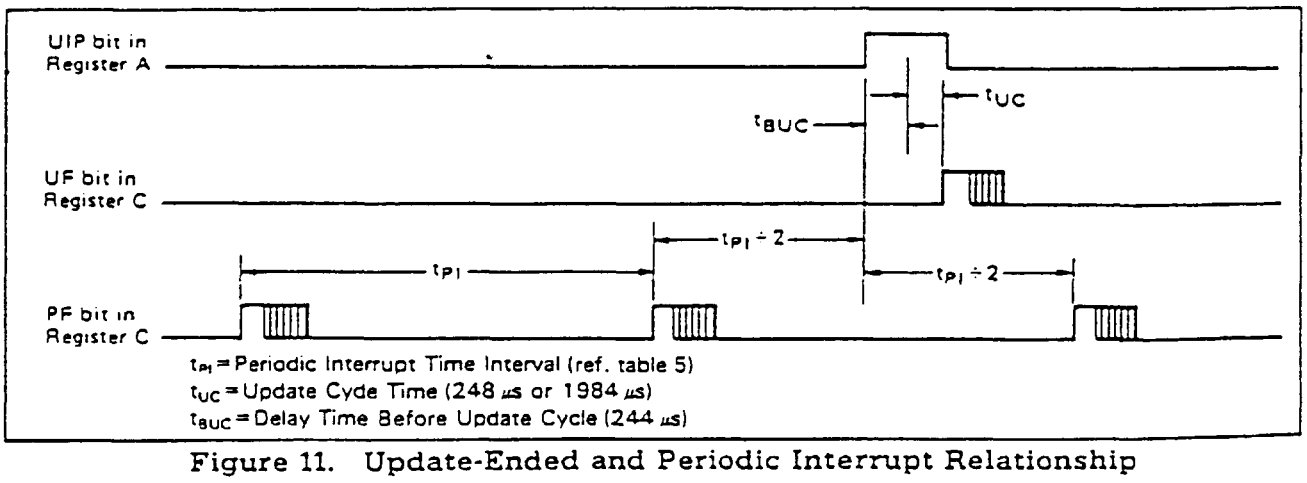


Figure 11. Update-Ended and Periodic Interrupt Relationship

Power-down Considerations

In most systems, the HD146818A must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability according to the specification described in the section regarding battery backed-up operation.

The stand-by ($\overline{STBY}$) pin controls bus inputs (AD_0-AD_7). $\overline{STBY}$, when asserted, disallows any unintended modification of the RTC data by the bus. $\overline{STBY}$ also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the square wave (SQW) pin.

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

Crystal Oscillation Circuit

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in figure 11.

Note For Board Design of The Oscillation Circuit

In designing the board, the following notes should be taken when the crystal oscillator is used.

(1) Crystal oscillator, load capacity C_{in}, C_{out} and R_f, R must be placed near the LSI as much as possible.
Normal oscillation may be disturbed when external noise is induced to pin 2 and 3.

(2) Pin 3 signal line should be wired apart from pin 4 signal line as much as possible. Don't wire them in parallel, or normal oscillation may be disturbed when this signal is feedbacked to OSC_1. (see figure 13)

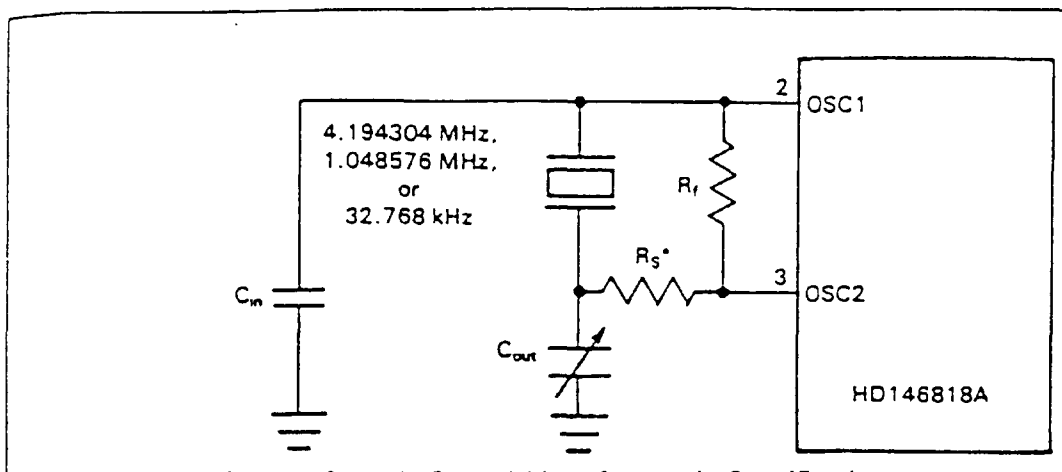
(3) A signal line or a power source line must not cross or go near the oscillation circuit line as shown in figure 14 to prevent the induction from these lines and perform the correct oscillation. The resistance among OSC_1, OSC_2 and other pins should be over 10 MΩ.

Table 8. Oscillator Circuit Parameters

	f_{osc}		
Parameter	**4.194304 MHz**	**1.048576 MHz**	**32.768 kHz**
R_S	—	—	390 kΩ
R_f	22 MΩ	22 MΩ	22 MΩ
C_{in}	15 pF	100 pF	22 pF
C_{out}	15 pF	68 pF	22 pF
CI*	80 Ω (max)	700 Ω (max)	40 kΩ (max)

* : Crystal Impedance

Note: 1. R_S are used for 32.768 kHz only.
2. Capacitance (C_{out}) should be adjusted to accurate frequency.



*32.768 kHz Only — Consult Crystal Manufacturer's Specification

Figure 12. Crystal Oscillator Connection

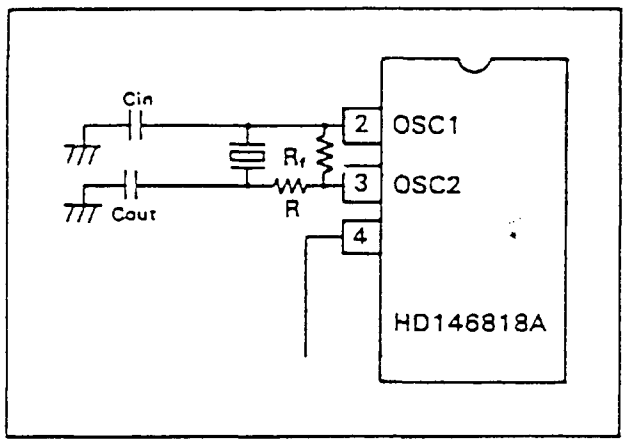


Figure 13. Note for Board Design of the Oscillation Circuit (1)

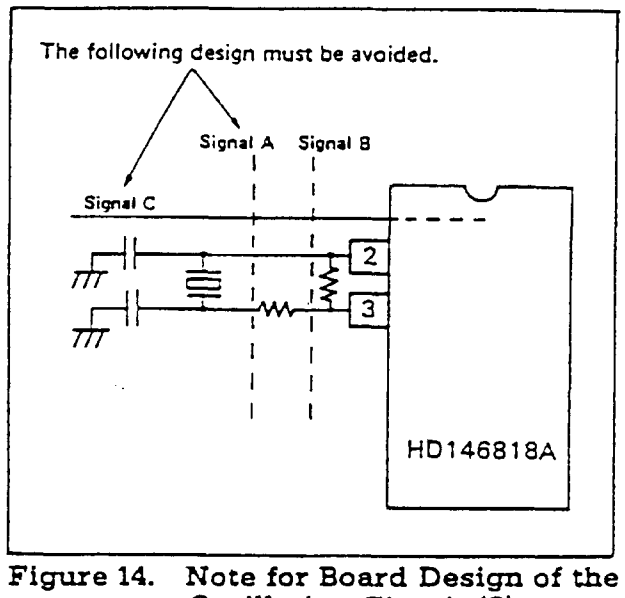


Figure 14. Note for Board Design of the Oscillation Circuit (2)

Battery Backup Operation

Battery Backup operation is one of the main feature of RTC. When RTC change to this mode, in order to retain the data of the internal RAM and register, following procedure should be used.

1) Change the supply from system V_{CC} to Battery Backup.
2) $\overline{STBY}$ input goes low after a detection of V_{CC} supply voltage down.
3) $\overline{STBY}$ should be latched before V_{CC} supply voltage becomes less than 4.5 V. (RTC needs one pair of AS, DS signals to latch the $\overline{STBY}$)

Figure 15 shows these flows.

Power reducing description

The standby ($\overline{STBY}$) pin controls bus inputs AD_0-AD_7 and $\overline{CS}$. An inner $\overline{STBY}$ signal latched after AS and DS signals gates these bus inputs, when negated, RTC reduces the power consumption by reducing the number of transitions seen internally. Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin.

The R/$\overline{W}$, DS, AS and $\overline{CS}$ inputs are not gated directly. Therefore these pins should be fixed to high or low voltage in the battery backup operation.

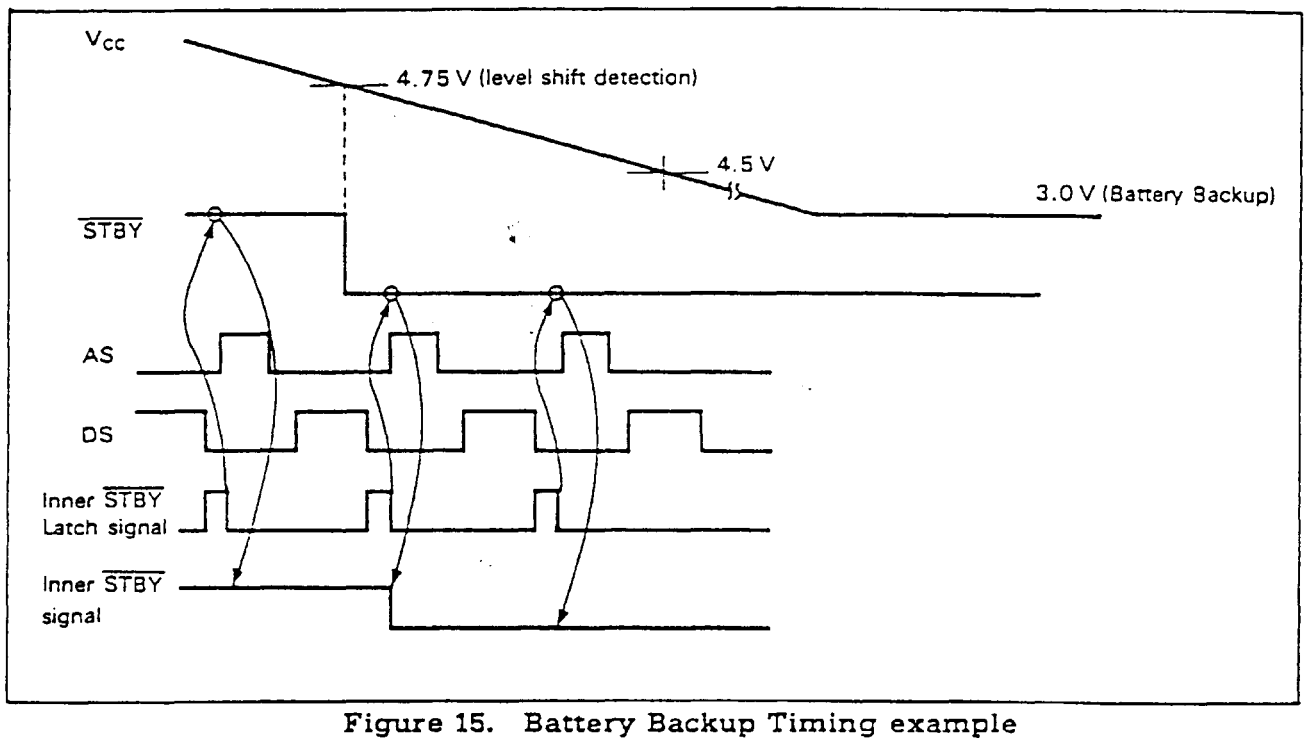


Figure 15. Battery Backup Timing example

CPU Interface Examples

The HD146818A is suited for use with microprocessors which generate an address-then-data multiplexed bus. figure 15 and 16 shows CPU interface examples to bus-compatible processors.
An example using either the 6800, 6802, or 6809 microprocessor is shown in figure 17. In this case, the AS and DS inputs should be left in a low state when the part is not being accessed.
$\overline{STBY}$ must be recognized by a dummy read or a dummy write before the HD146818A is accessed in order to latch the $\overline{STBY}$ input.
A program example for the non-multiplexed system is shown in the followings.

- Accumulator A: The address of the RTC to be accessed. ($00~$3F).
- Accumulator B:
  - — Write: The data to be written.
  - — Read: The data read from the RTC.

```
Read operation;  LDAA  =$00—=$3F  ; Set the address to be accessed.
                 STAA  RTC        ; Generate AS and latch data from ACCA.
                 LDAB  RTC+1      ; Generate DS and get data.
Write operation; LDAA  =$00—=$3F  ; Set the address to be accessed.
                 LDAB  WDATA      ; Set the data to be write.
                 STAA  RTC        ; Generate AS and latch data from ACCA.
                 STAB  RTC+1      ; Generate DS and strobe data.
```

The RTC is mapped to two consecutive memory locations. (RTC and RTC+1)

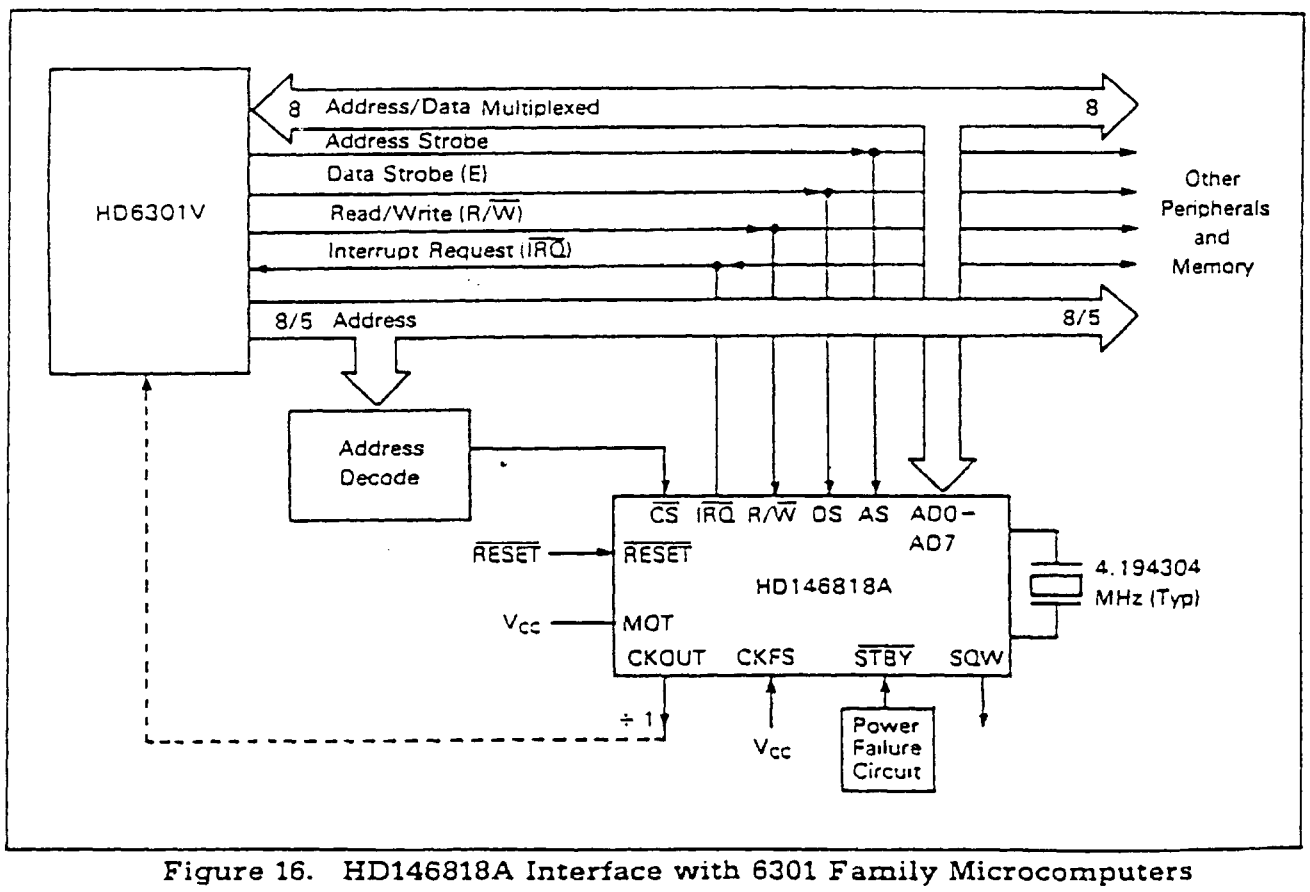


Figure 16. HD146818A Interface with 6301 Family Microcomputers

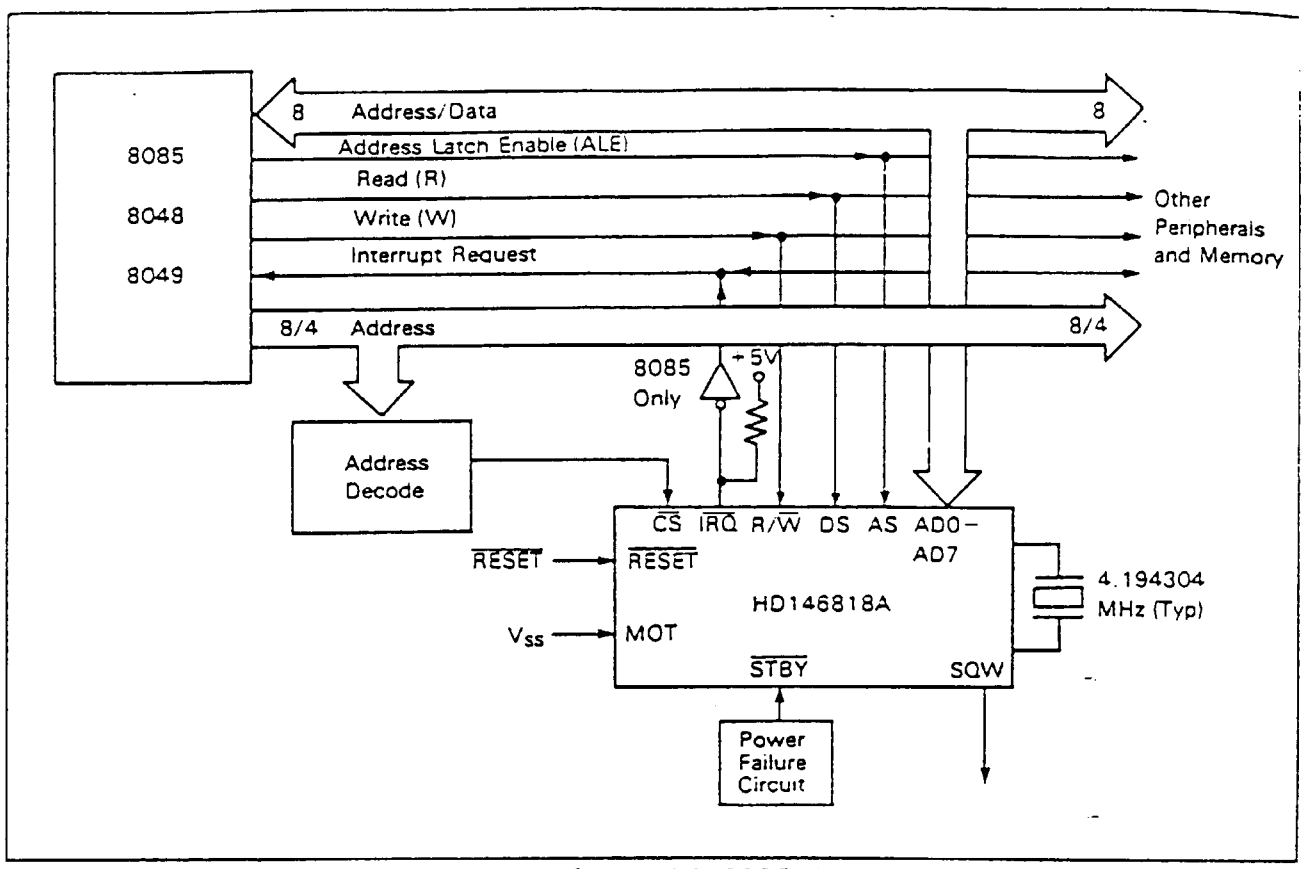


Figure 17. HD146818A Interface with 8085 Family Microprocessors

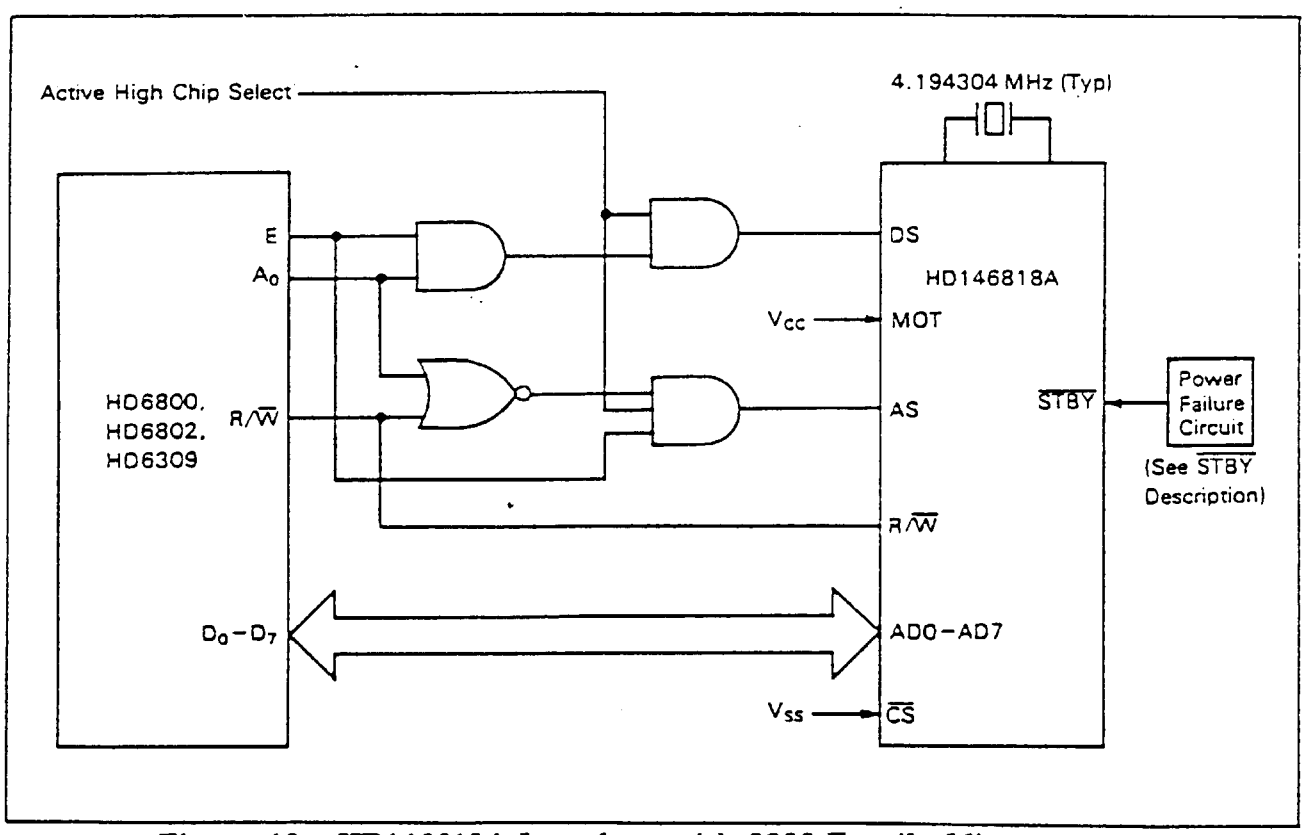


Figure 18. HD146818A Interface with 6800 Family Microprocessors

Absolute maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}*	− 0.3 — + 7.0	V
All Input Voltage Except OSC1	V_{in}*	V_{SS} − 0.3 — V_{CC} + 0.3	V
Maximum Output Current	$\|I_O\|$**	8	mA
Operating Temperature	T_{opr}	0 — + 70	°C
Storage Temperature	T_{stg}	− 55 — + 150	°C

* With respect to V_{SS} (System GND)

** Maximum output current is the maximum current which can flow in or flow out from one output terminal and I/O common terminal.

Note: Permanent LSI damage may occur if maximum rating are exceeded. Normal operation should be under recomended operating condition. If these conditions are exceeded, it could affect reliability of LSI.

Recomended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}*	4.5	5.0	5.5	V
Input High Voltage	$\overline{STBY}$, CKFS, AD_0~AD_7, DS AS, R/$\overline{W}$, $\overline{CS}$, PS	V_{IH}*	V_{CC}−2.0	—	V_{CC}	V
	$\overline{RES}$		V_{CC}−0.8	—	V_{CC}	
	OSC1		V_{CC}−1.0	—	V_{CC}	
	MOT		V_{CC}−0.2	—	V_{CC}	
Input Low Voltage	CKFS, PS, $\overline{RES}$, $\overline{STBY}$, DS, AS AD_0~AD_7, R/$\overline{W}$, $\overline{CS}$, OSC1	V_{IL}*	V_{SS}	—	0.8	V
	MOT		V_{SS}	—	0.4	
Operating Temperature		T_{opr}	0	25	70	°C

* With respect to V_{SS} (System GND)

Electrical Characteristics

DC Electrical Characteristics (V_{CC} = 3 V, V_{SS} = 0 V, T_A = 0°C to +70°C unless otherwise noted)

Item		Symbol	min	max	Test Condition	Unit
Frequency of Operation		f_{OSC}	32.768	32.768		kHz
Input High Voltage	$\overline{STBY}$, AD_0—AD_7, DS, AS, R/$\overline{W}$, $\overline{CS}$	V_{IH}	2.1	V_{CC}		V
	$\overline{RES}$, CKFS, PS, OSC1		2.5	V_{CC}		
	MOT		$V_{CC}-0.2$	V_{CC}		
Input Low Voltage	$\overline{STBY}$, AI_0—AD_7, DS, AS, R/$\overline{W}$, $\overline{CS}$, CKFS, PS, $\overline{RES}$, OSC1	V_{IL}	$V_{SS}-0.3$	0.5		V
	MOT		$V_{SS}-0.3$	0.2		
Input Current	AS, DS, R, $\overline{W}$	I_{in}	—	± 10		μA
	MOT, OSC1, $\overline{CS}$, $\overline{RES}$ $\overline{STBY}$, CKFS, PS		—	± 1		
Three-State Leakage	$\overline{IRQ}$, AD_0—AD_7	I_{TSL}	—	± 10		μA
Output High Voltage	All Outputs	V_{OH}	$V_{CC}-0.1$	—	I_{LOAD} < 10 μA	V
			$V_{CC}-0.3$	—	I_{LOAD} = − 0.25 mA	
Output Low Voltage	All Outputs	V_{OL}	—	0.1	I_{LOAD} < 10 μA	V
			—	0.3	I_{LOAD} = 0.25 mA	
I_{CC} – Bus Idle *		I_{CC3}	—	100	CKOUT = f_{OSC}, CL = 15pF SQW Disabled, $\overline{STBY}$ = 0.2V CL(OSC2) = 10pF, f_{OSC} = 32.768kHz	μA
I_{CC} – Quiescent		I_{CC4}	—	80	f_{OSC} = DC, OSC = DC, All Other inputs = V_{CC} −0.2V No clock	μA

* V_{IH} min = V_{CC} − 0.2V, V_{IL} max = V_{SS} + 0.2V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0°C to +70°C unless otherwise noted)

Item		Symbol	min	max	Test Condition	Unit
Frequency of Operation		f_{OSC}	32.768	4194.304		kHz
Inout High Voltage	$\overline{STBY}$, CKFS, AD_0—AD_7, DS, AS, R/$\overline{W}$, $\overline{CS}$, PS	V_{IH}	$V_{CC}-2.0$	V_{CC}		V
	$\overline{RES}$		$V_{CC}-0.8$	V_{CC}		
	OSC1		$V_{CC}-1.0$	V_{CC}		
	MOT		$V_{CC}-0.8$	V_{CC}		
Input Low Voltage	CKFS, PS, $\overline{RES}$, $\overline{STBY}$, AD_0—AD_7 DS, AS, R/$\overline{W}$, $\overline{CS}$, OSC1	V_{IL}	$V_{SS}-0.3$	0.8		V
	MOT		$V_{SS}-0.3$	0.4		
Input Current	AS, DS, R/$\overline{W}$	I_{in}	—	± 10		μA
	MOT, OSC1, $\overline{CS}$, $\overline{STBY}$, $\overline{RES}$, CKFS, PS		—	± 1		
Three-State Leakage	$\overline{IRQ}$, AD_0—AD_7	I_{TSL}	—	± 10		μA
Output High Voltage	All Outputs	V_{OH}	$V_{CC}-0.1$	—	I_{LOAD} < 10 μA	V
	AD_0—AD_7, CKOUT		4.1	—	I_{LOAD} = − 1.6 mA	
	SQW				I_{LOAD} = − 1.0 mA	
Output Low Voltage	All Outputs	V_{OL}	—	0.1	I_{LOAD} < 10 μA	V
	AD_0—AD_7, CKOUT		—	0.4	I_{LOAD} = 1.6 mA	
	$\overline{IRQ}$, SQW				I_{LOAD} = 1.0 mA	
I_{CC} — Bus Idle (External clock) *	f = 4.194304 MHz	I_{CC1}	—	4000	CKOut = f_{OSC}, C_L = 15 pF	μA
	f = 1.048576 MHz	I_{CC2}	—	1000	SQW Disabled. $\overline{STBY}$ = 0.2V	
	f = 32.768 kHz	I_{CC3}	—	100	C_L(OSC2) = 10pF	
I_{CC} — Quiescent		I_{CC4}	—	100	F_{OSC} = DC, OSC1 = DC All Other Inputs = $V_{CC}-0.2V$ No Clock	μA
Input Capacitance	AD_0—AD_7	C_{in}	—	12.5	V_{in} = 0 V Ta = 25 C f = 1MHz	pF
	All Other Input					
Output Capacitance	SQW, CKOUT, $\overline{IRQ}$	C_{out}	—	12.5	V_{in} = 0V, Ta = 25°C f = 1MHz	pF

* V_{IH} min = V_{CC} − 0.2V, V_{IL} max = V_{SS} + 0.2V

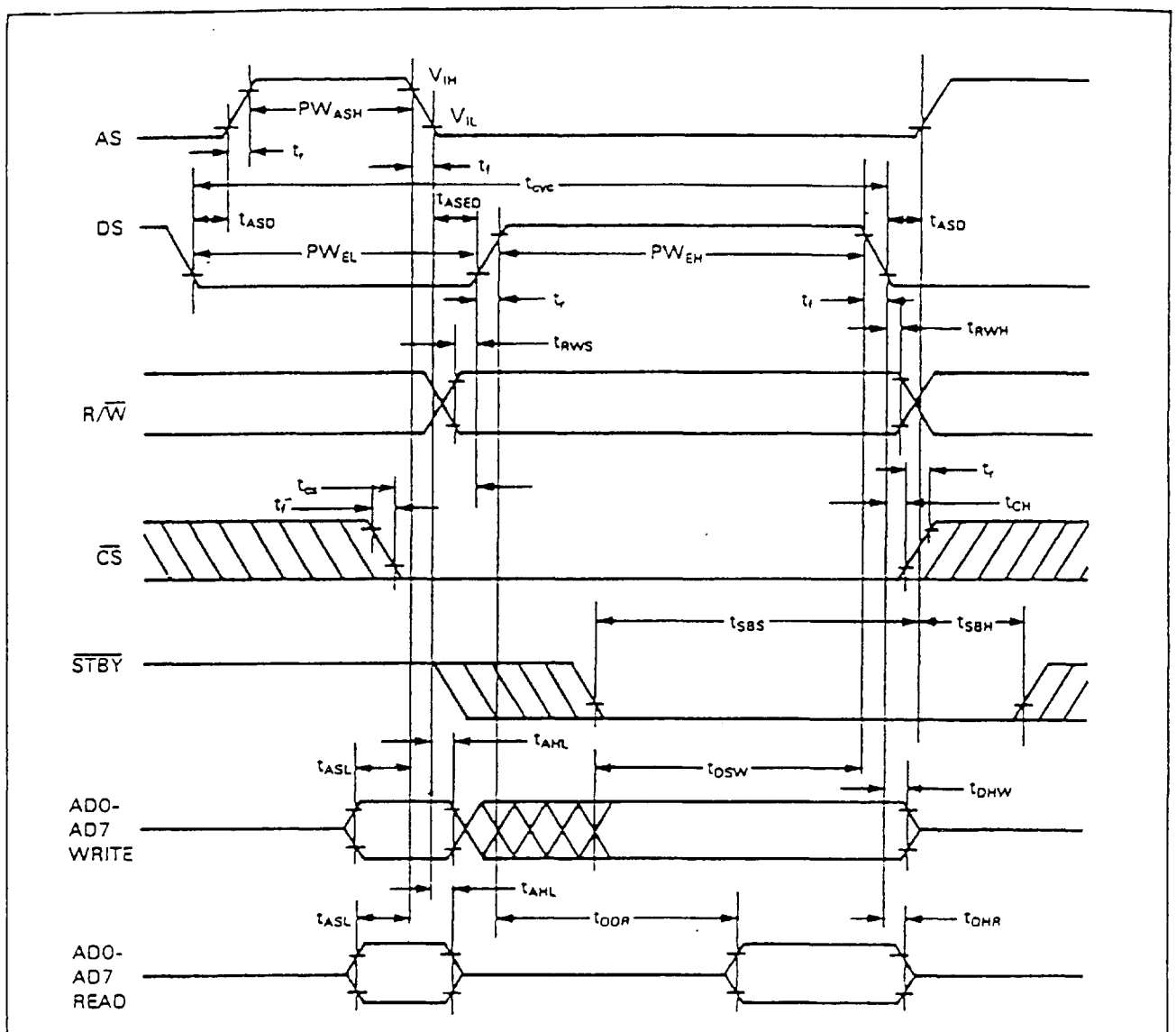
AC Characteristics (V_{SS} = 0 V, T_a = 0°C to + 70°C, unless otherwise noted.)

Bus Timing

Characteristics	Symbol	V_{CC} = 3.0 V 50 pF Load Min	Max	V_{CC} = 5.0 V ± 10% 1 TTL and 130 pF Load Min	Max	Unit
Cycle Time	t_{CYC}	5000	—	953	dc	ns
Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	1000	—	300	—	ns
Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	1500	—	325	—	ns
Input Rise and Fall Time	t_r, t_f	—	100	—	30	ns
R/$\overline{W}$ Hold Time	t_{RWH}	10	—	10	—	ns
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	200	—	80	—	ns
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	200	—	25	—	ns
Chip Select Hold Time	t_{CH}	10	—	0	—	ns
Read Data Hold Time	t_{DHR}	10	—	10	—	ns
Write Data Hold Time	t_{DHW}	100	—	0	—	ns
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	200	—	50	—	ns
Muxed Address Hold Time	t_{AHL}	100	—	20	—	ns
Delay Time DS/E to AS/ALE Rise	t_{ASD}	500	—	50	—	ns
Pulse Width, AS/ALE High	PW_{ASH}	600	—	135	—	ns
Delay Time AS/ALE to DS/E Rise	t_{ASED}	500	—	60	—	ns
Peripheral Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	1300	—	20	240	ns
Peripheral Data Setup Time	t_{DSW}	1500	—	200	—	ns
$\overline{STBY}$ Setup Time before AS/ALE Rise	t_{SBS}	20	—	20	—	ns
$\overline{STBY}$ Hold Time after AS/ALE Rise	t_{SBH}	100	—	50	—	ns

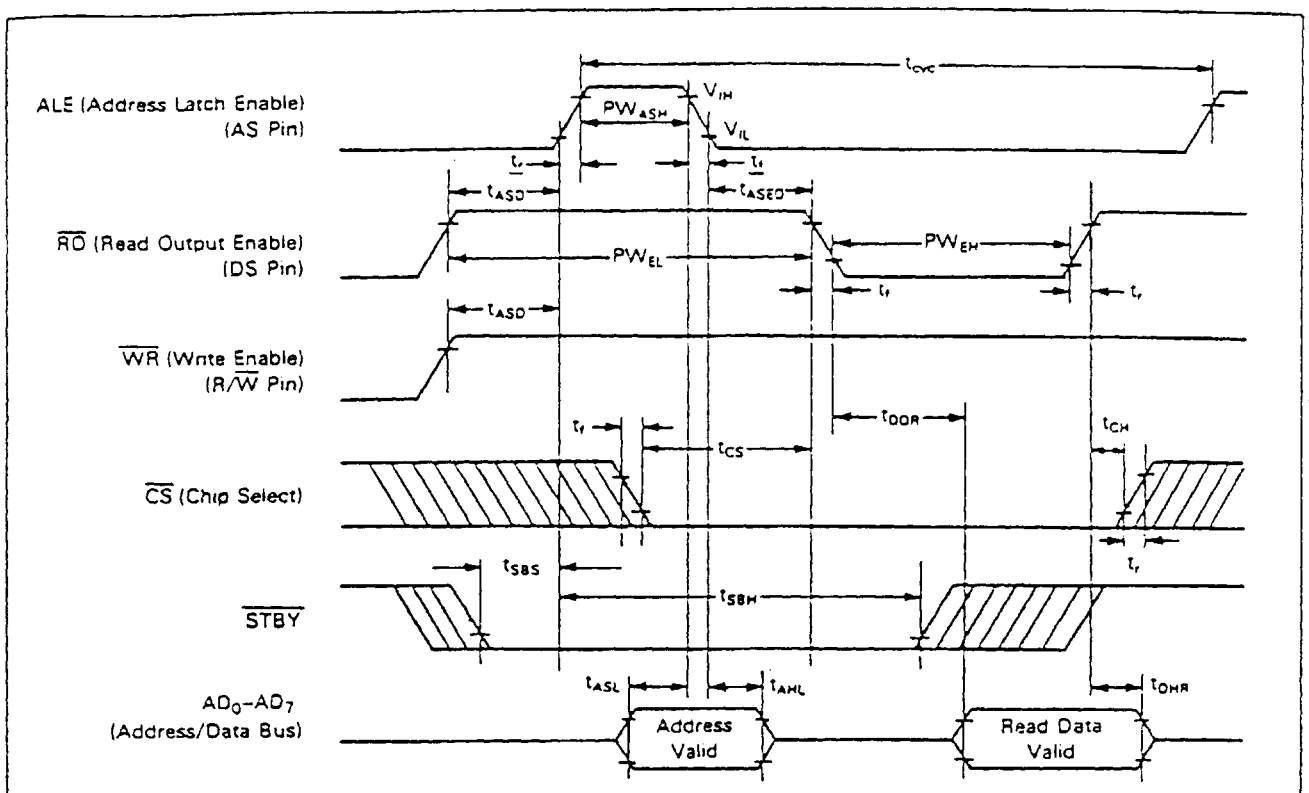
Control Signal Timing

Description	Symbol	V_{CC} = 3.0 V Min	V_{CC} = 3.0 V Max	V_{CC} = 5.0 V ± 10% Min	V_{CC} = 5.0 V ± 10% Max	Unit
Oscillator Startup 4MHz, 1MHz	t_{RC}	—	—	—	100	ms
Oscillator Startup 32kHz	t_{RC}	—	—	—	1000	ms
Reset Pulse Width	t_{RWL}	TBD	—	5	—	μs
Reset Delay Time	t_{RLH}	TBD	—	5	—	μs
Power Sense Pulse Width	t_{PWL}	TBD	—	5	—	μs
Power Sense Delay Time	t_{PLH}	TBD	—	5	—	μs
$\overline{IRQ}$ Release from DS	t_{IRDS}	—	TBD	—	2	μs
$\overline{IRQ}$ Release from $\overline{RES}$	t_{IRR}	—	TBD	—	2	μs
VRT Bit Delay	t_{VRTD}	—	TBD	—	2	μs



Note: $V_{OH} = V_{CC} - 2.0$ V, $V_{OL} = 0.8$ V for $V_{CC} = 5.0$ V ± 10 % for outputs only.
$V_{OH} = 2.0$ V, $V_{OL} = 0.5$ V, for $V_{CC} = 3.0$ V for outputs only.

Figure 19. Bus Read, Write Timing (6801 Family)



Note: $V_{OH} = V_{CC} - 2.0\,V$, $V_{OL} = Q.8\,V$, for $V_{CC} = 5.0\,V \pm 10\,\%$ for outputs only.
$V_{OH} = 2.0\,V$, $V_{OL} = 0.5\,V$, for $V_{CC} = 3.0\,V$, for outputs only

Figure 20. Read Timing (8085 Family)

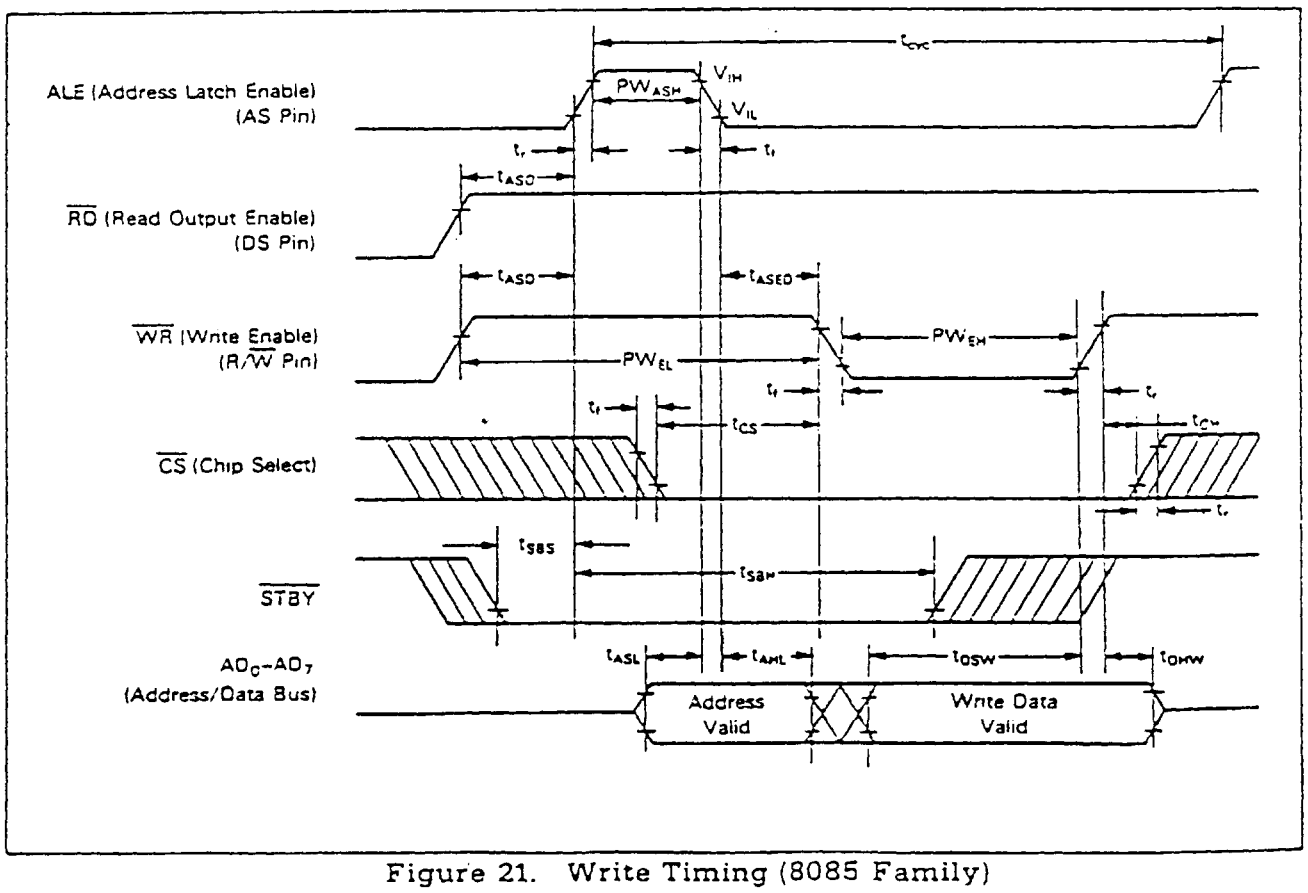


Figure 21. Write Timing (8085 Family)

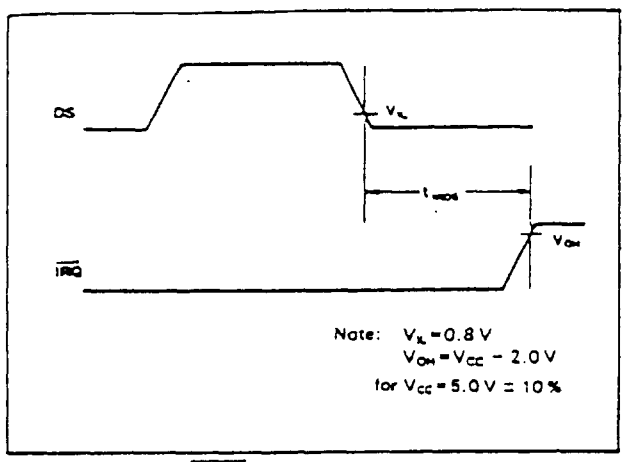


Figure 22. $\overline{IRQ}$ Release Delay (from DS)

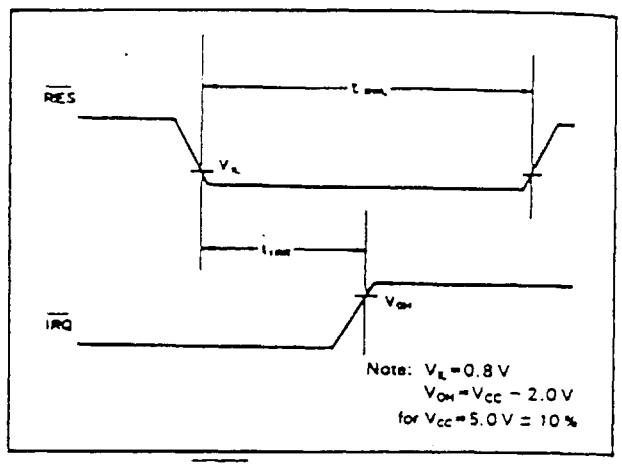


Figure 23. $\overline{IRQ}$ Release Delay (from $\overline{RES}$)

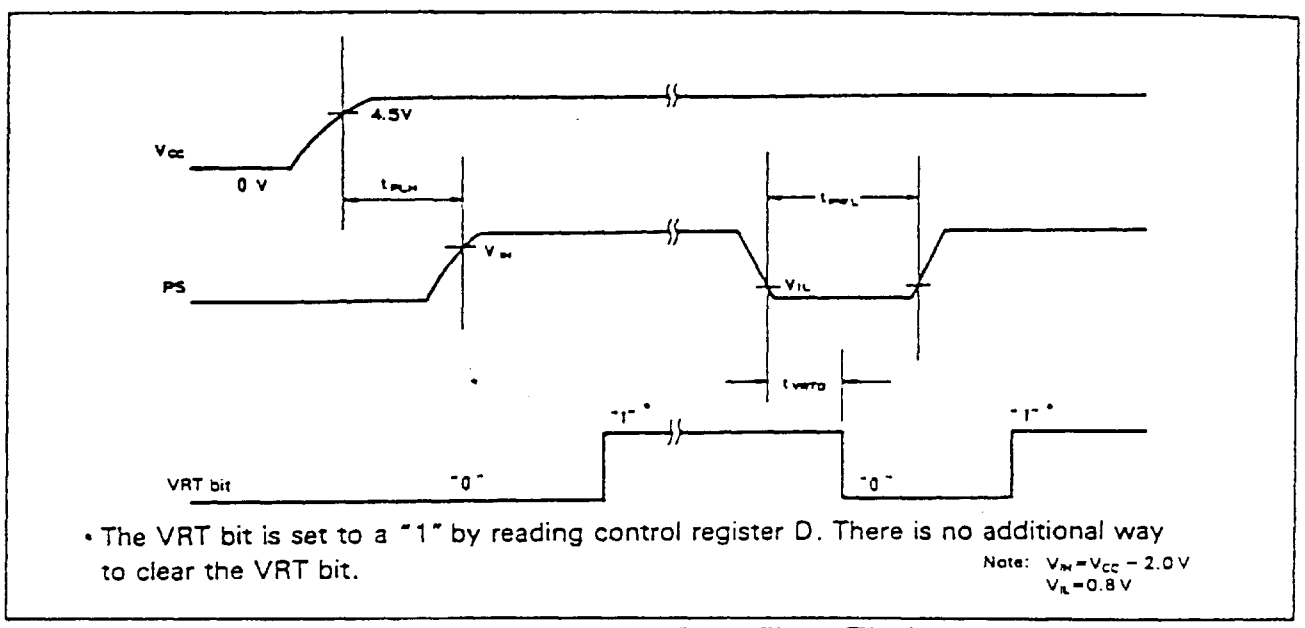


Figure 24. VRT Bit Clear Timing

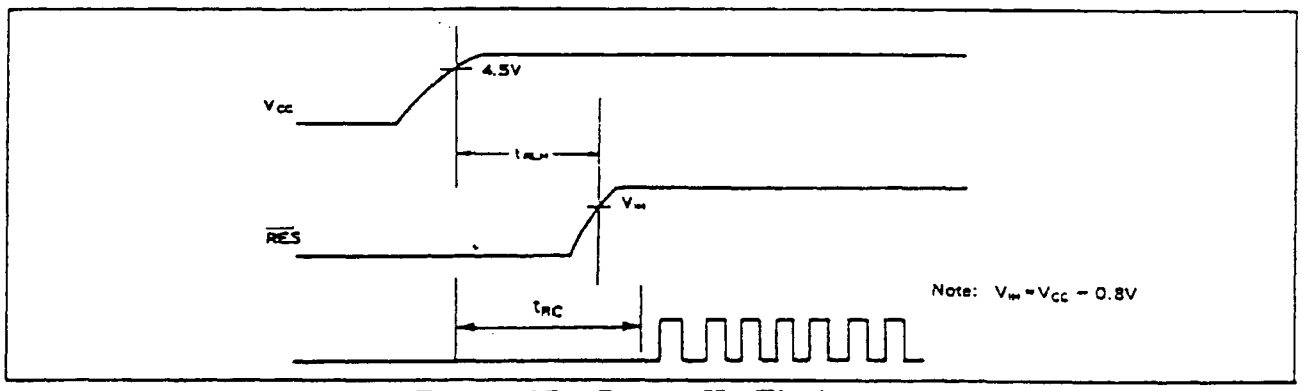


Figure 25. Power Up Timing

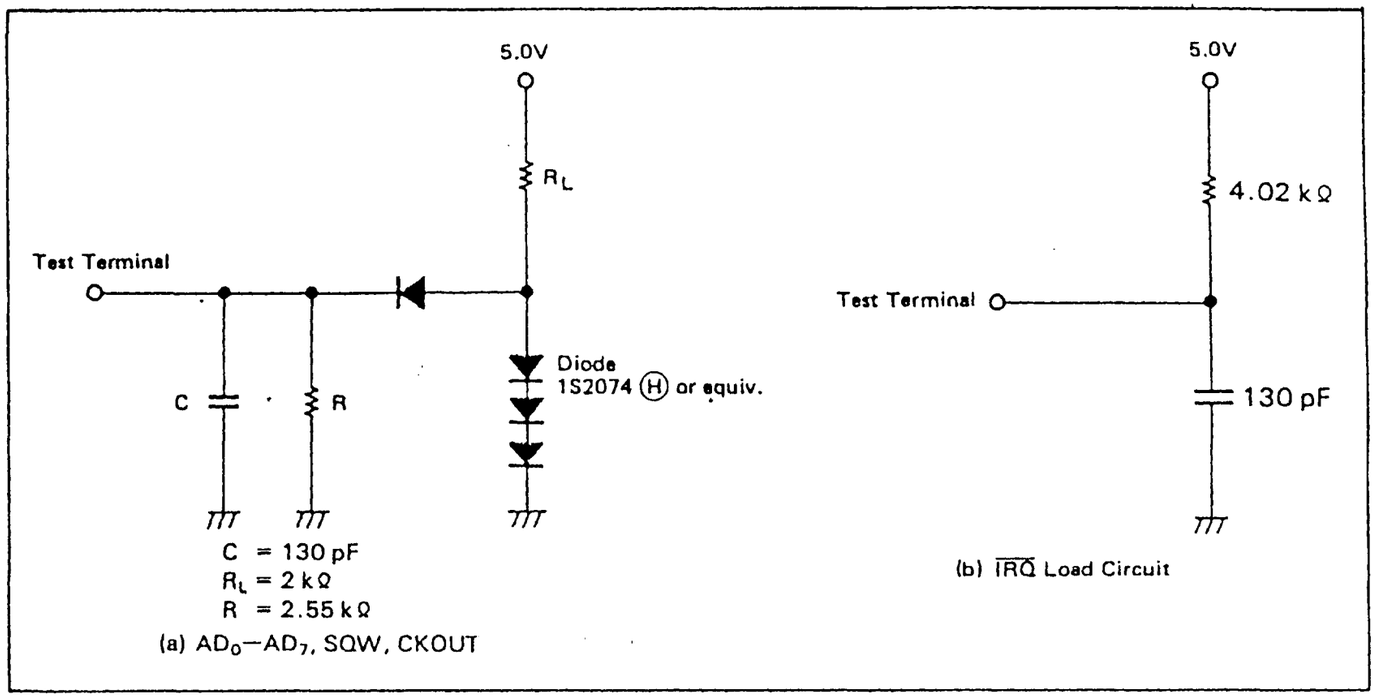


Figure 26. Test Load

Restriction on HD146818A Usage

The daylight saving function can not be performed on the HD146818A. So do not use this function for the system design.

<Restriction on usage>

Please set "0" to DSE bit (Daylight Saving Enable bit) on initializing the control register B.
DSE = "1" is prohibited.

Package Dimension

Unit: mm (inch)

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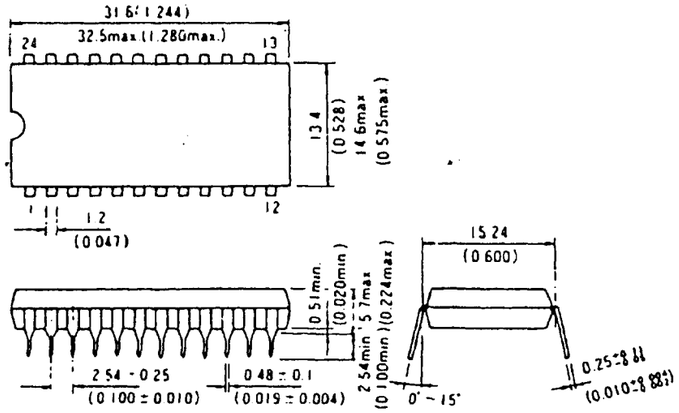

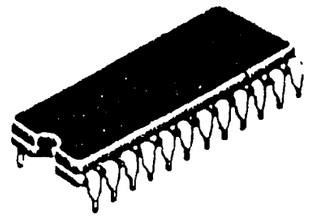

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