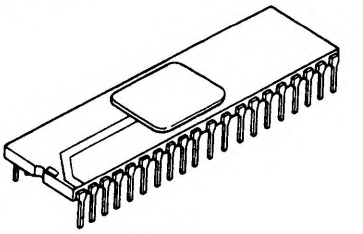
HD6843, HD68A43
FDC (Floppy Disk Controller)

The HD6843 Floppy Disk Controller performs the complex MPU/Floppy interface function. The FDC was designed to optimize the balance between the "Hardware/Software" in order to achieve integration of all key functions and maintain flexibility.

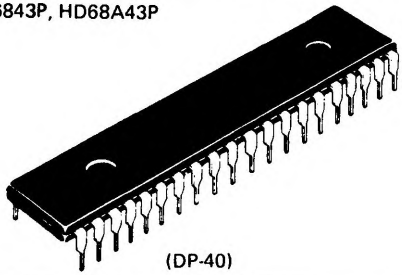
The FDC can interface a wide range of drives with a minimum of external hardware. Multiple drives can be controlled with the addition of external multiplexing rather than additional FDC's.

HD6843, HD68A43



(DC-40)

HD6843P, HD68A43P

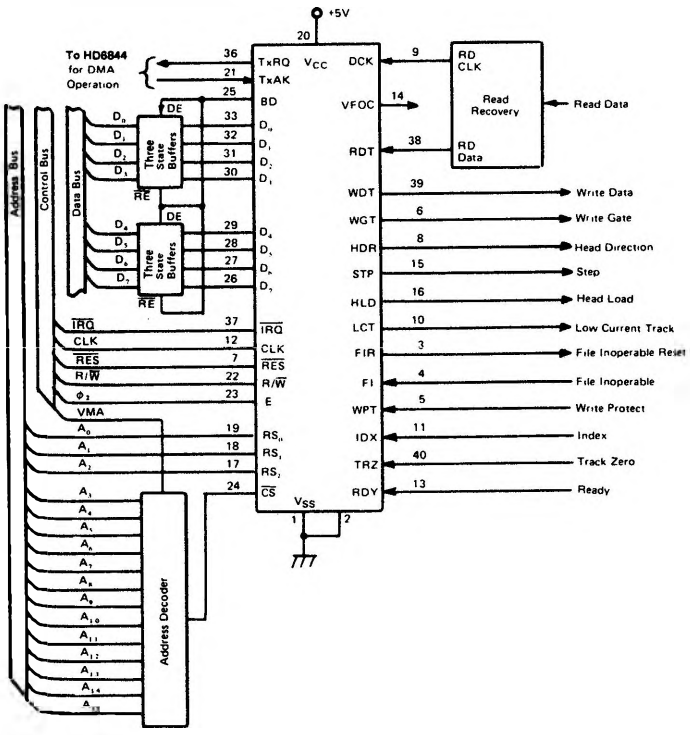


(DP-40)

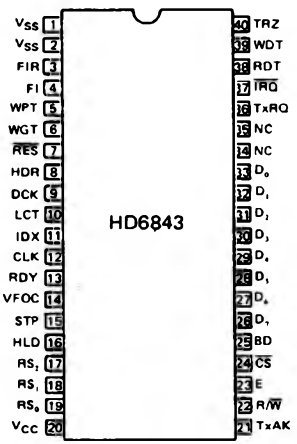
■ FEATURES

- Format compatible with IBM3740
- User Programmable read/write format
- Ten powerful macro-commands
- Macro End Interrupt allows parallel processing of MPU and FDC
- Controls multiple Floppies with external multiplexing
- Direct interface with HMCS6800
- Programmable seek and settling times enable operation with a wide range of Floppy drives
- Offers both Programmed Controlled I/O (PCIO) and DMA data transfer mode
- Free-Format read or write
- Single 5-volt power supply
- All registers directly accessible
- Compatible with MC6843

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}*	-0.3 ~ +7.0	V
Input Voltage	V_{in}*	-0.3 ~ +7.0	V
Operating Temperature	T_{opr}	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

(NOTE) Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V
Input "High" Voltage	V_{IH}*	2.0	–	V_{CC}	V
Input "Low" Voltage	V_{IL}*	-0.3	–	0.8	V
Operating Temperature	T_{opr}	-20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC}=5V±5%, V_{SS}=0V, Ta=-20~+75°C, unless otherwise noted.)

Item		Symbol	Test Condition	min.	typ.*	max.	Unit
Input "High" Voltage		V_{IH}		2.0	–	V_{CC}	V
Input "Low" Voltage		V_{IL}		-0.3	–	0.8	V
Input Leakage Current		I_{in}	V_{in}=0~5.25V	–	1.0	2.5	μA
Output "High" Voltage		V_{OH}	I_{OH}=-205μA (D_0~D_7) I_{OH}=-100μA (Others)	2.4	–	–	V
Output "Low" Voltage		V_{OL}	I_{OL}=3.2mA ($\overline{IRQ}$) I_{OL}=1.6mA (Others)	–	–	0.4	V
Three-state (off-state) Leakage Current		I_{TSI}	V_{in}=0.4~2.4V	–	2.0	10	μA
Output Leakage (off-state) Current ($\overline{IRQ}$)		I_{LOH}	V_{OH}=2.4V	–	1.0	10	μA
Power Dissipation		P_D		–	600	1000	mW
Input Capacitance	D_0~D_7	C_{in}	V_{in}=0V, T_a=25°C, f=1 MHz	–	–	12.5	pF
	Other inputs			–	–	10	pF
Output Capacitance		C_{out}	V_{in}=0V, T_a=25°C, f=1 MHz	–	–	10	pF

* V_{CC} = 5V, Ta = 25°C

• AC CHARACTERISTICS (V_{CC}=5V±5%, V_{SS}=0V, Ta=-20~+75°C, unless otherwise noted.)

Item	Symbol	Test Condition	HD6843			HD68A43			Unit
			min.	typ.	max.	min.	typ.	max.	
CLK Cycle Time	t_{cycC}	Figure 1	–	1.0	–	–	1.0	–	μs
CLK Pulse Width, "High"	PW_{HC}	Figure 1	0.4	–	–	0.4	–	–	μs
CLK Pulse Width, "Low"	PW_{LC}	Figure 1	0.35	–	–	0.35	–	–	μs
Rise and Fall Time of CLK	t_{Cr}, t_{Cf}	Figure 1	–	–	25	–	–	25	ns
DCK Cycle Time	t_{cycD}	Figure 2	2.6	4.0	–	2.6	4.0	–	μs
DCK Pulse Width, "High"	PW_{HD}	Figure 2	1.3	1.95	–	1.3	1.95	–	μs
DCK Pulse Width, "Low"	PW_{LD}	Figure 2	1.3	1.95	–	1.3	1.95	–	μs
Rise and Fall Time of DCK	t_{Dr}, t_{Df}	Figure 2	–	–	25	–	–	25	ns
RDT Width, "High"	t_{RDH}	Figure 2	1.0	–	–	1.0	–	–	μs
RDT Width, "Low"	t_{RDL}	Figure 2	1.0	–	–	1.0	–	–	μs
RDT~DCK Delay Time 1	t_{RDD1}	Figure 2	0.15	–	1.70	0.15	–	1.70	μs
RDT~DCK Delay Time 2	t_{RDD2}	Figure 2	0.15	–	1.70	0.15	–	1.70	μs
IDX Pulse Width, "High"	PW_{IDX}	Figure 3	20.0	–	–	20.0	–	–	μs
FIR Delay Time	t_{FIRD}	Figure 4	–	–	450	–	–	450	ns
FIR Pulse Width, "High"	PW_{FIR}	Figure 4	200	–	–	200	–	–	ns
WDT Pulse Width, "High"	PW_{WD}	Figure 7	–	1.0	–	–	1.0	–	μs
WDT Cycle Time	t_{cycW}	Figure 7	–	2.0	–	–	2.0	–	μs
STP Pulse Width, "High"	PW_{STP}	Figure 5	–	32	–	–	32	–	μs
STP Cycle Time	t_{cycS} *	Figure 5	1	–	15	1	–	15	ms
HLD Delay Time (HLD~STP)	t_{HLDD}	Figure 5	1	–	15	1	–	15	μs
HDR Set Up Time	t_{HDRS}	Figure 5	0	–	–	0	–	–	ns
HDR Hold Time	t_{HDRH}	Figure 5	32	–	–	32	–	–	μs
TxAK Set Up Time	t_{AS3}	Figure 10, 11	140	–	–	140	–	–	ns
TxAK Hold Time	t_{AH3}	Figure 10, 11	10	–	–	10	–	–	ns
TxRQ Release Time	t_{TR}	Figure 10, 11	–	–	450	–	–	240	ns
$\overline{IRQ}$ Release Time	t_{IR}	Figure 6	–	–	1.2	–	–	1.2	μs

* Cycle Time of STP changes according to the program.

• BUS TIMING CHARACTERISTICS (V_{CC}=5V±5%, V_{SS}=0V, Ta=-20~+75°C, unless otherwise noted.)

1 READ OPERATION SEQUENCE

Item	Symbol	Test Condition	HD6843			HD68A43			Unit
			min.	typ.	max.	min.	typ.	max.	
Enable Cycle Time	t_{cycE}	Figure 8, 10	1.0	–	–	0.666	–	–	μs
Enable Pulse Width, "High"	PW_{EH}	Figure 8, 10	0.4	–	–	0.23	–	–	μs
Enable Pulse Width, "Low"	PW_{EL}	Figure 8, 10	0.4	–	–	0.23	–	–	μs
Rise and Fall Time of Enable Input	t_{Er}, t_{Ef}	Figure 8, 10	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}	Figure 8, 10	140	–	–	140	–	–	ns
Data Delay Time	t_{DDR}	Figure 8, 10	–	–	225	–	–	200	ns
Data Access Time	t_{ACC}	Figure 8, 10	–	–	365	–	–	340	ns
Data Hold Time	t_{H}	Figure 8, 10	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}	Figure 8, 10	10	–	–	10	–	–	ns
Bus Direction Delay Time	t_{DBD}	Figure 8, 10	–	–	400	–	–	400	ns

2 WRITE OPERATION SEQUENCE

Item	Symbol	Test Condition	HD6843			HD68A43			Unit
			min.	typ.	max.	min.	typ.	max.	
Enable Cycle Time	t_{cycE}	Figure 9, 11	1.0	–	–	0.666	–	–	μs
Enable Pulse Width, "High"	PW_{EH}	Figure 9, 11	0.4	–	–	0.23	–	–	μs
Enable Pulse Width, "Low"	PW_{EL}	Figure 9, 11	0.4	–	–	0.23	–	–	μs
Rise and Fall Time of Enable Input	t_{Er}, t_{Ef}	Figure 9, 11	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}	Figure 9, 11	140	–	–	140	–	–	ns
Data Set Up Time	t_{DSW}	Figure 9, 11	100	–	–	60	–	–	ns
Data Hold Time	t_H	Figure 9, 11	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}	Figure 9, 11	10	–	–	10	–	–	ns
Bus Direction Delay Time	t_{DBD}	Figure 9, 11	–	–	400	–	–	400	ns

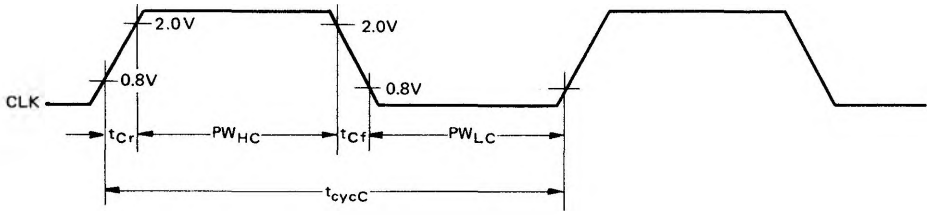


Figure 1 CLK Waveform

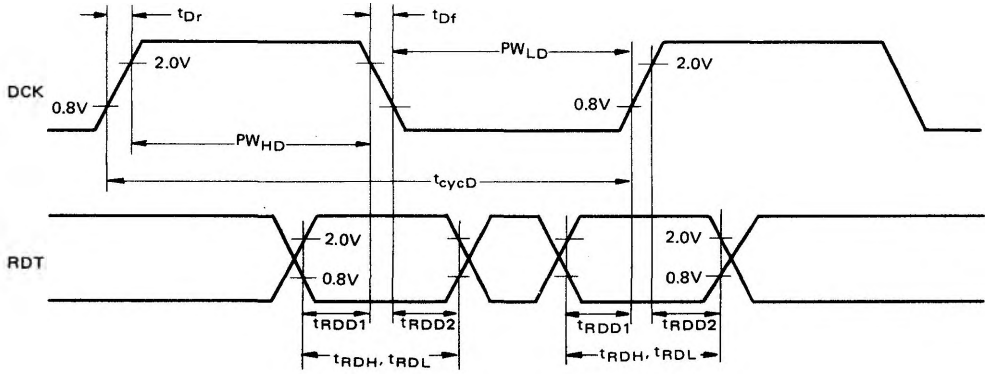


Figure 2 DCK, RDT Timing

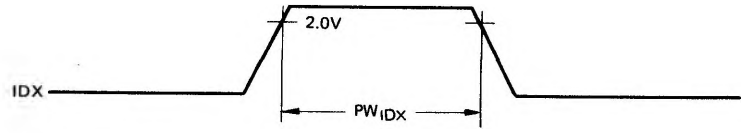


Figure 3 IDX Waveform

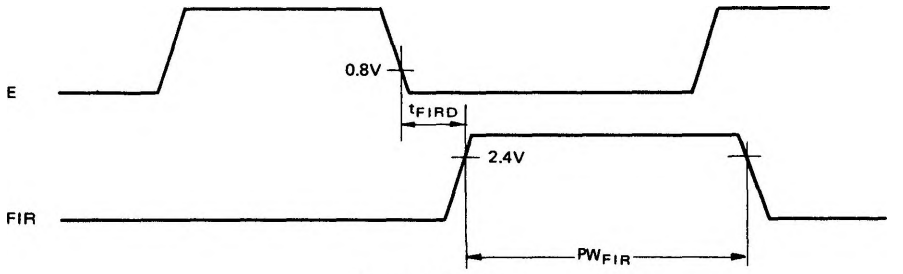


Figure 4 FIR Timing

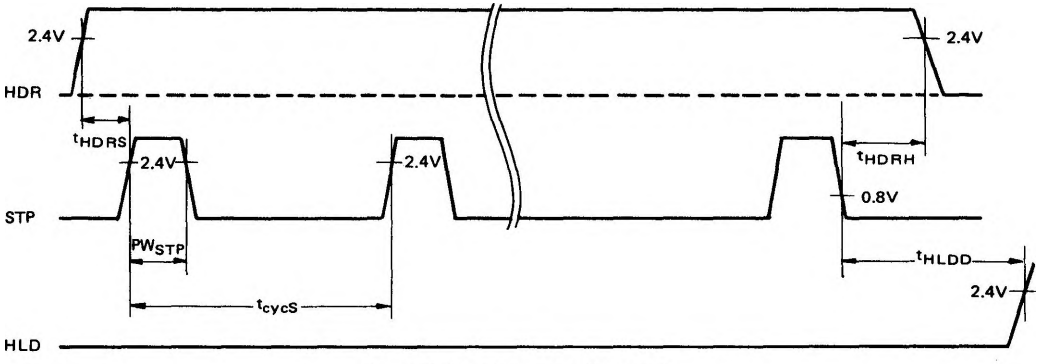


Figure 5 Seek Operation Sequence

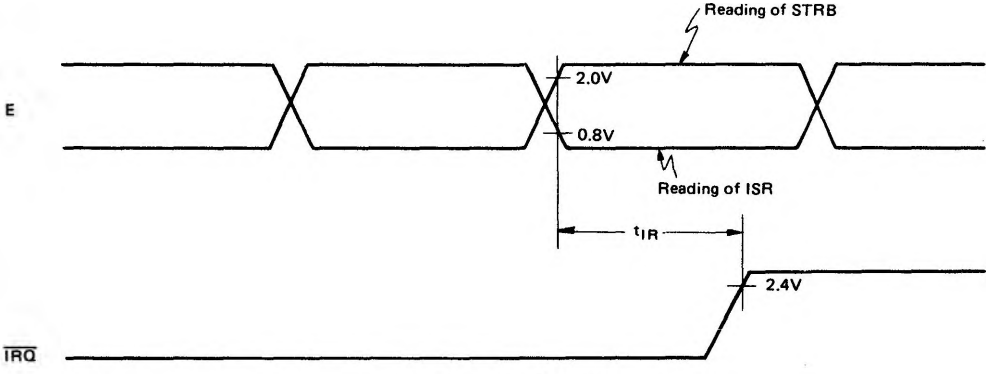


Figure 6 $\overline{IRQ}$ Release Timing

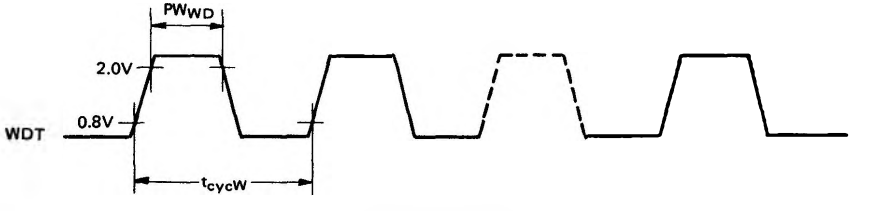


Figure 7 WDT Waveform

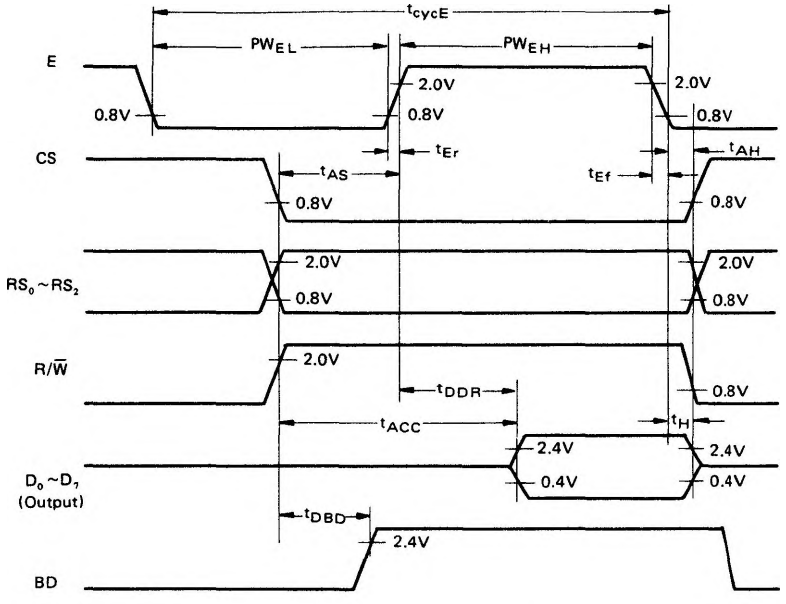


Figure 8 Read Timing

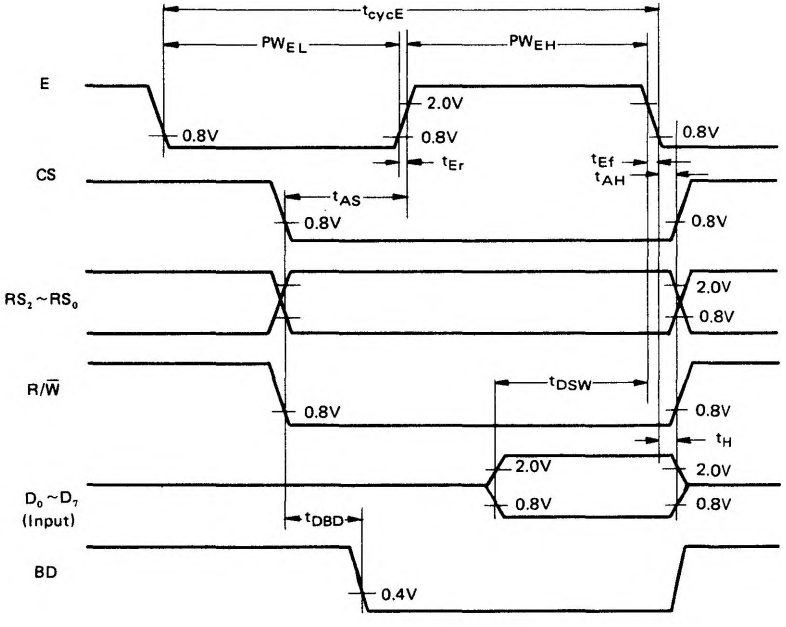


Figure 9 Write Timing

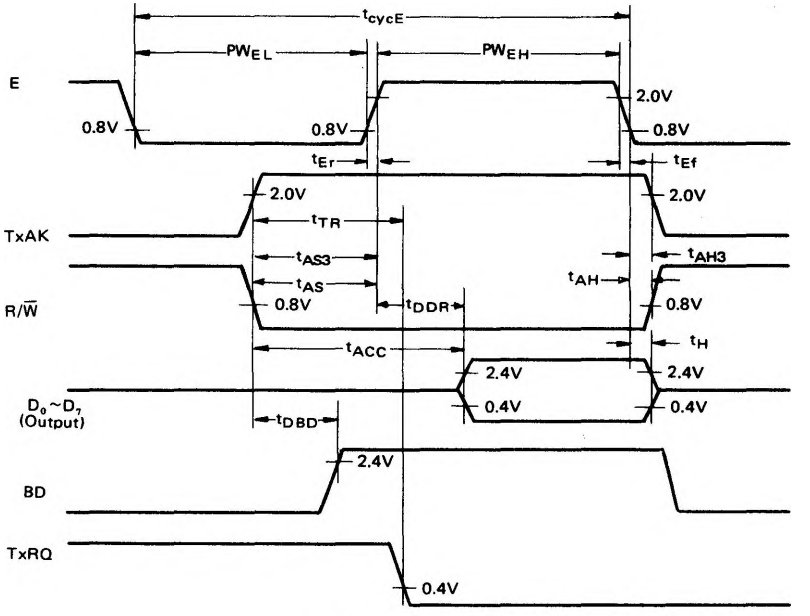


Figure 10 DMA Read Timing

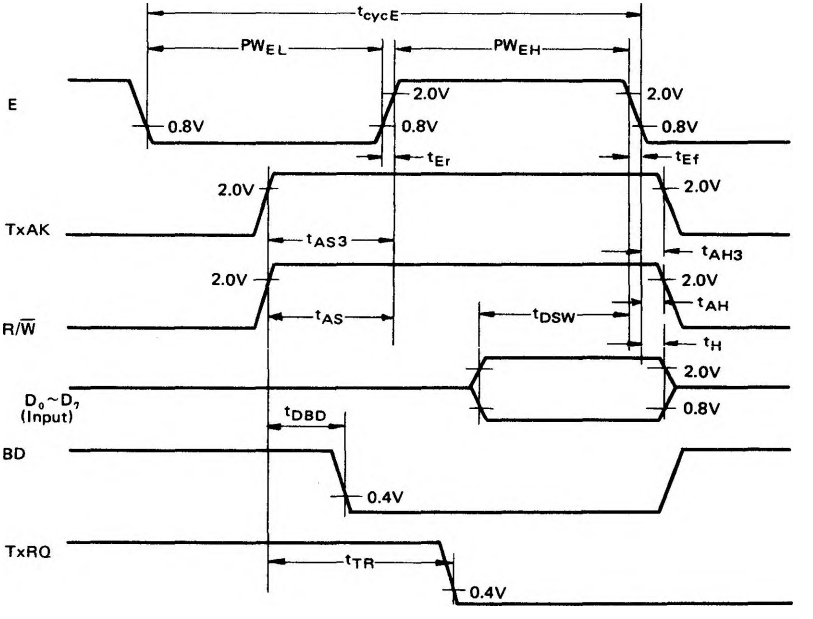


Figure 11 DMA Write Timing

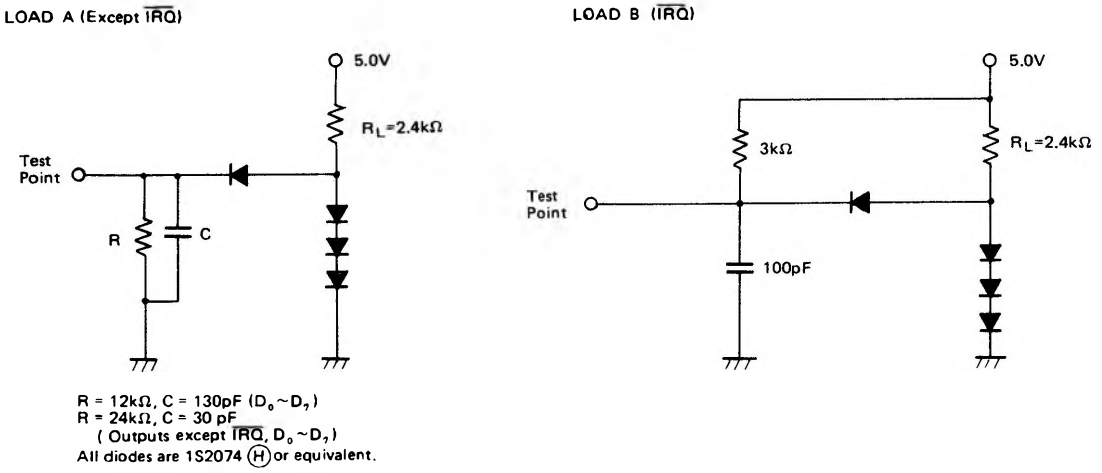


Figure 12 Load Circuit

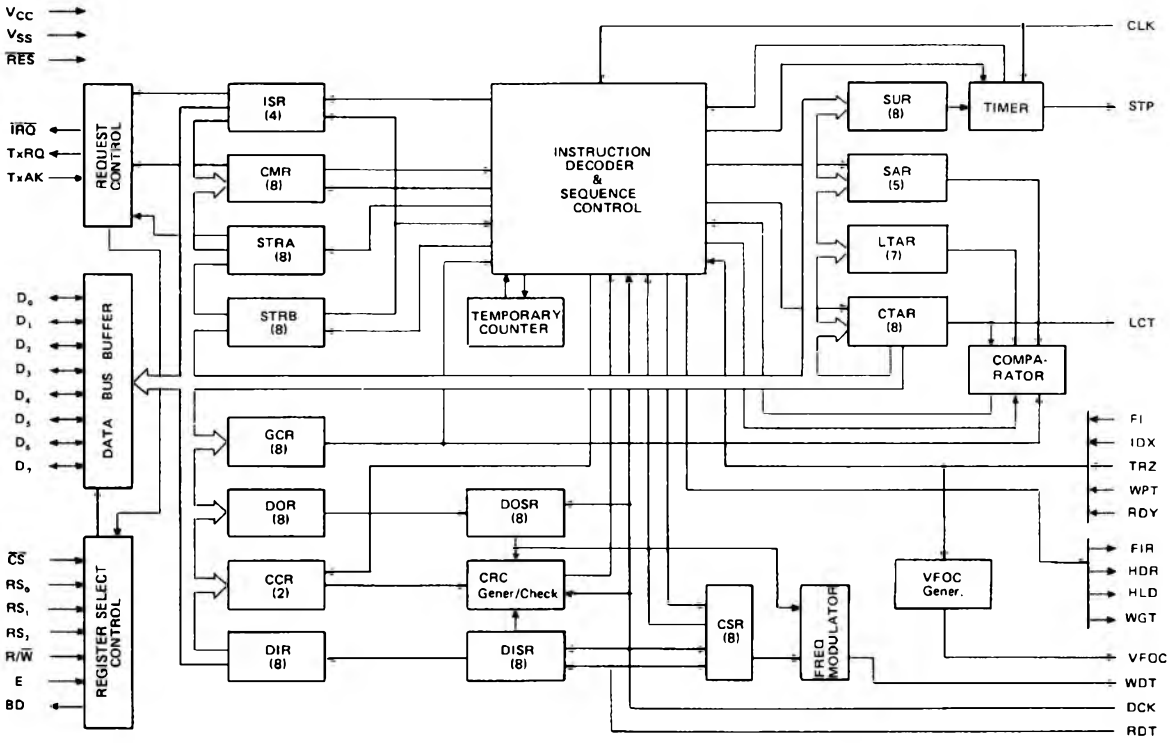


Figure 13 Block Diagram of the FDC

■ GENERAL DESCRIPTION

The HD6843 FDC consists of four primary sections; the Register, Serializing, Bus Interface, and Control sections. The following explanation of these sections can be followed in the block diagram of Figure 13.

• Register Section

The register section consists of twelve user accessible registers used for controlling a floppy disk drive. All twelve are connected by the internal data bus to allow the processor access to them.

Data Output Register (DOR)

The DOR is an 8-bit register which holds the data to be written onto the disk. The information is stored here by the bus interface.

Data Input Register (DIR)

The data words read from the disk are stored in the 8-bit DIR until read by the bus interface.

Current Track Address Register (CTAR)

CTAR is a 8-bit register containing the address of the track over which the R/W head is currently positioned.

Command Register (CMR)

The macro commands are written to the 8-bit CMR to begin their execution.

Interrupt Status Register (ISR)

The four bits of the ISR represent the four conditions that can cause an interrupt to occur.

Set-Up Register (SUR)

Variable Seek and Settling times are programmed by the SUR. Four bits are used to program the track to track seek time and four bits are used to program the head settling time for the floppy disk drive used with the FDC.

Status Register A (STRA)

The eight bits of STRA are used to indicate the state of the floppy disk interface.

Sector Address Register (SAR)

SAR contains the five bit sector address associated with the current data transfer.

Status Register B (STRB)

The eight error flags of STRB are used to signify error conditions detected by the FDC or generated by the floppy disk drive.

General Count Register (GCR)

The seven bits of GCR contain the destination track address when a SEK (seek) macro command is being executed. If a multi-sector Read or Write macro command is being executed, GCR contains the number of sectors to be read or written.

CRC Control Register (CCR)

The two bits of the CCR are used to enable the CRC and shift the CRC for the Free Format Commands.

Logical Track Address Register (LTAR)

The seven bit track address used for read and write operations is stored in the LTAR by the bus interface.

• Serializing Section

The serializing section handles the serial-to-parallel and parallel-to-serial conversions for Read/Write operations as well as CRC generation/checking and the generation/detection of the clock pattern. The Data Output Shift Register (DOSR), Data Input Shift Register (DISR), CRC Generator/Checker, and Clock Shift Register (CSR) comprise the serializing section of the FDC.

• Bus Interface

The Bus Interface section provides the timing and control logic that allows the FDC to operate with the 6800 bus, and is comprised of the Data Buffers. Request Control, and the Register Select circuitry.

• Control

The internal timing and control signals which sequence the FDC are derived from the macro instructions by the control section.

■ HD6843 PIN DESCRIPTION

• Power Pins

V_{CC}: +5 volt (±5%) power input.
V_{SS}: Power Supply Ground.

• Bus Pins

Reset ($\overline{RES}$) Input

The $\overline{RES}$ input is used to initialize the FDC. When $\overline{RES}$ becomes "Low", the state of the outputs is defined by the table below:

Output	State of Output	Output	State of Output
FIR	"Low"	HLD	"Low"
WGT	"Low"	TxRQ	"Low"
HDR	"Low"	$\overline{IRQ}$	"High"
STP	"Low"	WDT	"Low"

Registers which are affected by $\overline{RES}$ are shown in Table 7.

Interrupt Request ($\overline{IRQ}$) Output

The $\overline{IRQ}$ line is an open drain output that becomes a "Low" level (logic "0") when the FDC requests an interrupt. Interrupt requests are controlled by the interrupt enables in CMR (Command Register) with the function causing the interrupt shown in ISR (Interrupt Status Register).

Data Bus 0~Data Bus 7 (D_0~D_7) Bidirectional

The 8 bidirectional data lines allow the transfer of data between the FDC and the controlling system. The output buffers are three-state drivers that are enabled when the FDC is transferring data to the data bus.

Enable (E) Input

The E input to the FDC causes data transfers to occur between the FDC and the system controlling the FDC

(HMCS6800 MPU, DMA Controller, etc.) E must be a logic "1" ("High" level) for any transfer to be enabled on $D_0 \sim D_7$. The E input is normally connected to system ϕ_2.

Chip Select ($\overline{CS}$) Input

The $\overline{CS}$ input in conjunction with the E input, is used to enable data transfers on $D_0 \sim D_7$. E must be a "High" level and $\overline{CS}$ must be a "Low" level (logic "0") to enable the transfer. The TxAK input being a "High" level (logic "1") performs a similar function as $\overline{CS}$ being a "Low" level.

Read/Write (R/$\overline{W}$) Input

The R/$\overline{W}$ input is issued by the system controlling the FDC (HMCS6800 MPU, DMA Controller, etc.) to signify if a read or write operation is to be performed on the FDC. When TxAK is a "Low" level, R/$\overline{W}$ is used in conjunction with $\overline{CS}$ and $RS_0 \sim RS_2$ to determine which register is accessed by the bus as shown in Table 1. When TxAK is a "High" level, R/$\overline{W}$ is used to select either the DOR or DIR to the data bus (see description of TxAK input).

Register Select 0~Register Select 2 ($RS_0 \sim RS_2$) Input

$RS_0 \sim RS_2$, in conjunction with the R/$\overline{W}$ input, are used to select one of the user accessible registers in the FDC as shown in Table 1.

Transfer Request (TxRQ) Output

TxRQ is used in the DMA mode to request a data transfer from the DMAC. TxRQ is a "High" level if the FDC is in the DMA mode (CMR bit 5 is set) when a data transfer request occurs (STRA bit 0 is set). It is reset to a "Low" level (logic "0") when TxAK becomes a "High" level (logic "1"). Data transfer errors will occur if TxAK does not reset TxRQ before the next data transfer is required.

Transfer Acknowledge (TxAK) Input

TxAK is generated by the system controlling the FDC (HMCS6800 MPU, DMA Controller, etc.) and is a response to a TxRQ issued by the FDC. A "High" level (logic "1") on TxAK causes the FDC to neglect the state of $RS_0 \sim RS_2$ causing the FDC to select the DOR (Data Output Register) or DIR (Data Input Register) to the data bus ($D_0 \sim D_7$) as shown in Table 2. $\overline{CS}$ = "0" and TxAK = "1" cannot be permitted at the same time.

Table 2 Register Selection for DMA Transfers

TxAK	$RS_0 \sim RS_2$	$\overline{CS}$	R/$\overline{W}$	Register Selected
1	X	1	1	DOR
1	X	1	0	DIR

"1" ..... "High", "0" ..... "Low"

This mode of operation is normally used for DMA (Direct Memory Access) transfer with the FDC.

When TxAK is a "Low" level the registers are selected by $\overline{CS}$, R/$\overline{W}$ and $RS_0 \sim RS_2$ as shown in Table 1.

- **Bus Direction (BD) Output**

The BD output is provided to control external bidirectional buffers on the data bus ($D_0 \sim D_7$) as shown in Figure 14. Its polarity is shown by Table 3.

Table 3 Bus Direction (BD) States

TxAK	$\overline{CS}$	BD
1	1	R/$\overline{W}$
0	1	0
0	0	R/$\overline{W}$

"1" ..... "High", "0" ..... "Low"

(Operation of BD as defined by this chart allows the FDC to function with the DMA Controller HD6844.)

Table 1 Address Codes for User Accessible Registers

TxAK	$\overline{CS}$	RS_2	RS_1	RS_0	R/$\overline{W}$	Registers
0	0	0	0	0	0	DOR (Data Output Register)
					1	DIR (Data Input Register)
0	0	0	0	1	1/0	CTAR (Current Track Address Register)
0	0	0	1	0	0	CMR (Command Register)
					1	ISR (Interrupt Status Register)
0	0	0	1	1	0	SUR (Set Up Register)
					1	STRA (Status Regiser A)
0	0	1	0	0	0	SAR (Sector Address Register)
					1	STRB (Status Register B)
0	0	1	0	1	0	GCR (General Count Register)
0	0	1	1	0	0	CCR (CRC Control Register)
0	0	1	1	1	0	LTAR (Logical Track Address Register)

"1" ..... "High", "0" ..... "Low"

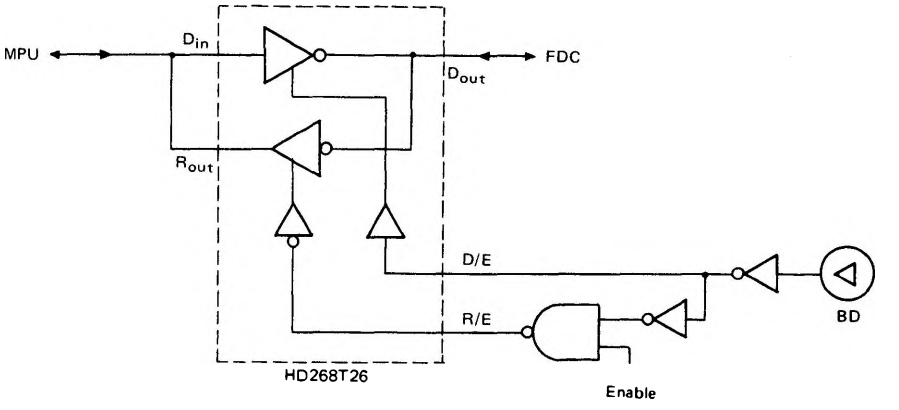


Figure 14 Bus Buffer Control

- **I/O and Control Pins**

Head Load (HLD) Output

HLD is used to notify the disk drive that the R/W head should be loaded (placed in contact with the media). When the FDC is ready for the head to load, HLD is a "High" level (logic "1"). A "Low" level (logic "0") HLD indicates the head should be unloaded.

Step (STP) Output

The STP output, in conjunction with HDR, is used to control head movement. A 32 μs wide positive (logic "1") pulse is generated on STP, to move the R/W head one track in the direction defined by the HDR output. The period of the STP signal is programmable by the SUR (Set-Up Register). The number of pulses generated on STP is the difference between the contents of the CTAR (Current Track Address Register), and the GCR (General Count Register) which contains the track address to which the head is to be moved.

Head Direction (HDR) Output

The HDR signal controls the direction of head movement. A "High" level (logic "1") signifies the head should step to the inside (toward the hub) of the disk. A "Low" level (logic "0") indicates the direction of head movement should be to the outside of the disk.

Low Current Track (LCT) Output

The LCT signal is used to control the level of write current used by the disk drive. LCT is a "Low" level (logic "0") when the write head is positioned over tracks 0~43. If it is over tracks 44~76, LCT is a "High" level (logic "1"). LCT is determined from the contents of the Current Track Address Register (CTAR).

Write Gate (WGT) Output

When a write operation is being performed, WGT is a logic "1" ("High" level). For a read operation, WGT is a "Low" level (logic "0").

File Inoperable Reset (FIR) Output

FIR is an output from the FDC to the floppy disk drive to reset it from an inoperable status. If the FI input is a "High" level, a pulse, of which width almost equals to E pulse "Low" width, is generated on the FIR output whenever Status Register B is read.

File Inoperable (FI) Input

FI is an input to the FDC from the drive. A "High" level indicates the drive is in an inoperable state. Its current state can be examined by reading bit 5 of Status Register B (STRB).

Track Zero (TRZ) Input

The TRZ input is reflected by bit 3 of STRA (Status Register A). The TRZ input must be a "High" level (logic "1") when the R/W head of the drive is positioned over track zero. A logic "1" on this input inhibits step pulses during a Seek Track Zero command.

Index (IDX) Input

The index input is received from the floppy disk drive and is used to sense the index hole in the disk media. The IDX signal is used to initialize the internal FDC timing. The state of the IDX input is reflected by bit 6 of Status Register A (STRA). A "High" level (logic "1") is to indicate the index hole is under the index sensor. The index input is used to count the number of disk revolutions while searching for the address ID field (see description of STRB bit 3).

Ready (RDY) Input

The ready input is received from the disk drive and can be read as bit 2 of STRA (Status Register A). A "High" level (logic "1") indicates the drive is ready and allows the FDC to operate the drive.

Write Protect (WPT) Input

WPT is an input indicating when the media is Write Protected. A "High" level during an FDC write operation results in a Write Error (STRB bit 6) but the FDC continues to perform the write function. The state of the WPT input can be read by examining bit 4 of the Status Register A (STRA).

Clock (CLK) Input

The CLK input is used to generate various timing sequences internal to the FDC. The head settling, seek time, step pulse width and write data pulse width, etc., are generated from the CLK input signal. The CLK is 1 MHz frequency and the duty is 50%.

- **Data Pins**

Data Clock (DCK) Input

DCK is used to clock data from the drive into the FDC. It is generated from the read data received from the drive.

Read Data (RDT) Input

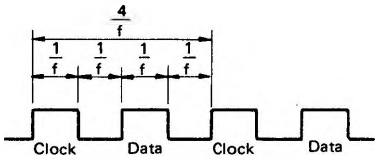
RDT is the serial data input from the drive. The data stream includes both the clock and data bits.

Write Data (WDT) Output

WDT is the double frequency modulated data output from the FDC. The time between clock bits is 4/f where f is the frequency of the clock input. The pulse width for both clock and data is 1/f (see Figure 15). For the normal clock frequency of 1 MHz the clock period is 4 μs, the clock pulse width is 1 μs and the data pulse width is 1 μs. Figure 15 shows the relationship between the WDT output and the frequency of the CLK inputs.

Variable Frequency Oscillator Control (VFOC) Output

VFOC is used as a sync signal during system diagnostics. Waveforms are shown in Figure 16.



f = Frequency of the CLK Input. To insure IBM3740 compatibility the clock frequency must be 1 MHz.

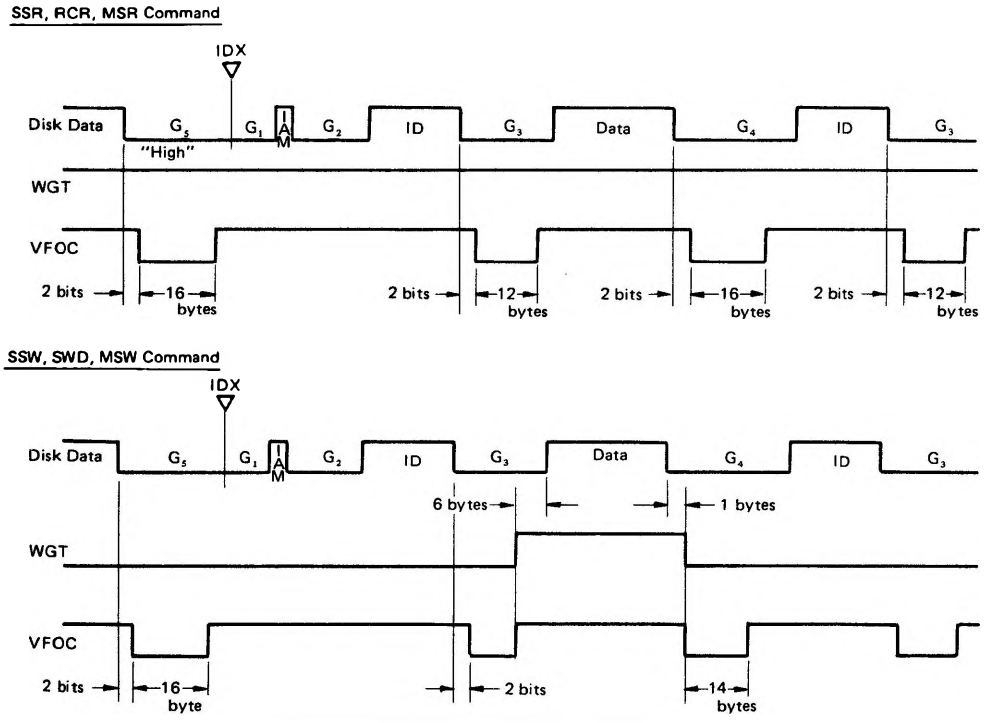
Figure 15 WDT Output Timing

■ FORMAT

The format used by the HD6843, shown in Figure 18, is compatible with the soft sector format of the IBM3740.

■ MACRO COMMAND SET

The macro command set shown in Table 4 is discussed in the following paragraphs.



In FFW Command, VFOC becomes "High" when WGT is at "High" level.
In FFR Command, VFOC remains "High".

Figure 16 Variable Frequency Oscillator Control Waveform (Relation Between WGT and VFOC)

SSW, SWD and MSW commands (Single Sector Write, Single Sector Write with Delet Data Mark, and Multi-Sector Write)

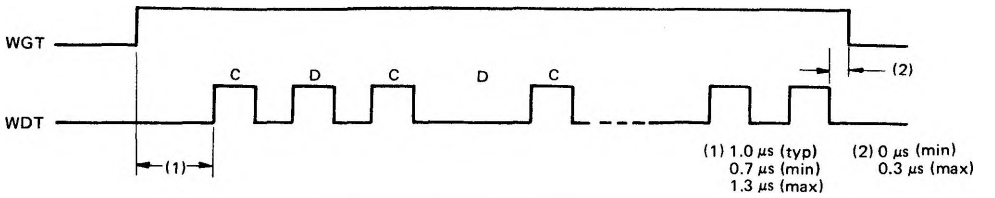


Figure 17 Write Data versus Write Gate Timing

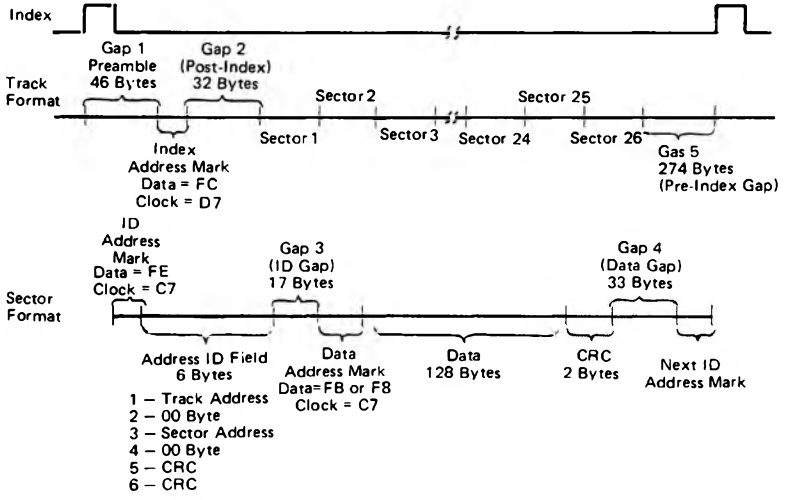


Figure 18 Soft Sector Format

Table 4 Macro Command Set

	Macro Command		CMR Bits				Hex Code
			Bit 3	Bit 2	Bit 1	Bit 0	
1	STZ	Seek Track Zero	0	0	1	0	2
2	SEK	Seek	0	0	1	1	3
3	SSR	Single Sector Read	0	1	0	0	4
4	SSW	Single Sector Write	0	1	0	1	5
5	RCR	Read CRC	0	1	1	0	6
6	SWD	Single Sector Write with Delete Data Mark	0	1	1	1	7
7	MSW	Multi Sector Write	1	1	0	1	D
8	MSR	Multi Sector Read	1	1	0	0	C
9	FFW	Free Format Write	1	0	1	1	B
10	FFR	Free Format Read	1	0	1	0	A

- **Seek Track Zero (STZ)**

The STZ command causes the R/W head to be released from the surface of the disk (HLD is reset) and positioned above track 00. The FDC issues step pulses on the STP output until the TRZ input becomes a "High" level or until 82 pulses have been sent to the drive. When the TRZ input becomes "High", the step pulses are inhibited on the STP output but the FDC remains busy until all 82 have been generated internally.

If the TRZ input remains "Low" (logic "0") after all 82 pulses have been generated, the seek error flag (STRB bit 4) is set.

After all 82 pulses have been generated, the head is loaded (HLD becomes a "High"). After the settling time specified in the SUR has expired, the Seek Command End flag is set (ISR bit 1), Busy STRA7 is reset, CTAR and GCR are cleared. The head remains in contact with the disk. A command such as RCR (Read CRC) may be issued following a STZ if the head must be released.

- **Seek (SEK)**

The SEK command is used to position the R/W head over the track on which a Read/Write operation is to be performed. The contents of the GCR are taken as the destination address and the content of the CTAR is the source address; therefore, the number of pulses (N) on the STP output are given by:

$$N = |(CTAR) - (GCR)|$$

HDR is a "High" for (GCR) > (CTAR) otherwise it is a "Low".

When a SEK command is issued, Busy is set, the head is raised from the disk, HDR is set as described above, and N number of pulses appear on the STP output. After the last step pulse is used, the head is placed in contact with the disk. Once the head settling time has expired, the Seek Command End flag (ISR bit 1) is set, Busy is reset, and the contents of the GCR are transferred to the CTAR.

■ SINGLE SECTOR READ/WRITE COMMANDS

The single sector Read/Write commands (SSR, RCR, SSW, and SWD) are used to Read/Write data from a single 128 byte sector on the disk. As shown in Figure 19 these types of instructions can be divided into two sections. The first section, which is common to all instructions, is the address search operation, while the second section is unique to the requirements of each instruction.

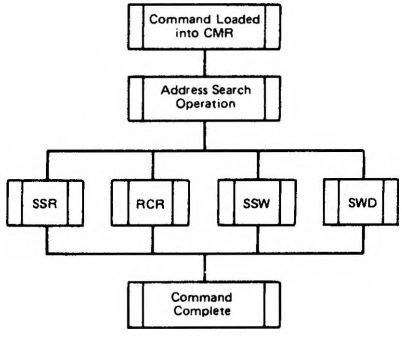


Figure 19 Basic Single Sector Command Flow Chart

- **Address Search Operation**

The flow chart of Figure 20 shows the operation of the address search operation.

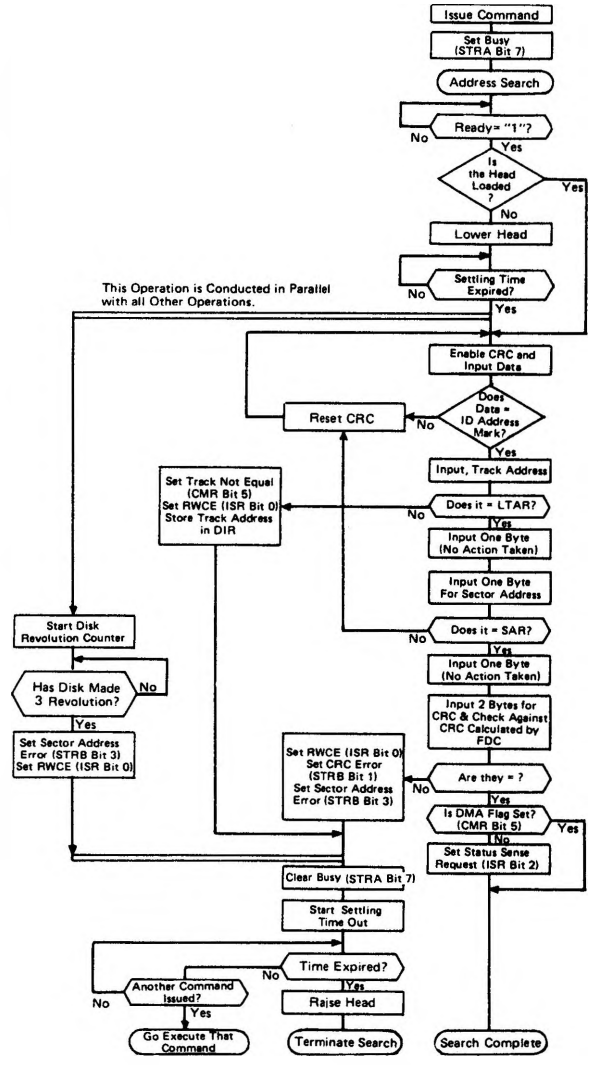


Figure 20 Operational Flow of the Address Search Sequence

- **Single Sector Read (SSR)**

The single sector read command follows the address search procedure as defined in the previous flowchart. If the search is successful, status sense request is set and the operation continues as described by the flowchart of Figure 21 .

- **Read CRC (RCR)**

The RCR command is used to verify that correct data was written on a disk. The operation is the same as for the SSR

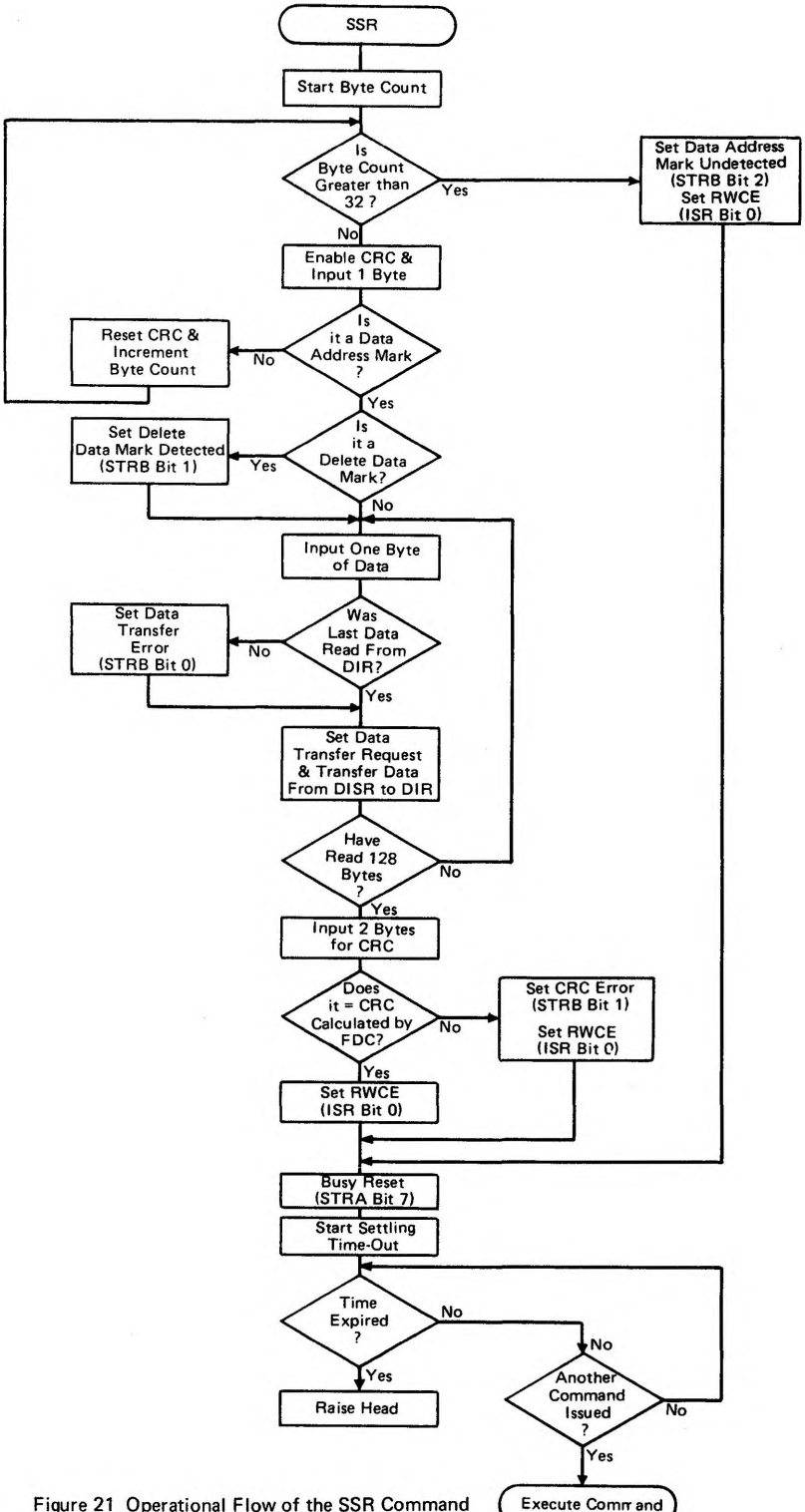


Figure 21 Operational Flow of the SSR Command

command with the exception that the data transfer request (STRA bit 0) is not set. The Status Sense Request interrupt can be disabled by using the DMA flag of CMR.

- **Single Sector Write (SSW)**

Single sector write is used to write 128 bytes of data on the disk. After the command is issued, the address search is performed. The remainder of the instruction's operation is shown in Figure 22.

- **Single Sector Write with Delete Data Mark (SWD)**

The operation flow of SWD is exactly like that of SSW. For SWD, the data pattern of the Data Address Mark becomes F8 instead of FB. The clock pattern remains C7.

- **Multi-Sector Commands (MSR/MSW)**

MSR is used for sequential reading of one or more sectors. If S sectors are to be read, S – 1 must be written into the GCR before the command is issued.

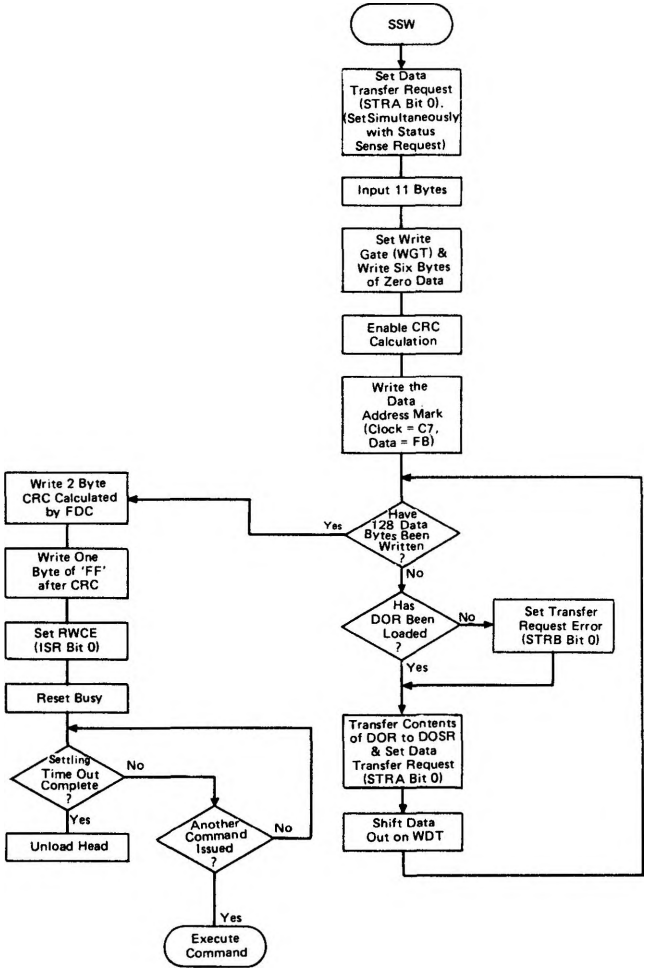


Figure 22 Operational Flow of the SSW Command

The basic operation for the MSR and MSW is the same as that for the SSR and SSW respectively. The basic operation begins with an address search operation, which is followed by a single sector read or write operation. This completes the operation on the first sector. The SAR is incremented, the GCR is decremented, and if no overflow is detected from the GCR (i.e., GCR become negative) the sequence is repeated until S number of sectors are read or written.

The completion of an MSR or MSW is like that of an SSR or SSW command. First RWCE is set and Busy is reset, after the settling time has expired, the head is released.

If a delete data mark is detected during an MSR command, STRA bit 1 (Delete Data Mark Detected) remains set throughout the commands operation.

When a multi-sector instruction is issued, the sum of the SAR and GCR must be less than 27. If SAR + GCR > 26, an address error (STRB bit 3 set) will occur after the contents of SAR becomes greater than 26.

- **Free Format Write (FFW)**

The FFW has two modes of operation which are selected by FWF (Free Format Write Flag) which is data bit 4 of the CMR.

When FWF = "0", the data bits of the DOR are written directly to the disk without first writing the preamble, address mark, etc. The contents of the DOR are FM modulated with a clock pattern of all ones.

If FWF = "1" the odd bits of the DOR are used as clock bits and even bits are used for data bits. In this mode, the DOSR clock is twice a normal write operation and one byte of DOR is one nibble (four bits of data) on the disk.

The two modes of the FFW command allow formatting a disk with either the IBM3470 format or a user defined format.

After the FFW command is loaded into the CMR, WGT becomes a "High" level, the contents of DOR are transferred to the DOSR, data transfer request (STRA bit 0) is set, and the serial bit pattern is shifted out on the WDT line. Therefore, DOR must be loaded before the FFW command is issued. Data from the DOR is continually transferred to the DOSR and shifted out on WDT until the CMR has been written with an all zero pattern. When CMR becomes zero, WGT becomes a "Low" level, but RWCE is not set and the R/W head is left in contact with the disk.

- **Free Format Read (FFR)**

FFR is used to input all data (including Address marks) from a disk. Once the FFR command is set into the CMR, the head is loaded and after the settling time has expired the serial data from the FDC is brought into the DISR. After 8 bits have accumulated, it is transferred to the DIR and Data Transfer Request (STRA bit 0) is set.

This operation continues until a zero pattern is stored in the CMR, terminating the FFR command. As in the case of the FFW command, RWCE is not set and the head remains in contact with the disk.

The first data that enters the DISR is not necessarily the first bit of a data word since the head may be lowered at any place on the disk. To prevent the FDC from remaining unsynchronized to the data, the FFR command will synchronize to an ID address mark (FE) or a Data Address mark (FB or F8) or an Index Address Mark (FC).

■ REGISTER DEFINITIONS

- **Data Output Register (DOR); Hex address 0, write only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8 Bits of Data Used for a Disk Write Operation							

When one of the four write macro commands (SSW, SWD, MSW, and FFW) is executed, the information contained in the DOR is loaded into the DOSR, and is shifted out on the WDT line using a double frequency (FM) format.

- **Data Input Register (DIR); Hex address 0, read only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8 Bits of Data Used for a Disk Read Operation							

One of the three read macro commands (SSR, MSR, FFR) executed, will cause the information on the RDT input to be clocked into the DISR. When 8 clock pulses have occurred, the 8 bits of information in the DISR are transferred to the DIR where it can be read by the bus interface.

- **Current Track Address (CTAR); Hex address 1, read/write**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Track Address of Current Head position							

The address of the track over which the R/W head is currently positioned is contained in the CTAR. At the end of a SEK command, the contents of the GCR are transferred to the CTAR. CTAR is cleared at the completion of a STZ command. CTAR is a read/write register so that the head position can be updated when several drives are connected to one FDC. Bit 7 is read as a "0".

- **Command Register (CMR); Hex address 2, write only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3*	Bit 2*	Bit 1*	Bit 0*
Function Interrupt Mask	ISR3 Interrupt Mask	DMA Flag	FWF	Macro Command			

*Bit 0 ~ 3 are cleared by $\overline{RES}$.

The commands that control the FDC are loaded into the lower four bits of the CMR. Information that controls the data transfer mode and interrupt conditions are loaded into bits four through seven.

Bit 0~Bit 3: Macro Command

The Macro Command to be executed by the FDC is written to bits 0~3.

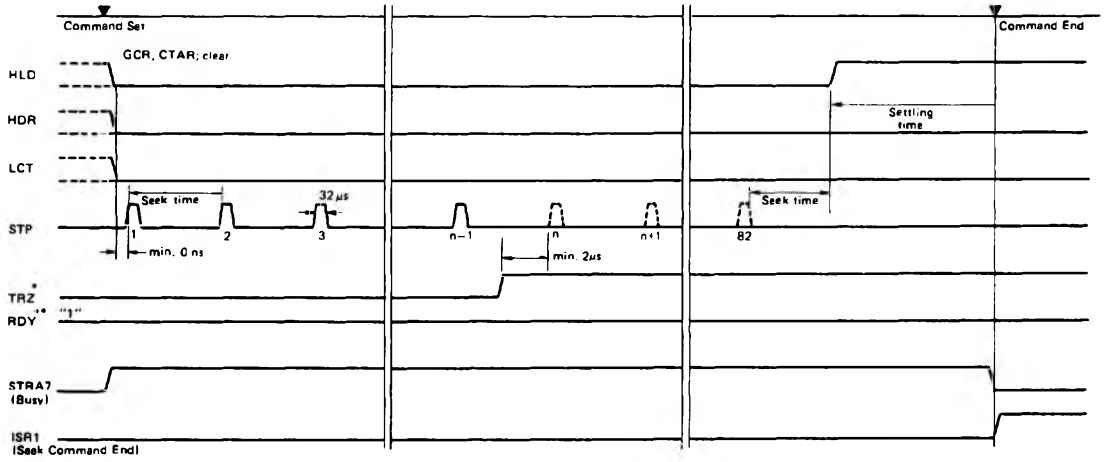
Bit 4: Free Format Write Flag (FWF)

If a Free Format Write command is issued, the state of bit 4 of the CMR determines what clock source will be used. The FWF is defined in the FFW (Free Format Write) command explanation.

Bit 5: DMA Flag

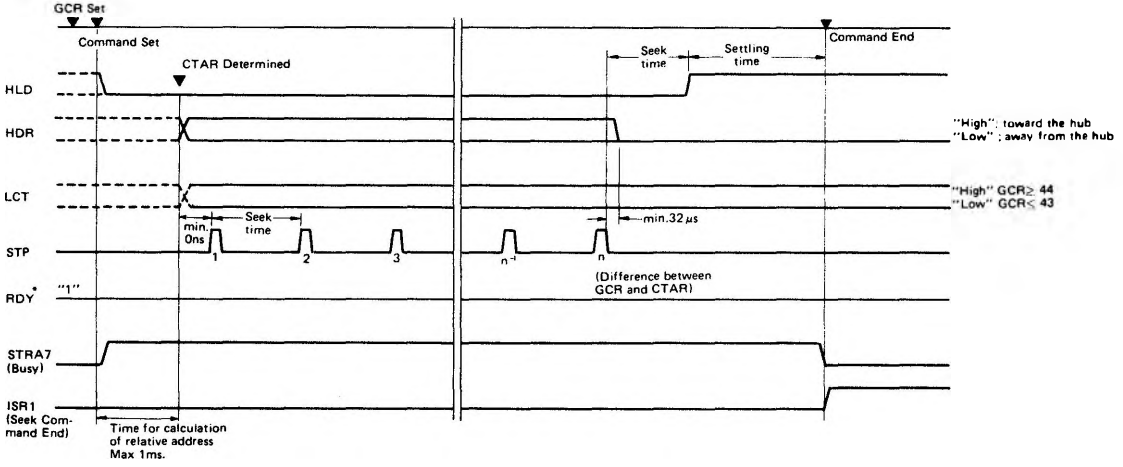
If bit 5 is a "1" the FDC is in the DMA mode. Bit 5 being a "1" inhibits setting of Status Sense Request (ISR bit 2) thereby preventing its associated interrupt. A logic "1" DMA flag also enables the TxRQ output allowing it to request DMA transfers when the Data Transfer Request flag (STRA bit 0) is set.

A logic "0" DMA flag indicates the program controlled I/O (PC I/O) mode.



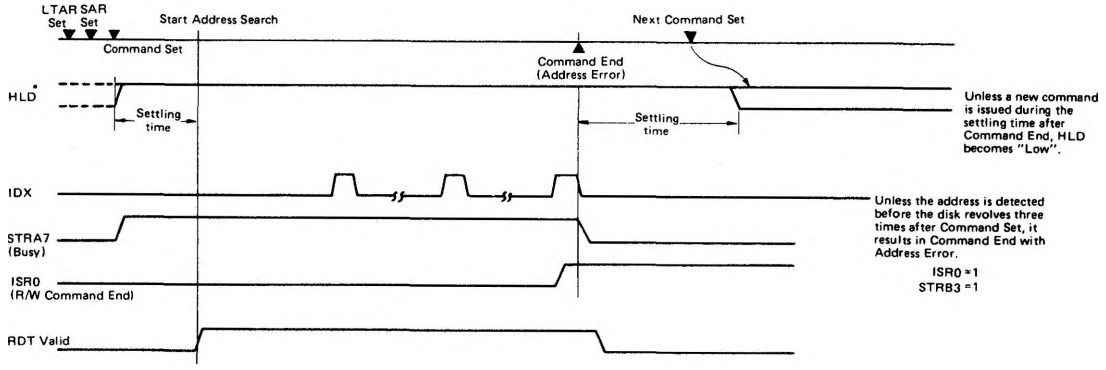
* STP output is masked when TRZ becomes "High". But if TRZ falls to "Low" again before 82 pulse outputs are all provided, STP output become available again from that time point.
** When RDY is "Low" with Command Set, the execution is postponed until RDY becomes "High".

Figure 23 Timing Sequence of STZ Command



* When RDY is "Low" with Command Set, the execution is postponed until RDY becomes "High"

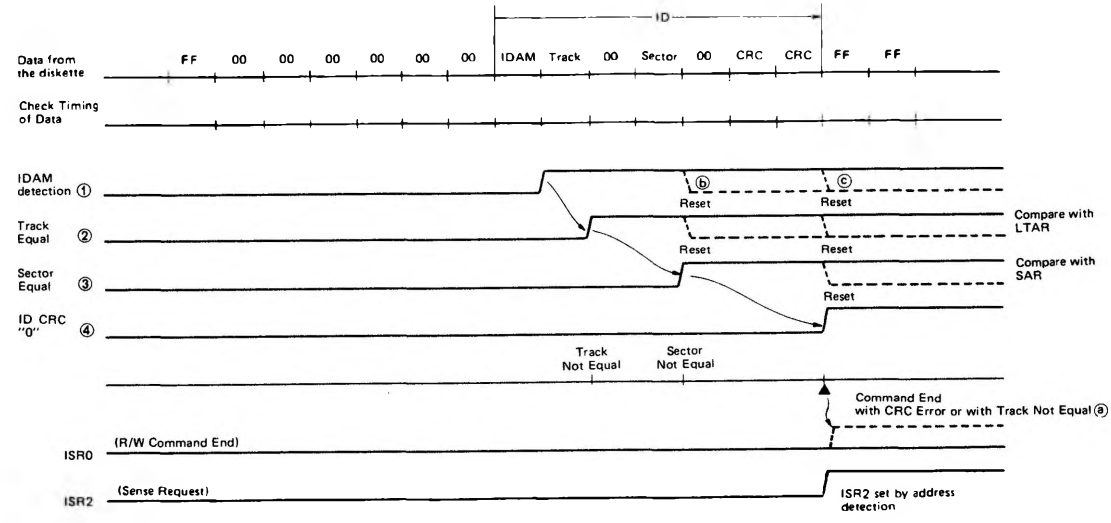
Figure 24 Timing Sequence of SEK Command



* If HLD has already been "High" when the command is set, the FDC starts the address search immediately.

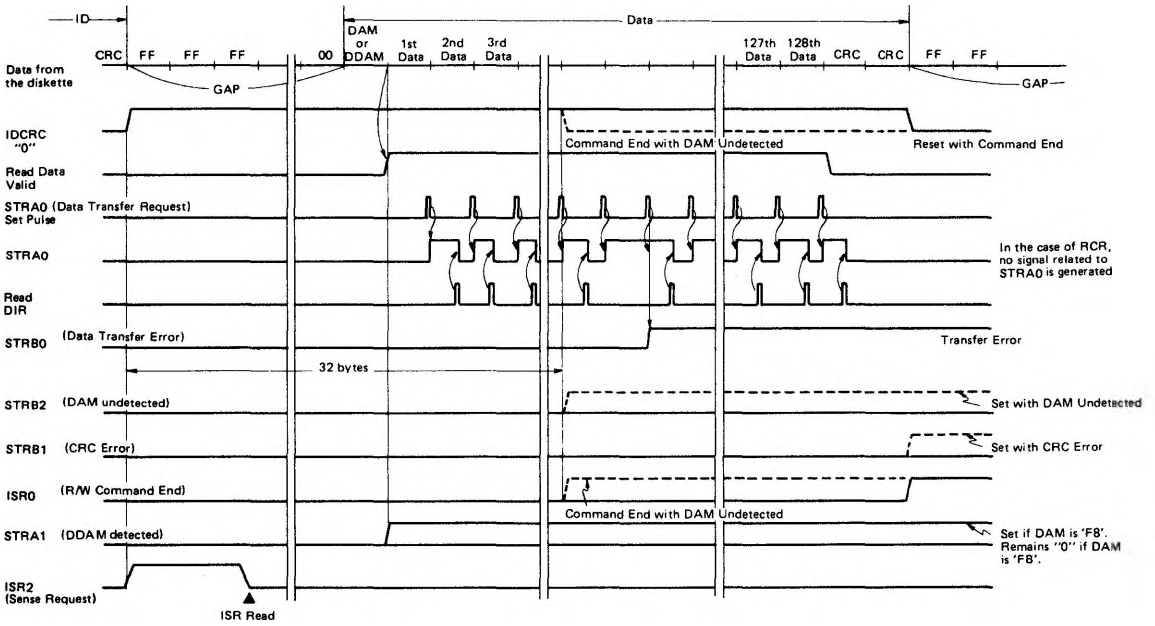
When RDY is "Low" with Command Set, the FDC waits for the execution until RDY becomes "High".

Figure 25 Timing Sequence of SSR, SSW, RCR, SWD, MSR, MSW Command (Relation with HLD and IDX)



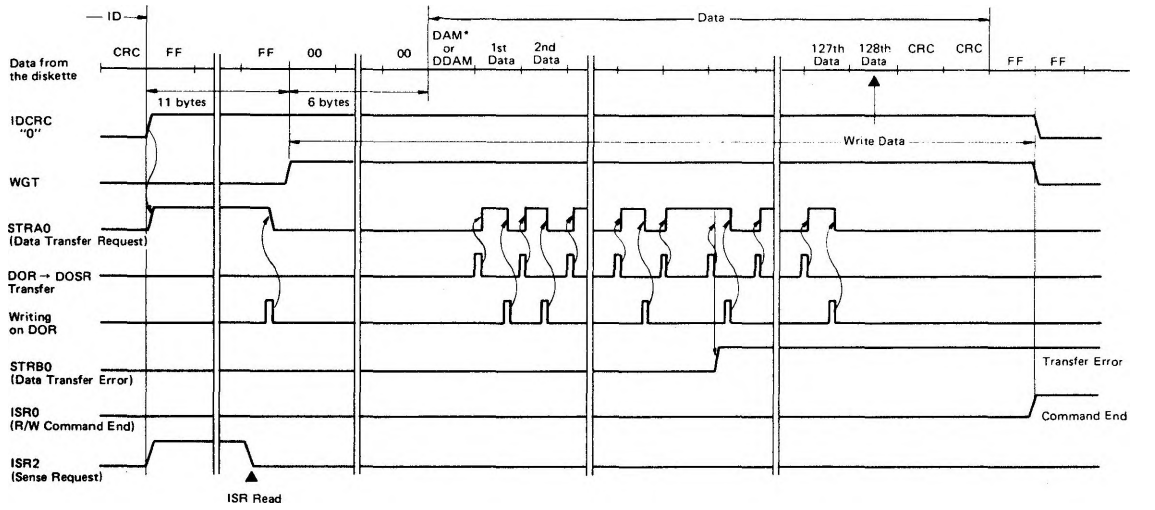
ⓐ ; In the case of Track Not Equal, ② is not set and if CRC equals to the one calculated by FDC, STRA5 is set.
ⓑ ; In the case of Sector Not Equal, ③ is not set and ① & ② are reset to search the next IDAM.
ⓒ ; In the case of CRC Error, ④ is not set and ①, ② & ③ are reset. (ISR0: Set, STRB1: Set, STRB3: Set)
When ①, ②, ③, & ④ are all set, ISR2 is Set. These four signals are reset with Command End.
When ④ is "1", go to the data transfer routine.

Figure 26 Internal Timing Sequence of Address Search Routine



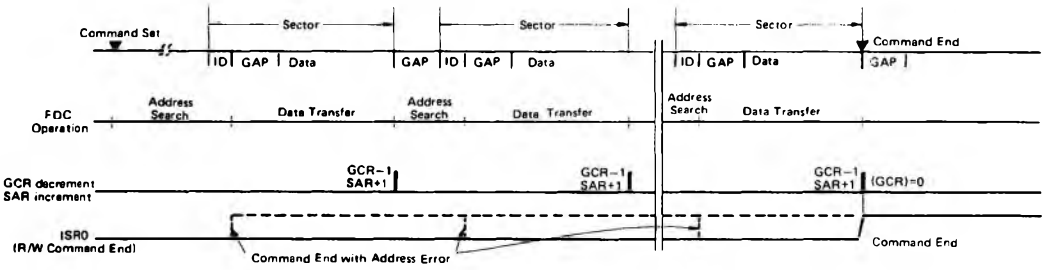
Unless DAM(FB) or DDAM(F8) is detected within 32 bytes after ID field has been detected, STRB2 is set to end the command.

Figure 27 Data Transfer Timing of SSR, RCR Command



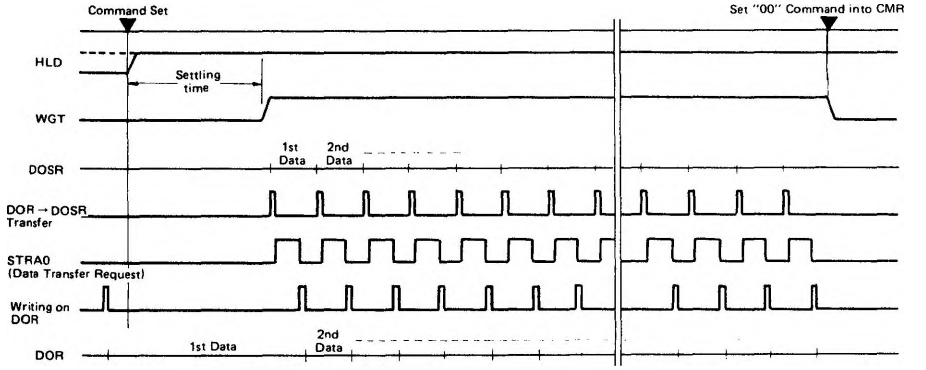
* As Data Address Mark, SSW command writes 'FB' and SWD command writes 'F8'.

Figure 28 Data Transfer Timing of SSW, SWD Command



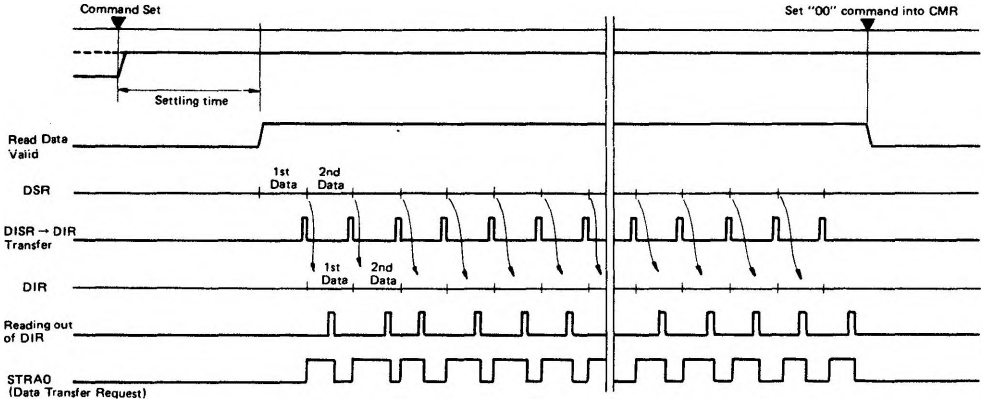
Address Search and Data Transfer in each sector is the same as those of SSR or SSW command.
When Address Error occurs, it results in Command End. If an error relating to Data Transfer occurs, Error flag is set. But the command continues to be executed to shift into the next sector.

Figure 29 Timing Sequence of MSR, MSW Command



- The first one-byte data must be set into DOR before Command Set.
- If HLD has already been "High" when the command is set, WGT becomes "High" immediately.
- When '00' command is set into CMR, an interrupt of Command End is not generated.

Figure 30 Timing Sequence of FFW Command



If HLD has already been "High" when the command is set, Read operation starts immediately without waiting for the settling time.
When "00" command is set into CMR, an interrupt of Command End is not generated.

Figure 31 Timing Sequence of FFR Command

Bit 6: ISR3 Interrupt Mask

CMR bit 6 (ISR3 Mask) is used to control the operation of ISR bit 3. A logic "1" in CMR bit 6 inhibits output of STRB-OR-Interrupt signal to $\overline{IRQ}$. If CMR bit 6 (ISR3 Mask) and CMR bit 7 are "0" STRB-OR-Interrupt signal will be output to $\overline{IRQ}$.

Bit 7: Function Interrupt Mask

When CMR bit 7 is a logic "1" all interrupts are inhibited.

Table 5

Causes of Interrupt	Command Register Masks That Affect Interrupts		
	CMR7 (Function Interrupt Mask)	CMR6 (ISR3 Mask)	CMR5 (DMA Flag)
ISR0 (Read write Command End)	M	x	x
ISR1 (Seek Command End)	M	x	x
ISR2 (Status Sense Request)	M	x	M
ISR3 (STRB-OR-Interrupt)	M	M	x

x = No effect
M = Bits that are used as masks

- **Interrupt Status Register (ISR); Hex address 2, read only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2*	Bit 1*	Bit 0*
Not Used (Read as "0")				STRB -OR	Status Sense Request	Seek Command End	Read Write Command End

* Cleared by $\overline{RES}$

Bit 0: Read Write Command End (RWCE)

When an SSR, RCR, SSW, SWD, MSR or MSW Macro Command has completed execution, bit 0 becomes set (logic "1"). If the function interrupts are enabled (bit 7 of CMR is a logic "0"), the conclusion of a Macro Command's execution will cause an interrupt.

Bit 1: Seek Command End (SCE)

Seek Command End is set on SEK and STZ commands to indicate the head has been loaded and the settling time specified in SUR has expired. Since RWCE is not set for the SEK or STZ command, SCE can be used as an interrupt to signify the SEK or STZ command has finished. SCE is not set for any of the R/W commands.

Bit 2: Status Sense Request

For an SSR, SSW, SWD, MSR, or MSW Command, Status Sense Request indicates that the specified address ID field has been detected and verified by a CRC check. This is used as an early indication that data transfers will occur after 18 more byte times. For MSR and MSW commands, it is set for each sector.

In the PC I/O mode, an interrupt occurs when Status Sense Request becomes a logic "1". In the DMA mode, (DMA flag of CMR is set) Status Sense Request is unchanged and does not generate an interrupt when the address ID field has been verified.

Bit 3: STRB-OR

STRB-OR is an "OR" of all of the bits of Status Register B.

$$\text{STRB-OR} = \text{STRB0} + \text{STRB1} + \text{STRB2} + \text{STRB3} + \text{STRB4} + \text{STRB5} + \text{STRB6} + \text{STRB7}$$

$$\text{STRB-OR-Interrupt} = \text{STRB1} + \text{STRB2} + \text{STRB3} + \text{STRB4} + \text{STRB5} + \text{STRB6} + \text{STRB7}$$

STRB-OR-Interrupt signal causes $\overline{IRQ}$. STRB-OR is read by Read ISR. STRB0 (Data Transfer Error) sets ISR Bit 3 but does not cause Interrupt.

ISR0, ISR1, and ISR2 are cleared when the Interrupt Status Register is read, but ISR3 is cleared only after Status Register B has been read except when FI input is "High".

- **Set-Up Register (SUR); Hex address 3, write only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Track to Track Seek Time				Head Settling Time			

The SUR is not affected by a reset operation; therefore, once it is initialized, the information remains until power is removed from the FDC.

Bit 0 ~ Bit 3: Head Settling Time

The head settling time is used to generate a delay after the head is placed in contact with the disk. This allows the head to stop bouncing before any operations are performed. The delay is programmed by bits 0~3 and is specified by the equation:

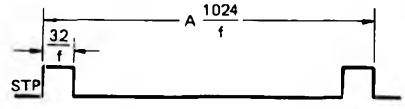
$$\text{Delay} = \frac{4096}{f} \cdot B$$

B = Number contained in bits 0~3 of SUR
f = Frequency of CLK input

For IBM3740 compatibility f = 1 MHz and the timing range is 4.096 ms for a "0001" to 61.44 ms for a "1111". A "0000" code prevents Settling Time complete from being set and the FDC must be Reset.

Bit 4 ~ Bit 7: Track to Track Seek Time

The frequency of STP is determined by bit 4~ bit 7 of SUR as shown below.



A = Number specified in bits 4~7 of SUR.
f = Frequency of CLK input.

For IBM compatible operation, f is 1 MHz. This results in an STP pulse width of 32 μs and an STP interval of 1.024 ms for a "0001" to 15.36 ms for a "1111".

- **Status Register A (STRA); Hex address 3, read only**

Bit 7*	Bit 6	Bit 5*	Bit 4	Bit 3	Bit 2	Bit 1*	Bit 0*
Busy	Index	Track Not Equal	Write Protect	Track Zero	Drive Ready	Delete Data Mark Detected	Data Transfer Request

* Cleared by $\overline{RES}$

Bit 0: Data Transfer Request

For a write operation (SSW, SWD, MSW, FFW) the transfer request bit indicates that the DOR is ready to accept the next data word to be written on the disk. If data is not written into the DOR before the last data bit in the DOSR is shifted out to the WDT line; the data transfer error bit (bit 0 of STRB) will be set. After a write command has been issued, the first transfer request occurs simultaneously with the Status Sense Request. For a write operation, transfer request is reset after the DOR has been written from the data bus.

During a read operation (SSR, MSR, FFR) the transfer request bit signifies data from the DISR has been transferred to the DIR. The DIR must be read before the DISR is full again or the data transfer error bit (bit 0 of STRB) will be set. For read operations, transfer request is reset by a read of the DIR.

Bit 1: Delete Data Mark Detected

A Single Sector Read operation that detects a delete data code (F8) instead of a general data code (FB) as a Data Address Mark will set the Delete Data Mark Detected bit. For the MSR command, bit 1 is set the first time an "F8" code is found and remains set throughout the execution of the command. Bit 1 is reset whenever an SSR, SSW, SWD, MSR, MSW, or RCR command is issued.

Bit 2: Drive Ready

The Drive Ready bit indicates the state of the Ready input from the floppy disk drive. If a command is issued with Ready at logic "0", its execution will be inhibited until Ready becomes a logic "1". If ready becomes a "0" during the execution of a command the Hard Error Flag (STRB bit 7) is set.

Bit 3: Track Zero

The state of the Track Zero input from the floppy disk drive is reflected in this bit of STRA. A logic "1" on the Track Zero input inhibits step pulses during an STZ command.

Bit 4: Write Protect

The Write Protect input from the floppy disk drive is reflected by bit 4 of STRA. A "High" level (logic "1") on the WPT input during the execution of any write command results in a write error (bit 6 of STRB set).

Bit 5: Track Not Equal

If the track address read from the address ID field does not coincide with the address in the LTAR inspite of CRC matching the one calculated by FDC, the Track Not Equal bit is set. Track Not Equal applies to all non-free format read/write commands, and is reset after a non-free format read/write command is issued.

Bit 6: Index

The state of the index input appears in bit 6 of STRA. The index input is used to count the number of disk revolutions while the FDC is looking for the address ID field (see operation of STRB bit 3) during the address search phase of a non-free format read/write command.

Bit 7: Busy

When Busy is a logic "1", the FDC is executing a command and no new commands can be issued. Busy should be confirmed to be "0" before reading ISR or STRB as well as issuing a command.

- **Sector Address Register (SAR); Hex address 4, write only**

Bit 7	Bit 6	Bit 5	Bit 4*	Bit 3*	Bit 2*	Bit 1*	Bit 0*
Not Used			5 Bit Sector Address				

* Cleared by $\overline{RES}$

Before a data transfer macro command (SSW, SWD, SSR, RCR, MSW, MSR) is issued, the address of the sector on which the operation is to be performed must be written into the SAR. The address in the sector address byte of an Address ID field of the disk is compared with the contents of the SAR. During an MSW or MSR command, the SAR is incremented after each sector is read or written. When execution is complete, the SAR contains the address of the last sector on which an operation was performed plus one.

- **Status Register B(STRB); Hex address 4, read only**

Bit 7*	Bit 6*	Bit 5	Bit 4*	Bit 3*	Bit 2*	Bit 1*	Bit 0*
Hard Error	Write Error	File Inoperable	Seek Error	Sector Address Undetected	Data Mark Undetected	CRC Error	Data Transfer Error

* Cleared by $\overline{RES}$

The bits of the STRB represent possible error conditions that may occur during execution of macro commands. Whenever STRB is reset, ISR bit 3 is also reset.

Bit 0: Data Transfer Error

Data Transfer Error indicates an underflow or overflow of data. If a Write operation is being performed, it signifies that data was not presented to the DOR before the DOSR became empty. In this case, the current contents of the DOR are transferred to the DOSR and the write operation continues. The data transfer error remains set until STRB is read, and the data transfer request remains set until data is written into the DOR. The operation of the CRC is unchanged.

For read commands, a data transfer error indicates that data in the DIR was not read before the next data word from the disk was transferred to the DIR. The read operation continues until sufficient data has been read from the disk to satisfy the requirements of the command (128 bytes for SSR). The error indication remains set until STRB is read, and the transfer request remains set until data is read from the DIR.

Bit 1: CRC Error

A CRC error occurs when the CRC read from the disk does not match that calculated by the FDC on the data it reads from the disk. A CRC error can occur in two different situations; checking the address ID field, checking the data field.

If the CRC error occurs during the check of an address ID field, Sector Address Undetected (STRB bit 3) will also be indicated (see Table 6). A CRC error of a data field is indicated by a CRC Error and no Sector Address Undetected.

Bit 2: Data Mark Undetected

If a valid data mark is not detected in the data block of a sector, it is indicated by a Data Mark Undetected error.

Bit 3: Sector Address Undetected

The Sector Address Undetected bit can be set on two conditions; not finding the sector address and a CRC error on an address ID field.

If the disk makes three revolutions during an address search operation and the sector address specified in the sector address register is not found in any of the address ID fields, a Sector Address Undetected condition is indicated.

A CRC error that occurs on an address ID field will set bit 3 also. Table 6 shows how bits 1 and 3 are related.

Table 6 Relationship of CRC Error and Sector Address Undetected

CRC Error (STRB1)	Sector Address Undetected (STRB3)	Condition
0	0	No Error
0	1	Sector Address not Detected
1	0	CRC Error on a Data Field
1	1	CRC Error on Address ID Field

Bit 4: Seek Error

An STZ (Seek Track Zero) command that never receives a track zero indication on the track zero input will result in a Seek Error (see description of STZ command).

Bit 5: File Inoperable

The state of the File Inoperable input appears in bit 5. If the File Inoperable input is a "High" level, a pulse of width equals to Enable pulse width PW_{EL} is issued on the FIR output when STRB is read. FI is not latched but the input is gated to the bus when STRB is read.

Bit 6: Write Error

If the WPT input becomes a "High" level (logic "1") during the execution of a write command the Write Error bit is set.

Bit 7: Hard Error

If the Ready input becomes a "Low" level during the operation of a command (Busy is set), a Hard Error indication will result.

- **General Count Register (GCR); Hex address 5, write only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	7 Bit Count for Track Number on SEK Command and Sector Count for MSR or MSW Command						

The GCR contains the destination track address for the R/W head on an SEK Macro Command. The contents of the GCR are transferred to the CTAR at the end of the SEK Command. For multi-sector read or write operations (MSR, MSW), the GCR contains the number of sectors to be read minus one. During the MSR or MSW execution the GCR is decremented after each sector is read or written.

- **CRC Control Register (CCR) ; Hex address 6, write only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used						Shift CRC	CRC Enable

The CCR information is used only in the free format commands; for all other commands this register is masked and has no function.

Bit 0: CRC Enable

During an FFW command, CRC Enable is set by software and CRC generation takes effect on the next transfer of data from DOR to DOSR (see figure 32). The CRC generation continues until Shift CRC (CCR bit 1) is set.

For an FFR command, CRC Enable is set by software and CRC generation takes effect on the next data read from DIR. The calculation continues for all data bytes read from DIR until CRC Enable is reset. The bytes read previous to resetting CRC Enable are considered the CRC information bytes and the CRC check is made against them.

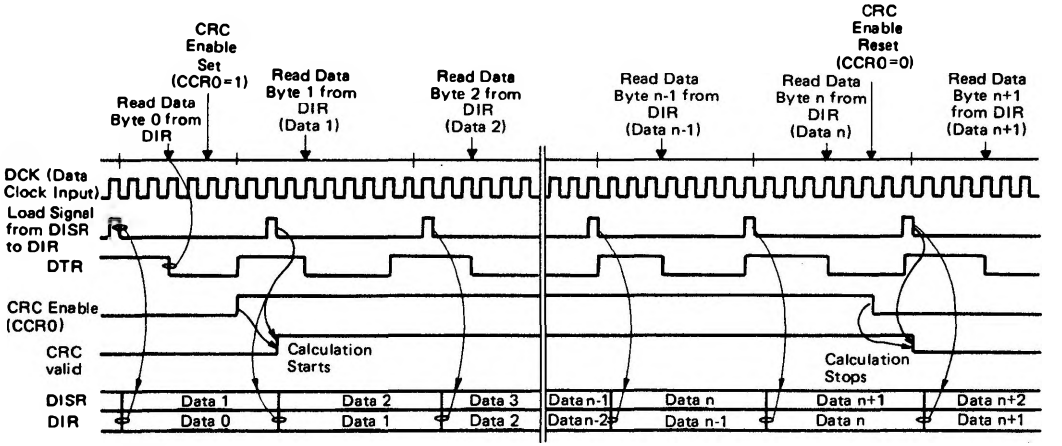
Bit 1: Shift CRC

Bit 1 is valid only for the FFW command. After setting, it takes effect on the next transfer of data from DOR to DOSR (see Figure 33). Setting Shift CRC terminates the CRC calculation and causes the CRC calculated on all the data written into DOR up to the setting of bit 1, to be shifted out the WDT output. The CRC calculation will not include any data written to DOR after Shift CRC is set.

- **LTAR (Logical Track Address); Hex address 7, write only**

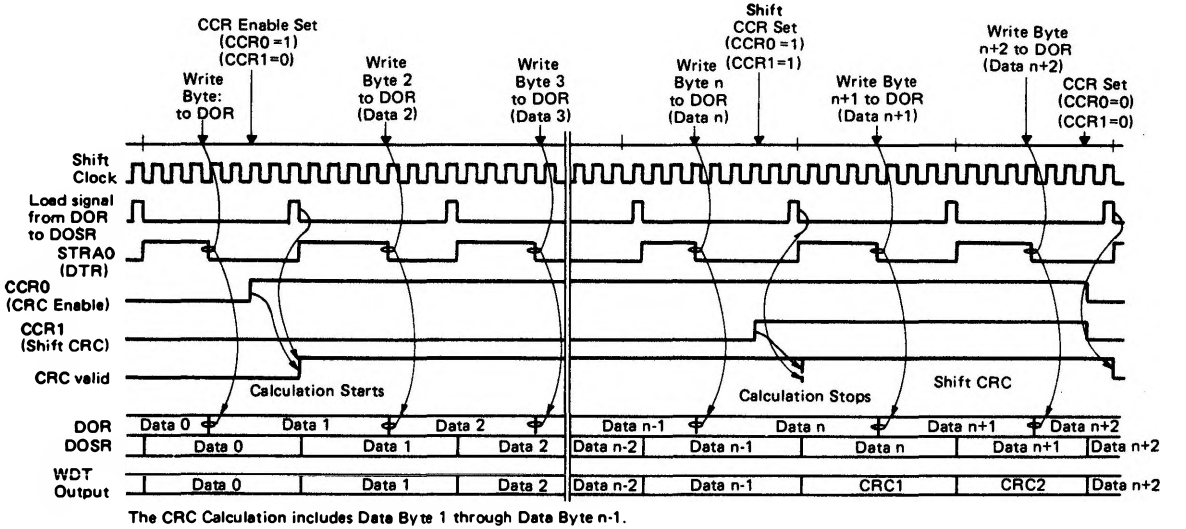
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	7 Bit Logical Track Address						

When a read or write macro command (SSW, SWD, SSR, RCR, MSW, MSR) is issued, the address of the track on which the operation is to be performed must be written into the LTAR. The address in the track address byte of an Address ID field of the disk is compared with the contents of the LTAR. The contents of LTAR are not affected by the execution of any of the commands.



CRC Calculation includes Data Byte 1 through Data Byte n.

Figure 32 CCR Control Register Timing for an FFR Command (READ)



The CRC Calculation includes Data Byte 1 through Data Byte n-1.

Figure 33 CCR Control Register Timing for an FFW Command (WRITE)

Table 7 Programming Reference Data

Table 7 is a summary of the information in the data sheet and can be used as a reference when programming the HD6843.

Registers	Hex Address	R/W Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR	0	WO	8 Bits of Data Used for a Disk Write Operation							
DIR	0	RO	8 Bits of Data Used for a Disk Read Operation							
CTAR	1	R/W	Track Address of Current Head Position							
CMR	2	WO	Function Interrupt Mask	ISR3 Interrupt Mask	DMA Flag	FWF	Macro Command			
ISR	2	RO	Not Used				STRB -OR	Status Sense Request	Seek Command End	Read Write Command End
SUR	3	WO	Track to Track Seek Time				Head Settling Time			
STRA	3	RO	Busy	Index	Track Not Equal	Write Protect	Track Zero	Drive Ready	Delete Data Mark Detected	Data Transfer Request
SAR	4	WO	Not Used			5 Bit Sector Address				
STRB	4	RO	Hard Error	Write Error	File Inoperable	Seek Error	Sector Address Undetected	Data Mark Undetected	CRC Error	Data Transfer Error
GCR	5	WO	Not Used	7 Bit Count for Track Number on SEK or Sector Count for MSR or MSW.						
CCR	6	WO	Not Used						Shift CRC	CRC Enable
LTAR	7	WO	Not Used	7 Bit Logical Track Address						

RO – Read Only
WO – Write Only
R/W – Read/Write

* Cleared by $\overline{RES}$

MACRO COMMANDS

Hex Code	Instruction	Hex Code	Instruction
2	STZ	A	FFR
3	SEK	B	FFW
4	SSR	C	MSR
5	SSW	D	MSW
6	RCR		
7	SWD		

Table 8 Error Condition, Command Execution, Interrupt, and Head Control

Error	Flag	Set Condition	Reset Condition	Command	Command Execution	Interrupt	Head Control
Track Not Equal	STRA5	Track information of ID field is not equal to the content of LTAR.	Issuing of SSR, RCR, MSR, SSW, SWD or MSW Command	SSR, RCR, MSR SSW, SWD, MSW	The execution of a command is interrupted and R/W Command End (ISR0) is set.	Request (ISR0)	Unchanged**
Data Transfer Error	STRB0	Overrun or underflow during the data transfer	Reading of STRB	SSR, MSR, SSW, SWD, MSW, FFR FFW	Read/Write command continues to be executed.	No interrupt	Unchanged**
CRC Error	STRB1	CRC Error on ID field or Date field	Reading of STRB	SSR, RCR, MSR, SSW, SWD, MSW (FFR)	The execution of a command is interrupted and R/W Command End (ISR0) is set.	Request (ISR0, ISR3)	Unchanged**
Data Mark Undetected	STRB2	DAM or DDAM is undetected within 32 bytes after ID field has been detected.	Reading of STRB	SSR, RCR, MSR	The execution of a command is interrupted and R/W Command End (ISR0) is set.	Request (ISR0, ISR3)	Unchanged**
Sector Address Undetected	STRB3	(1) Sector Address of ID field is not equal to the content of SAR. (2) CRC Error on ID field	Reading of STRB after Busy (STRA7) is reset.	SSR, RCR, MSR SSW, SWD, MSW	The execution of a command is interrupted and R/W Command End (ISR0) is set.	Request (ISR0, ISR3)	Unchanged (Head remains loaded after settling time has expired.)
Seek Error	STRB4	TRZ signal semains "Low" level though eighty-two STP pulse outputs are provided in STZ command.	Reading of STRB	STZ	The execution of a command is interrupted and Seek Command End (ISR1) is set.	Request (ISR1, ISR3)	Unchanged
File Inoperable	STRB5	A "High" level input of FI terminal is reflected.	FI signal of the FDD is reset when "High" pulse output is provided by reading of STRB at FI="1".	All commands	The execution of a command is interrupted. If it is a Read/Write command, ISR0 is set. If it is a seek command, ISR1 is set.	Request (ISR0 or ISR1, ISR3)	Unload the head imediately (HLD="Low") Set WGT to "Low"
Write Error	STRB6	Write operation (WGT="High") is performed when the input of WPT terminal is "High" level.	Reading of STRB	SSW, SWD, MSW FFW	The execution of a command is interrupted and R/W Command End (ISR0) is set.	Request (ISR0, ISR3)	Unload the head imediately (HLD="Low" Set WGT to "Low"
Hard Error	STRB7	RDY input signal becomes "Low" level during the execution of a command (Busy="1".)	Reading of STRB	All commands	The execution of a command is interrupted. If it is a Read/Write command, ISR0 is set. If it is a seek command, ISR1 is set.	Request (ISR0 or ISR1, ISR3)	Unload the head imediately (HLD="Low") Set WGT to "Low"
Not Ready during the idling	STRA2	–	–	–	–	No interrupt	Unload the head imediately (HLD="Low")

* These errors except STRB5 and STRA2 are reset by $\overline{RES}$ inputs.

** Head is unloaded if the new command is not issued during the settling time after Read/Write command ends.