HFA1106

315MHz, Low Power, Video Operational Amplifier with Compensation Pin

September 1998

Features

- **Compensation Pin for Bandwidth Limiting**
- **Lower Lot-to-Lot Variability With External Compensation**
- **High Input Impedance 1MΩ**
- **Differential Gain 0.02%**
- **Differential Phase . . . . . 0.05 Degrees**
- **Wide -3dB Bandwidth 315MHz**
- **Very Fast Slew Rate 700V/μs**
- **Low Supply Current 5.8mA**
- **Gain Flatness (to 100MHz) . . . . . ±0.1dB**

Applications

- **Noise Critical Applications**
- **Professional Video Processing**
- **Medical Imaging**
- **Video Digitizing Boards/Systems**
- **Radar/IF Processing**
- **Hand Held and Miniaturized RF Equipment**
- **Battery Powered Communications**
- **Flash A/D Drivers**
- **Oscilloscopes and Analyzers**

Description

The HFA1106 is a high speed, low power current feedback operational amplifier built with Intersil's proprietary complementary bipolar UHF-1 process. This amplifier features a compensation pin connected to the internal high impedance node, which allows for implementation of external clamping or bandwidth limiting.

Bandwidth limiting is accomplished by connecting a capacitor (C_{COMP}) and series damping resistor (R_{COMP}) from pin 8 to ground. Amplifier performance for various values of C_{COMP} is documented in the Electrical Specifications.

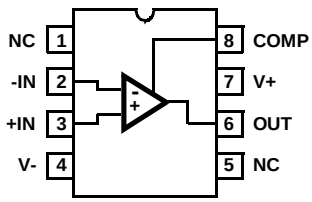
The HFA1106 is ideal for noise critical wideband applications. Not only can the bandwidth be limited to minimize broadband noise, the HFA1106 is optimized for lower feedback resistors (R_F = 100Ω for A_V = +2) than most current feedback amplifiers. The low feedback resistor reduces the inverting input noise current contribution to total output noise, while reducing DC errors as well. Please see the "Application Information" section for details.

Part Number Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1106IP	-40 to 85	8 Ld PDIP	E8.3
HFA1106IB (H1106I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1106
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 1) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating . . . . . >600V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Die Only) . . . . . 175^{o}C
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability; however, continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $C_{COMP} = 0pF$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	$\mu V/^{o}C$
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	47	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	$nA/^{o}C$
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	0.8	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	$nA/^{o}C$
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	4	8	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $C_{COMP} = 0pF$, $R_L = 100\Omega$, Unless Otherwise Specified **(Contin-**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Inverting Input Resistance		C	25	-	60	-	Ω
Input Capacitance		C	25	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS Tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	$A_V = -1$	C	25	-	500	-	kΩ
AC CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($A_V = +1$, $R_F = 150\Omega$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	250	315	-	MHz
	$C_C = 2pF$	B	25	140	170	-	MHz
	$C_C = 5pF$	B	25	65	80	-	MHz
-3dB Bandwidth ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	185	245	-	MHz
	$C_C = 2pF$	B	25	110	140	-	MHz
	$C_C = 5pF$	B	25	55	70	-	MHz
±0.1dB Flat Bandwidth ($A_V = +1$, $R_F = 150\Omega$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	45	65	-	MHz
	$C_C = 2pF$	B	25	25	40	-	MHz
	$C_C = 5pF$	B	25	13	17	-	MHz
±0.1dB Flat Bandwidth ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	$C_C = 0pF$	B	25	60	100	-	MHz
	$C_C = 2pF$	B	25	15	30	-	MHz
	$C_C = 5pF$	B	25	11	14	-	MHz
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
Output Voltage Swing	$A_V = -1$, $R_F = 510\Omega$	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current	$A_V = -1$, $R_L = 50\Omega$, $R_F = 510\Omega$	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Closed Loop Output Impedance	DC	B	25	-	0.07	-	Ω
Output Short Circuit Current	$A_V = -1$	B	25	-	90	-	mA
Second Harmonic Distortion (10MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-45	-53	-	dBc
	$C_C = 2pF$	B	25	-42	-48	-	dBc
	$C_C = 5pF$	B	25	-38	-44	-	dBc
Third Harmonic Distortion (10MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-50	-57	-	dBc
	$C_C = 2pF$	B	25	-48	-56	-	dBc
	$C_C = 5pF$	B	25	-48	-56	-	dBc
Second Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-42	-46	-	dBc
	$C_C = 2pF$	B	25	-38	-42	-	dBc
	$C_C = 5pF$	B	25	-34	-38	-	dBc
Third Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$)	$C_C = 0pF$	B	25	-46	-57	-	dBc
	$C_C = 2pF$	B	25	-52	-57	-	dBc
	$C_C = 5pF$	B	25	-50	-57	-	dBc

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $C_{COMP} = 0pF$, $R_L = 100\Omega$, Unless Otherwise Specified **(Contin-**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$, $A_V = +1$, $R_F = 150\Omega$)	$C_C = 0pF$	B	25	-	2.6	2.9	ns
	$C_C = 2pF$	B	25	-	3.7	4.2	ns
	$C_C = 5pF$	B	25	-	5.2	6.2	ns
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$, $A_V = +2$)	$C_C = 0pF$	B	25	-	2.7	3.2	ns
	$C_C = 2pF$	B	25	-	3.9	4.4	ns
	$C_C = 5pF$	B	25	-	5.9	6.9	ns
Overshoot (Note 4) ($A_V = +1$, $R_F = 150\Omega$, V_{IN} $t_{RISE} = 2.5ns$)	$V_{OUT} = 250mV_{P-P}$	B	25	-	1.5	4	%
	$V_{OUT} = 2V_{P-P}$	B	25	-	6	10	%
	$V_{OUT} = 0V$ to $2V$	B	25	-	4	7.5	%
Overshoot (Note 4) ($A_V = +2$, V_{IN} $t_{RISE} = 2.5ns$)	$V_{OUT} = 250mV_{P-P}$	B	25	-	2	5	%
	$V_{OUT} = 2V_{P-P}$	B	25	-	6.5	12	%
	$V_{OUT} = 0V$ to $2V$	B	25	-	2.5	7.5	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $R_F = 150\Omega$)	+SR, $C_C = 0pF$	B	25	580	680	-	V/µs
	-SR, $C_C = 0pF$	B	25	400	545	-	V/µs
	+SR, $C_C = 2pF$	B	25	470	530	-	V/µs
	-SR, $C_C = 2pF$	B	25	300	410	-	V/µs
	+SR, $C_C = 5pF$	B	25	320	365	-	V/µs
	-SR, $C_C = 5pF$	B	25	200	300	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	+SR, $C_C = 0pF$	B	25	750	910	-	V/µs
	-SR, $C_C = 0pF$	B	25	500	720	-	V/µs
	+SR, $C_C = 2pF$	B	25	550	730	-	V/µs
	-SR, $C_C = 2pF$	B	25	350	520	-	V/µs
	+SR, $C_C = 5pF$	B	25	380	485	-	V/µs
	-SR, $C_C = 5pF$	B	25	250	375	-	V/µs
Settling Time ($V_{OUT} = +2V$ to $0V$ Step, $C_C = 0pF$ to $5pF$)	To 0.1%	B	25	-	26	35	ns
	To 0.05%	B	25	-	33	43	ns
	To 0.02%	B	25	-	49	75	ns
Overdrive Recovery Time	$V_{IN} = \pm2V$	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
Differential Gain ($f = 3.58MHz$, $R_L = 150\Omega$)	$C_C = 0pF$	B	25	-	0.02	-	%
	$C_C = 5pF$	B	25	-	0.02	-	%
Differential Phase ($f = 3.58MHz$, $R_L = 150\Omega$)	$C_C = 0pF$	B	25	-	0.05	-	Degrees
	$C_C = 5pF$	B	25	-	0.07	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current		A	25	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTES:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. Undershoot dominates for output signal swings below GND (e.g. $2V_{P-P}$) yielding a higher overshoot limit compared to the $V_{OUT} = 0V$ to $2V$ condition.

Application Information

Optimum Feedback Resistor

All current feedback amplifiers (CFAs) require a feedback resistor (R_F) even for unity gain applications, and R_F in conjunction with the internal compensation capacitor sets the dominant pole of the frequency response. Thus the amplifier's bandwidth is inversely proportional to R_F. The HFA1106 design is optimized for $R_F = 150\Omega$ at a gain of +1. Decreasing R_F decreases stability resulting in excessive peaking and overshoot - Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies. At higher gains, however, the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth (e.g., $R_F = 100\Omega$ for $A_V = +2$).

Why Use Externally Compensated Amplifiers?

Externally compensated op amps were originally developed to allow operation at gains below the amplifier's minimum stable gain. This enabled development of non-unity gain stable op amps with very high bandwidth and slew rates. Users needing lower closed loop gains could stabilize the amplifier with external compensation if the associated performance decrease was tolerable.

With the advent of CFAs, unity gain stability and high performance are no longer mutually exclusive, so why offer unity gain stable op amps with compensation pins?

The main reason for external compensation is to allow users to tailor the amplifier's performance to their specific system needs. Bandwidth can be limited to the exact value required, thereby eliminating excess bandwidth and its associated noise. A compensated op amp is also more predictable; lower lot-to-lot variation requires less system overdesign to cover process variability. Finally, access to the internal high impedance node allows users to implement external output limiting or allows for stabilizing the amplifier when driving large capacitive loads.

Noise Advantages - Uncompensated

The HFA1106 delivers lower broadband noise even without an external compensation capacitor. Package capacitance present at the Comp pin stabilizes the op amp, so lower value feedback resistors can be used. A smaller value R_F minimizes the noise voltage contribution of the amplifier's inverting input noise current - $I_{NI} \times R_F$, usually a large contributor on CFAs - and minimizes the resistor's thermal noise contribution ($4KTR_F$). Figure 1 details the HFA1105 broadband noise performance in its recommended configuration of $A_V = +2$, and $R_F = 510\Omega$. Adding a Comp pin to the HFA1105 (thereby creating the HFA1106) yields the 23% noise reduction shown in Figure 2. In both cases, the scope bandwidth, 100MHz, limits the measurement range to prevent amplifier bandwidth differences from affecting the results.

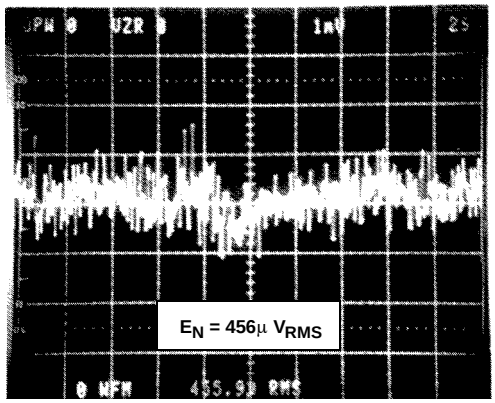


FIGURE 1. HFA1105 NOISE PERFORMANCE, $A_V = +2$, $R_F = 510\Omega$

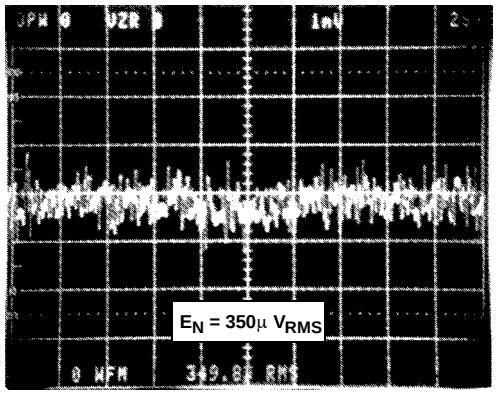


FIGURE 2. HFA1106 NOISE PERFORMANCE, UNCOMPENSATED, $A_V = +2$, $R_F = 100\Omega$

Offset Advantage

An added advantage of the lower value R_F is a smaller DC output offset. The op amp's inverting input bias current (I_{BI}) flows through the feedback resistor and generates an offset voltage error defined by:

$$V_E = I_{BI} \times R_F; \text{ and } V_{OS} = A_V (\pm V_{IO}) \pm V_E$$

Reducing R_F reduces these errors.

Bandwidth Limiting

The HFA1106 bandwidth may be limited by connecting a resistor, R_{COMP} (required to damp the interaction between the compensation capacitor and the package parasitics), and capacitor, C_{COMP} , in series from pin 8 to GND. Typical performance characteristics for various C_{COMP} values are listed in the specification table. The HFA1106 is already unity gain stable, so the main reason for limiting the bandwidth is to reduce the broadband noise.

Noise Advantages - Compensated

System noise reduction is maximized by limiting the op amp to the bandwidth required for the application. Noise increases as the square root of the bandwidth increase (4x bandwidth increase yields 2x noise increase), so eliminating excess

bandwidth significantly reduces system noise. Figure 3 illustrates the noise performance of the HFA1106 with its bandwidth limited to 40MHz by a 10pF C_{COMP}. As expected the noise decreases by approximately 37% (100% x (1-$\sqrt{40MHz/100MHz}$)) compared with Figure 2. The decrease is an even more dramatic 48% versus the HFA1105 noise level in Figure 1.

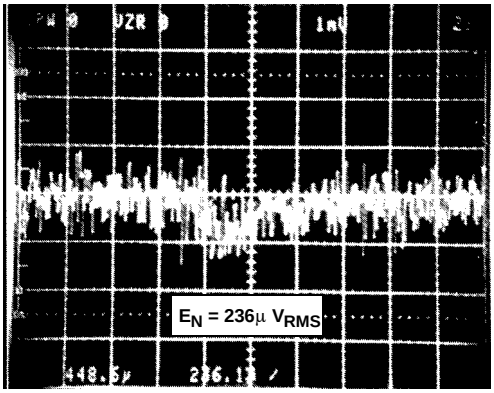


FIGURE 3. HFA1106 NOISE PERFORMANCE, COMPENSATED, A_V = +2, R_F = 100Ω, C_C = 10pF

Additionally, compensating the HFA1106 allows the use of a lower value R_F for a given gain. The decreased bandwidth due to C_{COMP} keeps the amplifier stable by offsetting the increased bandwidth from the lower R_F. As noted previously, a lower value R_F provides the double benefit of reduced DC errors and lower total noise.

Less Lot-to-Lot Variability

External compensation provides another advantage by allowing designers to set the op amp's performance with a precision external component. On-chip compensation capacitors can vary by 10-20% over the process extremes. A precise external capacitor dominates the on-chip compensation for consistent lot-to-lot performance and more robust designs. Compensating high frequency amplifiers to lower bandwidths can simplify design tasks and ensure long term manufacturability.

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, compensated for by increasing C_{COMP}, or isolated by a series output resistor.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

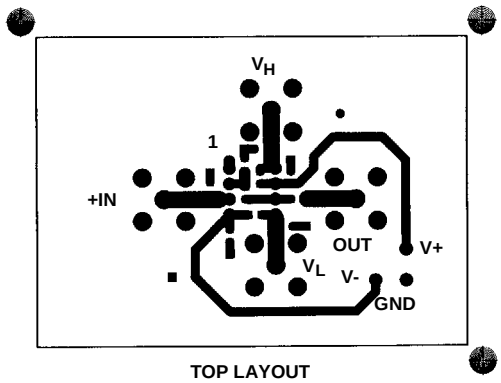
An example of a good high frequency layout is the Evaluation Board shown in Figure 4.

Evaluation Board

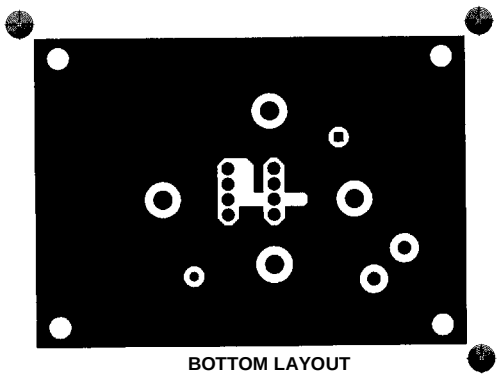
The performance of the HFA1106 may be evaluated using the HFA11XX Evaluation Board.

Figure 4 details the evaluation board layout and schematic. Connecting R_{COMP} and C_{COMP} in series from socket pin 8 to the GND plane compensates the op amp. Cutting the trace from pin 8 to the V_H connector removes the stray parallel capacitance, which would otherwise affect the evaluation. Additionally, the 500Ω feedback and gain setting resistors should be changed to the proper value for the gain being evaluated.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.



TOP LAYOUT



BOTTOM LAYOUT

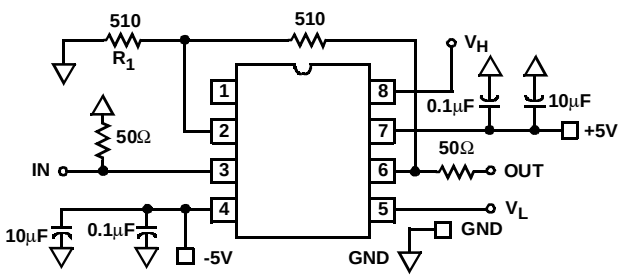


FIGURE 4. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

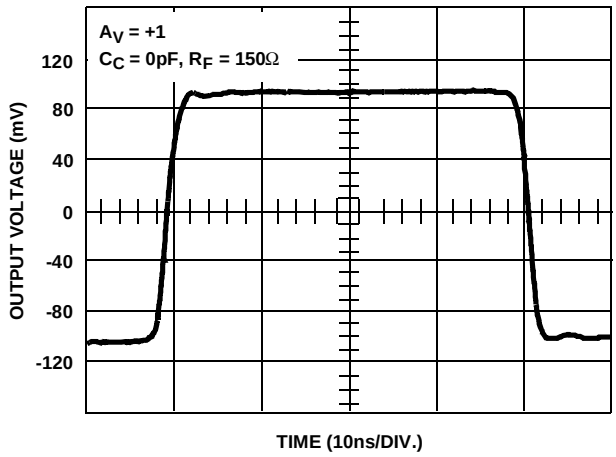


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

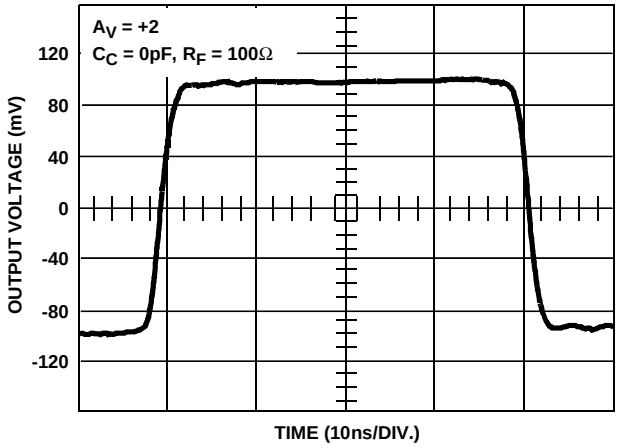


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

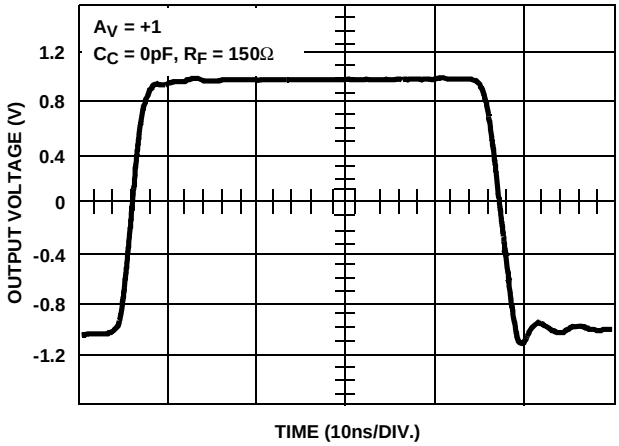


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

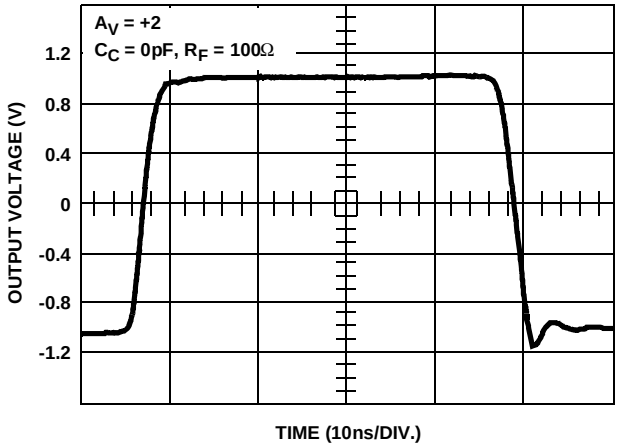


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

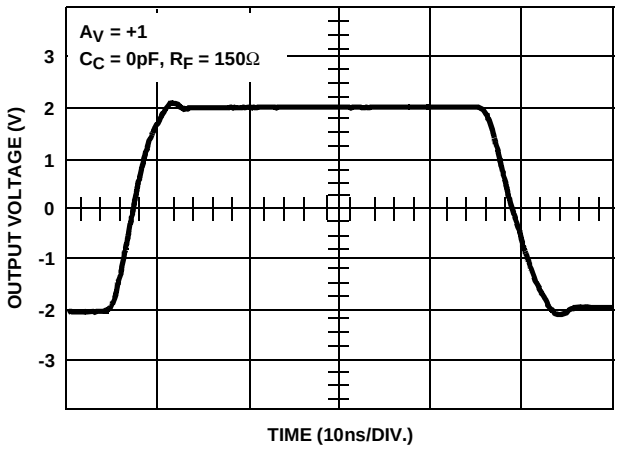


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

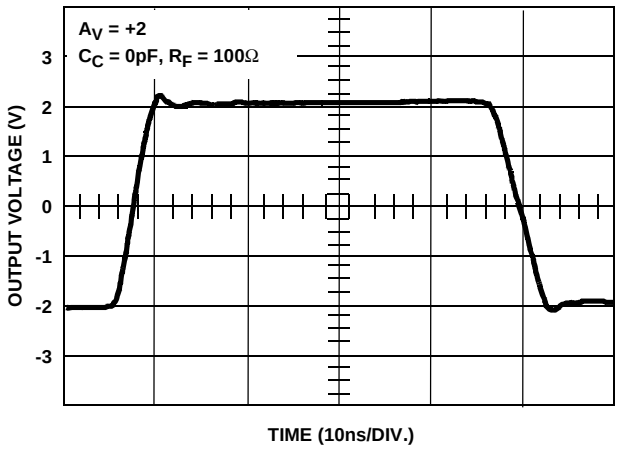


FIGURE 10. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

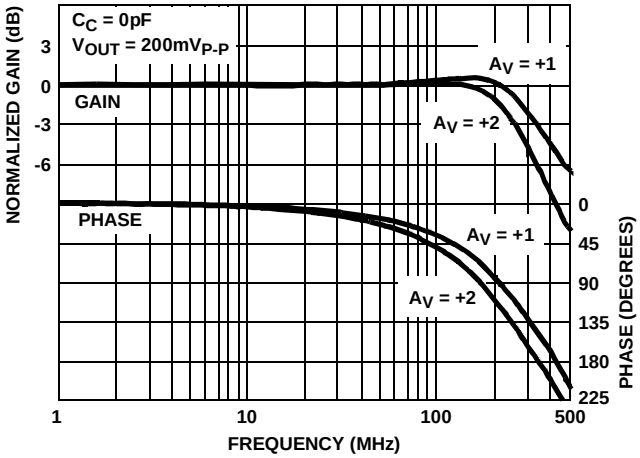


FIGURE 11. FREQUENCY RESPONSE

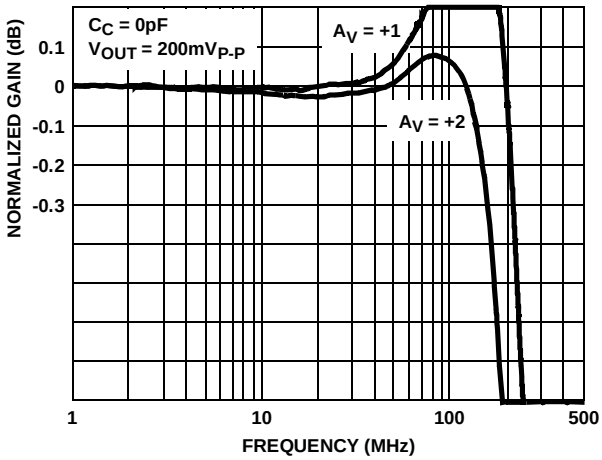


FIGURE 12. GAIN FLATNESS

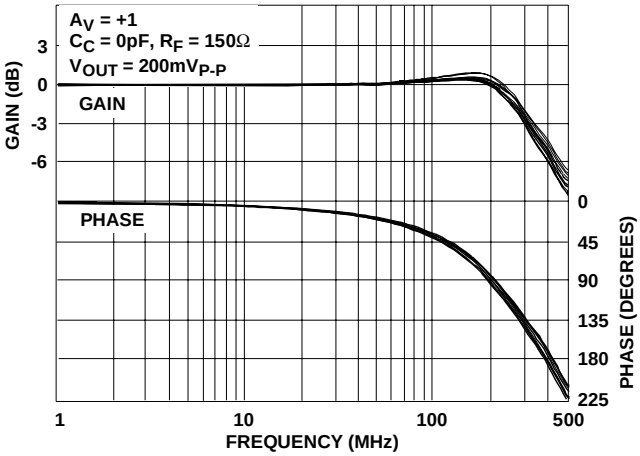


FIGURE 13. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

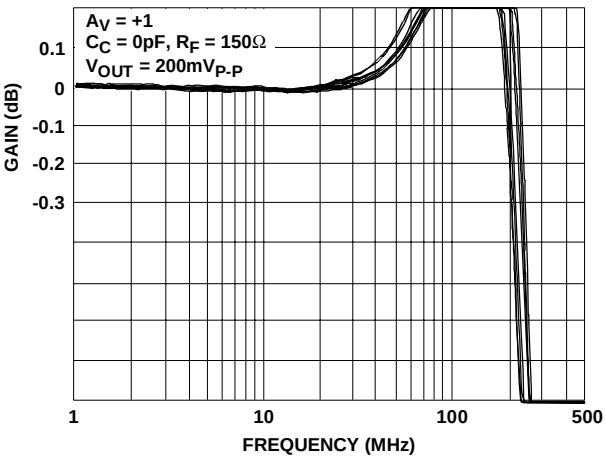


FIGURE 14. GAIN FLATNESS (12 UNITS, 4 RUNS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

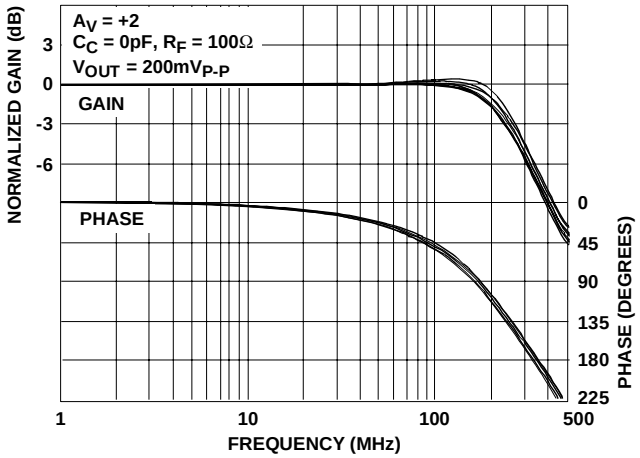


FIGURE 15. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

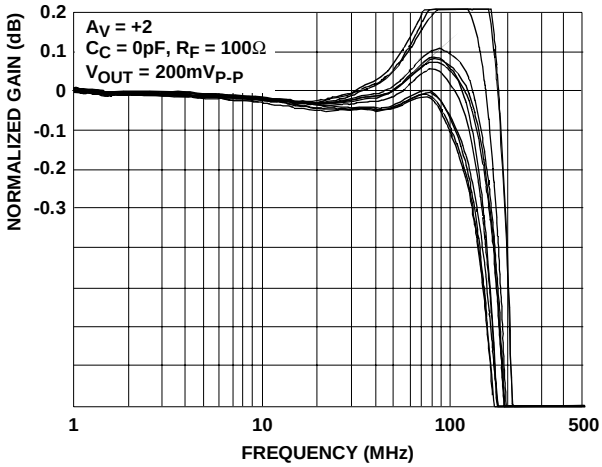


FIGURE 16. GAIN FLATNESS (12 UNITS, 4 RUNS)

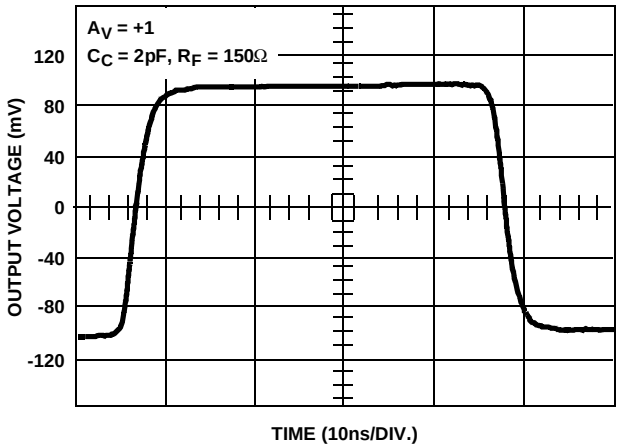


FIGURE 17. SMALL SIGNAL PULSE RESPONSE

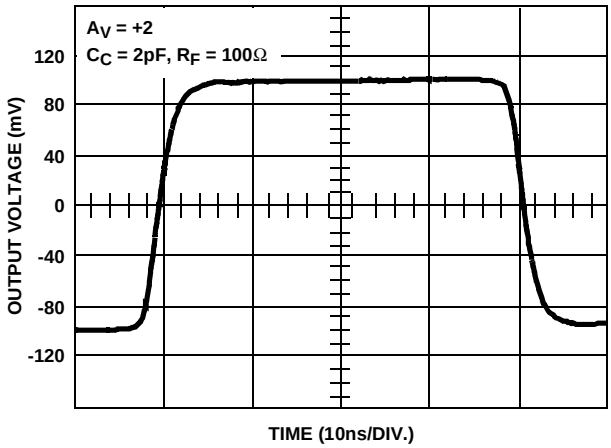


FIGURE 18. SMALL SIGNAL PULSE RESPONSE

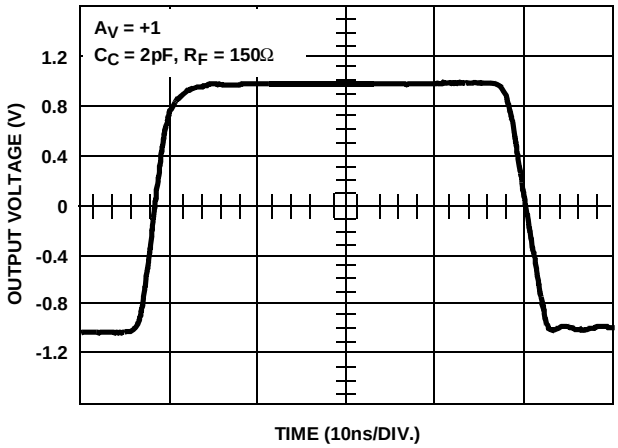


FIGURE 19. LARGE SIGNAL PULSE RESPONSE

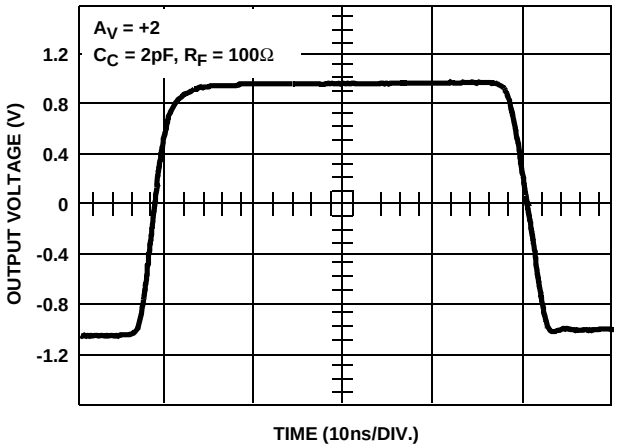


FIGURE 20. LARGE SIGNAL OUTPUT VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

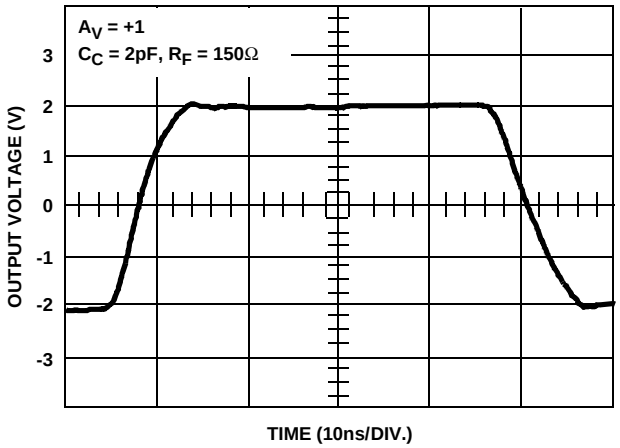


FIGURE 21. LARGE SIGNAL PULSE RESPONSE

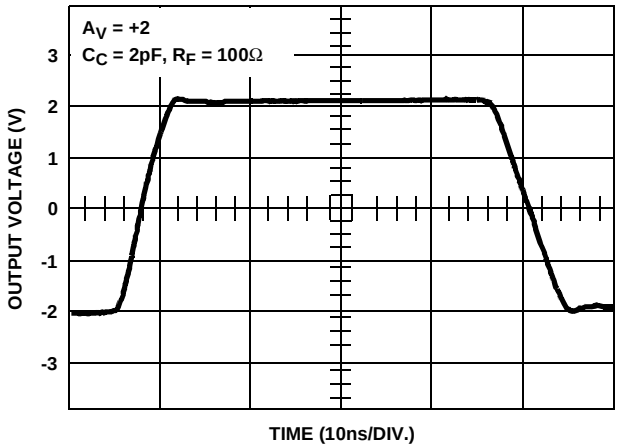


FIGURE 22. LARGE SIGNAL PULSE RESPONSE

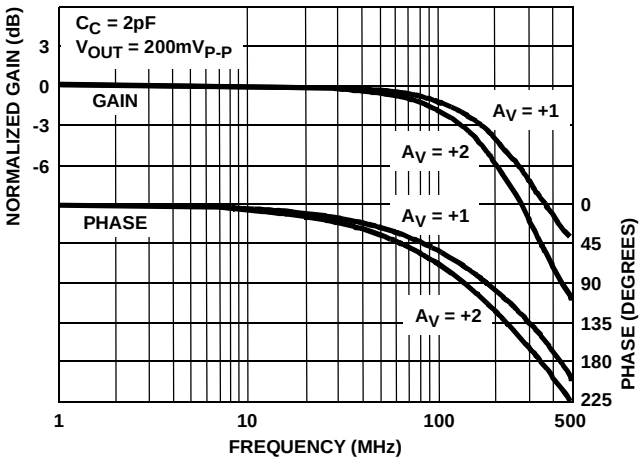


FIGURE 23. FREQUENCY RESPONSE

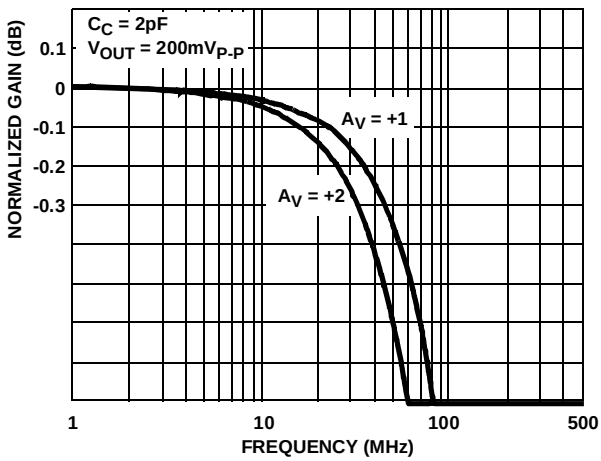


FIGURE 24. GAIN FLATNESS

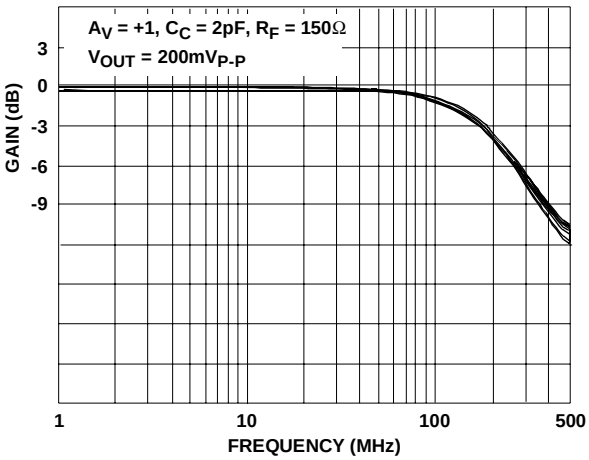


FIGURE 25. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

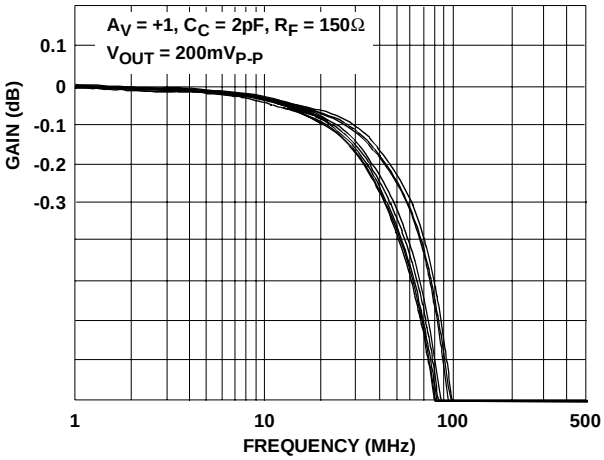


FIGURE 26. GAIN FLATNESS (12 UNITS, 4 RUNS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

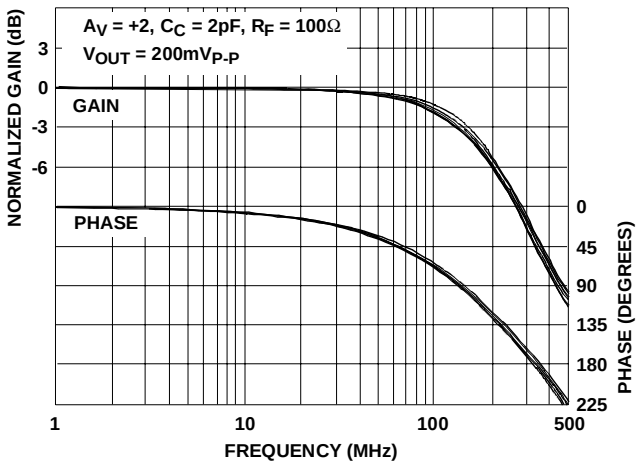


FIGURE 27. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

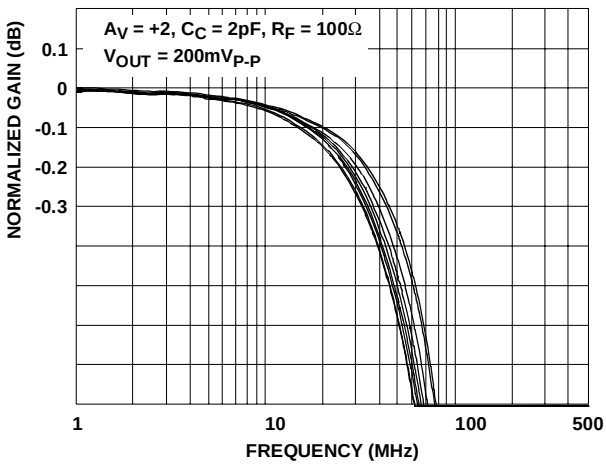


FIGURE 28. GAIN FLATNESS (12 UNITS, 4 RUNS)

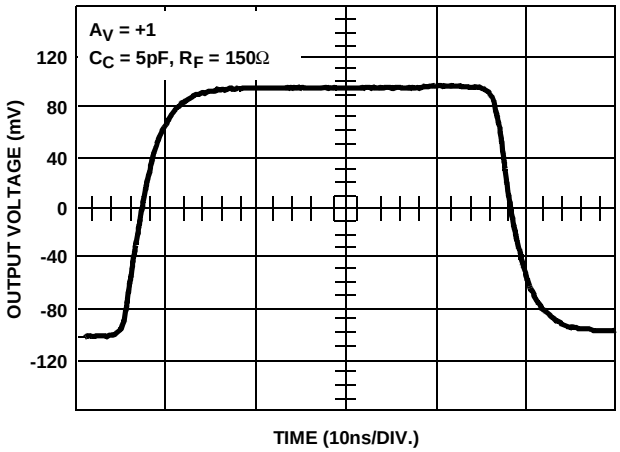


FIGURE 29. SMALL SIGNAL PULSE RESPONSE

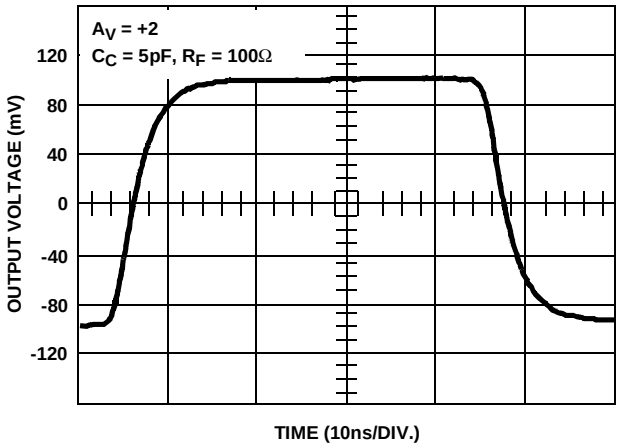


FIGURE 30. SMALL SIGNAL PULSE RESPONSE

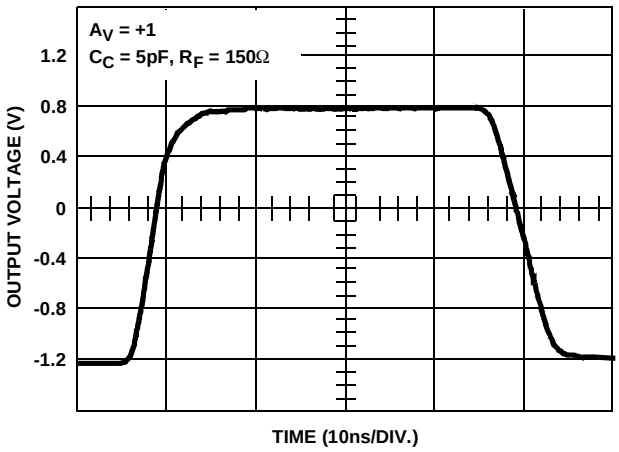


FIGURE 31. LARGE SIGNAL PULSE RESPONSE

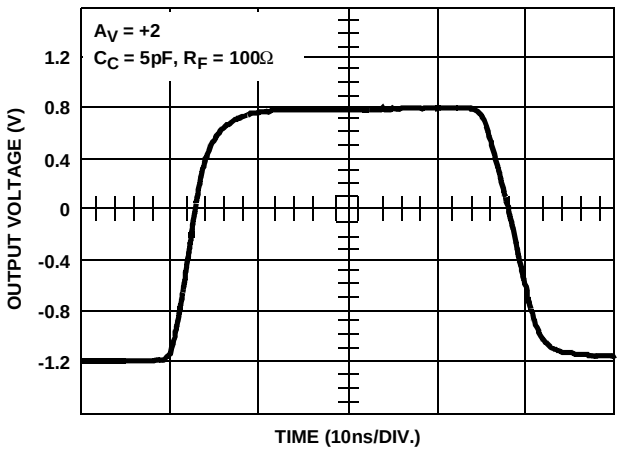


FIGURE 32. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

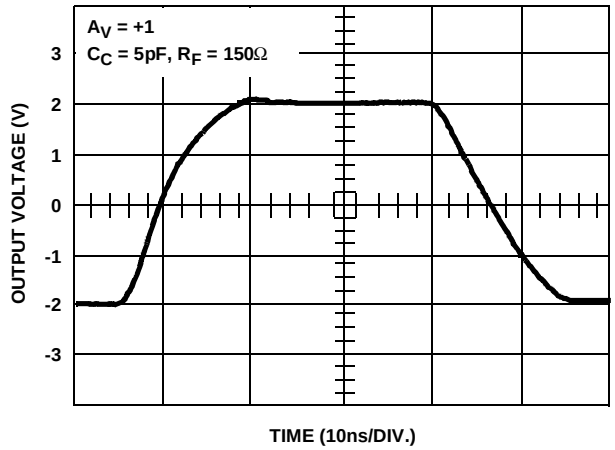


FIGURE 33. LARGE SIGNAL PULSE RESPONSE

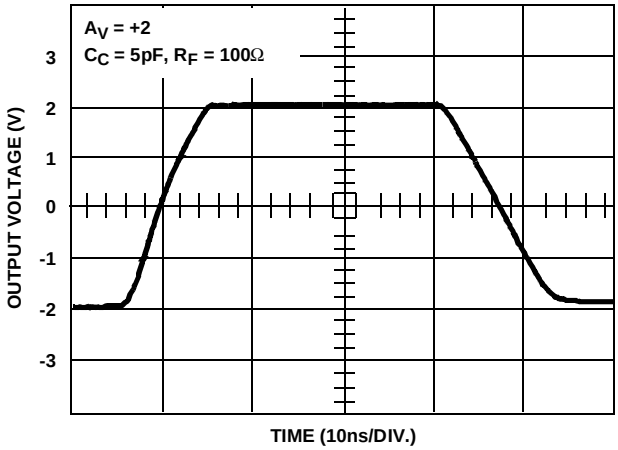


FIGURE 34. LARGE SIGNAL PULSE RESPONSE

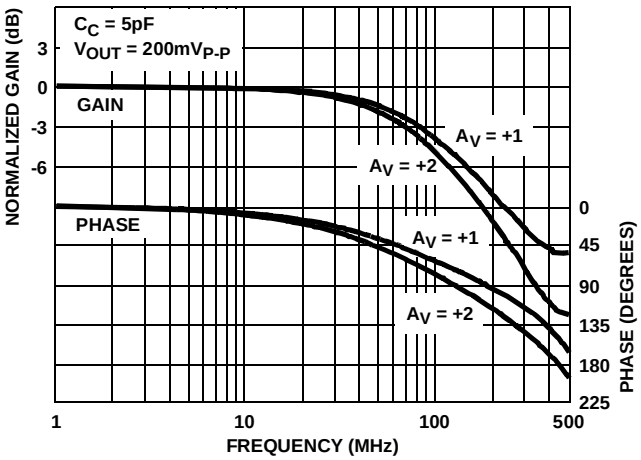


FIGURE 35. FREQUENCY RESPONSE

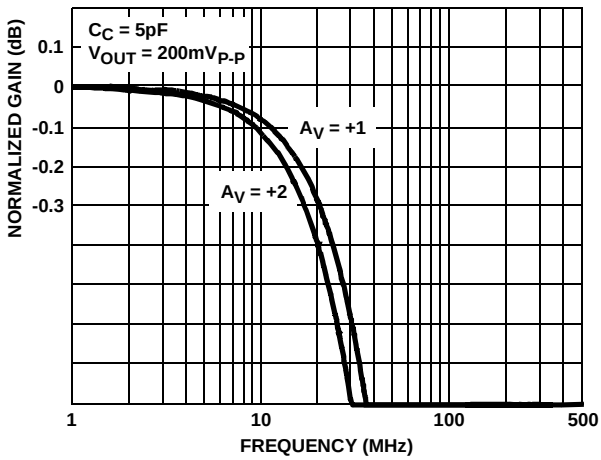


FIGURE 36. GAIN FLATNESS

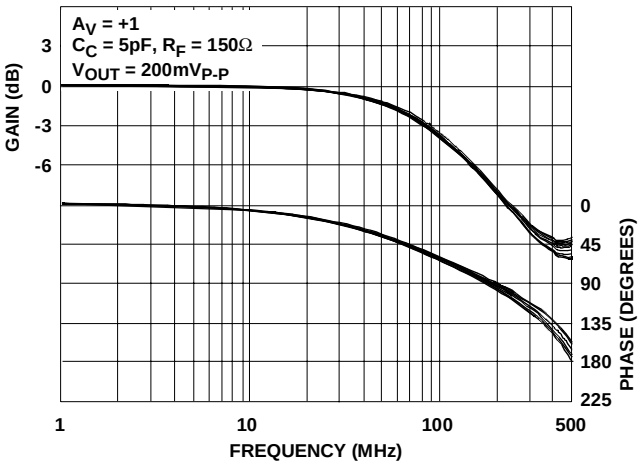


FIGURE 37. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

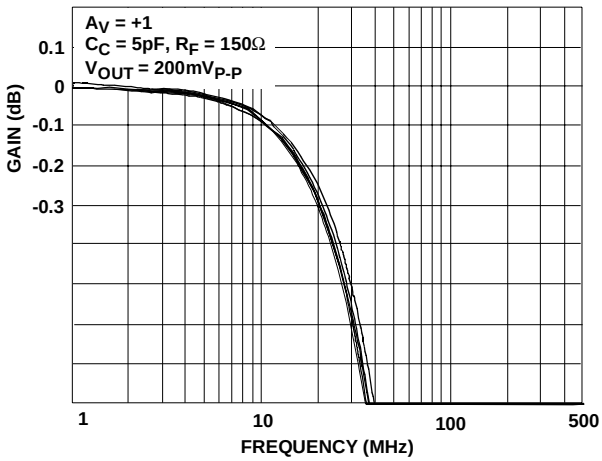


FIGURE 38. GAIN FLATNESS (12 UNITS, 4 RUNS)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

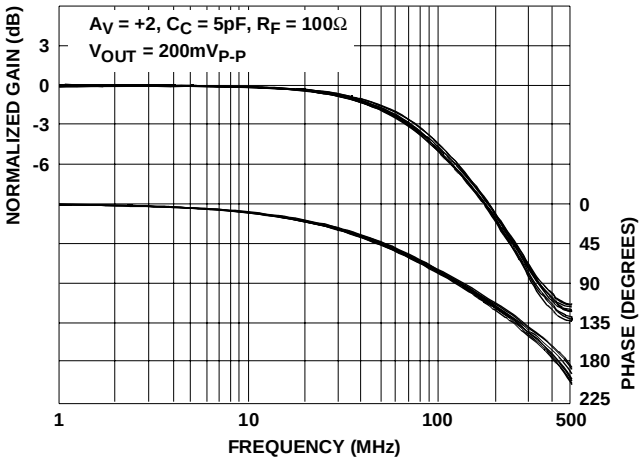


FIGURE 39. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

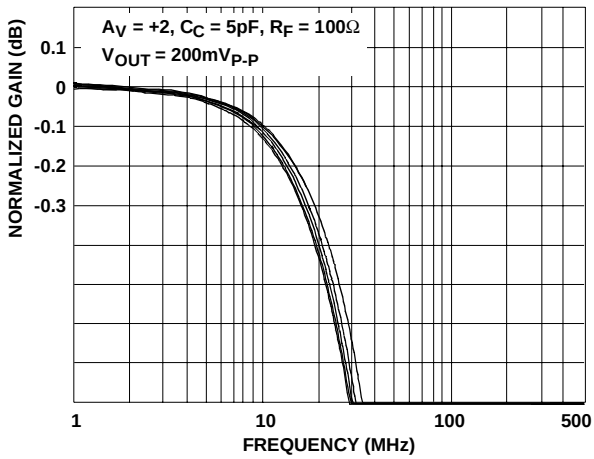


FIGURE 40. GAIN FLATNESS (12 UNITS, 4 RUNS)

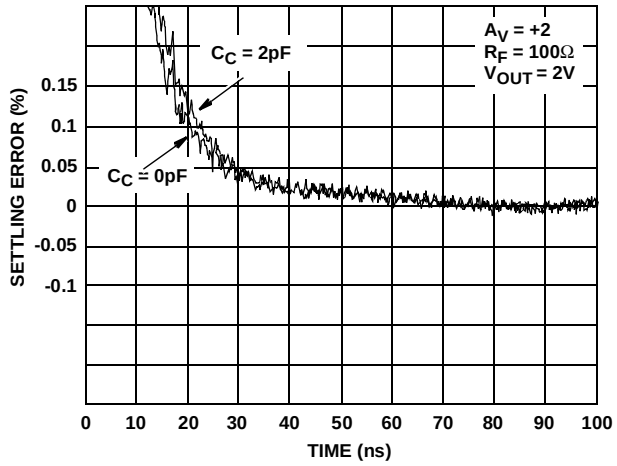


FIGURE 41. SETTLING RESPONSE

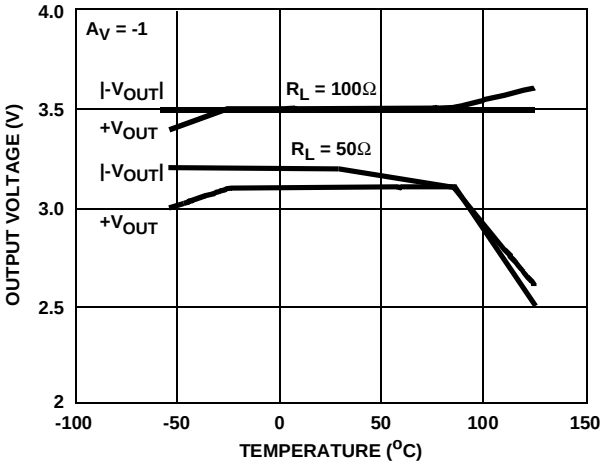


FIGURE 42. OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

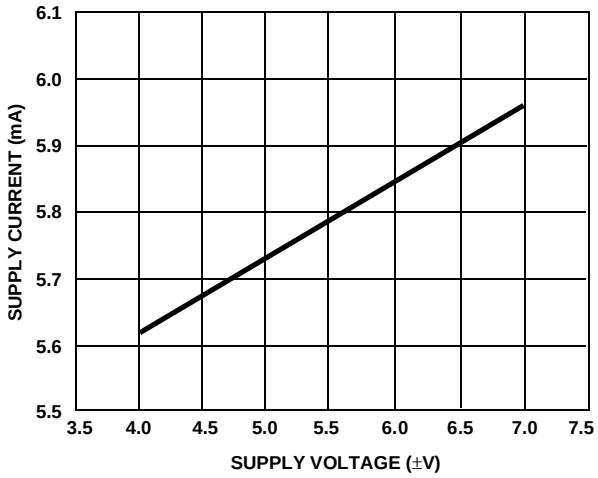


FIGURE 43. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

59 mils x 58.2 mils x 19 mils
1500µm x 1480µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

75

SUBSTRATE POTENTIAL (Powered Up):

Floating
(Recommend Connection to V-)

Metallization Mask Layout

HFA1106