Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**

- **User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors**

- **Low Differential Gain and Phase . . . . .0.02%/0.04 Deg.**

- **Low Distortion (HD3, 30MHz) . . . . -73dBc (Typ)**

- **Wide -3dB Bandwidth . . . . 850MHz (Typ)**

- **Very High Slew Rate . . . . 2400V/μs (Typ)**

- **Fast Settling (0.1%) . . . . 13ns (Typ)**

- **Excellent Gain Flatness (to 100MHz) . . . . 0.07dB (Typ)**

- **Excellent Gain Accuracy. . . . . .0.99V/V (Typ)**

- **High Output Current . . . . 60mA (Typ)**

- **Fast Overdrive Recovery . . . .<10ns (Typ)**

Applications

- **Video Switching and Routing**

- **Pulse and Video Amplifiers**

- **Wideband Amplifiers**

- **RF/IF Signal Processing**

- **Flash A/D Driver**

- **Medical Imaging Systems**

Description

The HFA1112/883 is a closed loop buffer that achieves a high degree of gain accuracy, wide bandwidth, and low distortion. Manufactured on the Intersil proprietary complementary bipolar UHF-1 process, the HFA1112/883 also offers very fast slew rates, and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Component and composite video systems will also benefit from this buffer's performance, as indicated by the excellent gain flatness, and 0.02%/0.04 Deg. Differential Gain/Phase specifications (R_L = 150Ω).

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.
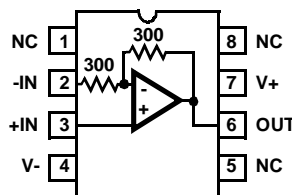
This amplifier is available with programmable output clamps as the HFA1113/883. For applications requiring a standard buffer pinout, please refer to the HFA1110/883 datasheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1112MJ/883	-55°C to +125°C	8 Lead Ceramic DIP

Pinout

HFA1112/883
(CERDIP)
TOP VIEW

Spec Number **511084-883**

FN3610.1

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Differential Input Voltage 5V
Voltage at Either Input Terminal . . . . V+ to V-
Output Current (50% Duty Cycle) . . . . ±55mA
Junction Temperature . . . . +175°C
ESD Rating . . . . < 2000V
Storage Temperature Range . . . . -65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering 10s) . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	115°C/W	30°C/W

Maximum Package Power Dissipation at +75°C
  CerDIP Package 0.87W
Package Power Dissipation Derating Factor above +75°C
  CerDIP Package . . . . 8.7mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (±V_S) . . . . ±5V R_L Š≥ 50Ω
Operating Temperature Range . . . . -55°C ≤ T_A ≤ +125°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V_{SUPPLY} = ±5V, R_{SOURCE} = 0Ω, R_L = 100Ω, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Output Offset Voltage	V_{OS}	V_{CM} = 0V		1	+25°C	-25	25	mV
				2, 3	+125°C, -55°C	-40	40	mV
Power Supply Rejection Ratio	PSRRP	ΔV_{SUP} = ±1.25V V+ = 6.25V, V- = -5V V+ = 3.75V, V- = -5V		1	+25°C	39	-	dB
				2, 3	+125°C, -55°C	35	-	dB
	PSRRN	ΔV_{SUP} = ±1.25V V+ = 5V, V- = -6.25V V+ = 5V, V- = -3.75V		1	+25°C	39	-	dB
				2, 3	+125°C, -55°C	35	-	dB
Non-Inverting Input (+IN) Current	I_{BSP}	V_{CM} = 0V		1	+25°C	-40	40	µA
				2, 3	+125°C, -55°C	-65	65	µA
+IN Common Mode Rejection	CMS_{IBP}	ΔV_{CM} = ±2V V+ = 3V, V- = -7V V+ = 7V, V- = -3V		1	+25°C	-	40	µA/V
				2, 3	+125°C, -55°C	-	50	µA/V
+IN Resistance	+R_{IN}	Note 1		1	+25°C	25	-	kΩ
				2, 3	+125°C, -55°C	20	-	kΩ
Gain (V_{OUT} = 2V_{P-P})	A_{VP1}	A_V = +1 V_{IN} = -1V to +1V		1	+25°C	0.980	1.020	V/V
				2, 3	+125°C, -55°C	0.975	1.025	V/V
Gain (V_{OUT} = 2V_{P-P})	A_{VM1}	A_V = -1 V_{IN} = -1V to +1V		1	+25°C	0.980	1.020	V/V
				2, 3	+125°C, -55°C	0.975	1.025	V/V
Gain (V_{OUT} = 4V_{P-P})	A_{VP2}	A_V = +2 V_{IN} = -1V to +1V		1	+25°C	1.960	2.040	V/V
				2, 3	+125°C, -55°C	1.950	2.050	V/V
Output Voltage Swing	V_{OP100}	A_V = -1 R_L = 100Ω	V_{IN} = -3.2V	1	+25°C	3	-	V
			V_{IN} = -2.7V	2, 3	+125°C, -55°C	2.5	-	V
	V_{ON100}	A_V = -1 R_L = 100Ω	V_{IN} = +3.2V	1	+25°C	-	-3	V
			V_{IN} = +2.7V	2, 3	+125°C, -55°C	-	-2.5	V
Output Voltage Swing	V_{OP50}	A_V = -1 R_L = 50Ω	V_{IN} = -2.7V	1, 2	+25°C, +125°C	2.5	-	V
			V_{IN} = -2.25V	3	-55°C	1.5	-	V
	V_{ON50}	A_V = -1 R_L = 50Ω	V_{IN} = +2.7V	1, 2	+25°C, +125°C	-	-2.5	V
			V_{IN} = +2.25V	3	-55°C	-	-1.5	V

Spec Number **511084-883**

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at $V_{SUPPLY} = \pm 5V$, $R_{SOURCE} = 0\Omega$, $R_L = 100\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current	$+I_{OUT}$	Note 2	1, 2	+25°C, +125°C	50	-	mA
			3	-55°C	30	-	mA
	$-I_{OUT}$	Note 2	1, 2	+25°C, +125°C	-	-50	mA
			3	-55°C	-	-30	mA
Quiescent Power Supply Current	I_{CC}	$R_L = 100\Omega$	1	+25°C	14	26	mA
			2, 3	+125°C, -55°C	-	33	mA
	I_{EE}	$R_L = 100\Omega$	1	+25°C	-26	-14	mA
			2, 3	+125°C, -55°C	-33	-	mA

NOTES:

1. Guaranteed from +IN Common Mode Rejection Test, by: $+R_{IN} = 1/CMS_{IBP}$.

2. Guaranteed from V_{OUT} Test with $R_L = 50\Omega$, by: $I_{OUT} = V_{OUT}/50\Omega$.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
-3dB Bandwidth	BW(-1)	$A_V = -1$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	450	-	MHz
	BW(+1)	$A_V = +1$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	500	-	MHz
	BW(+2)	$A_V = +2$, $V_{OUT} = 200mV_{P-P}$	1	+25°C	350	-	MHz
Gain Flatness	GF30	$A_V = +2$, $f \le 30MHz$ $V_{OUT} = 200mV_{P-P}$	1	+25°C	-	±0.04	dB
	GF50	$A_V = +2$, $f \le 50MHz$ $V_{OUT} = 200mV_{P-P}$	1	+25°C	-	±0.08	dB
	GF100	$A_V = +2$, $f \le 100MHz$ $V_{OUT} = 200mV_{P-P}$	1	+25°C	-	±0.22	dB
Slew Rate	+SR(-1)	$A_V = -1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1500	-	V/μs
	-SR(-1)	$A_V = -1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1800	-	V/μs
	+SR(+1)	$A_V = +1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	900	-	V/μs
	-SR(+1)	$A_V = +1$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	800	-	V/μs
	+SR(+2)	$A_V = +2$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1200	-	V/μs
	-SR(+2)	$A_V = +2$, $V_{OUT} = 5V_{P-P}$	1, 2	+25°C	1100	-	V/μs
Rise and Fall Time	$T_R(-1)$	$A_V = -1$, $V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	750	ps
	$T_F(-1)$	$A_V = -1$, $V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	800	ps
	$T_R(+1)$	$A_V = +1$, $V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	750	ps
	$T_F(+1)$	$A_V = +1$, $V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	750	ps
	$T_R(+2)$	$A_V = +2$, $V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	1000	ps
	$T_F(+2)$	$A_V = +2$, $V_{OUT} = 0.5V_{P-P}$	1, 2	+25°C	-	1000	ps

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Overshoot	+OS(-1)	$A_V = -1$, $V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	30	%
	-OS(-1)	$A_V = -1$, $V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	25	%
	+OS(+1)	$A_V = +1$, $V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	65	%
	-OS(+1)	$A_V = +1$, $V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	60	%
	+OS(+2)	$A_V = +2$, $V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	20	%
	-OS(+2)	$A_V = +2$, $V_{OUT} = 0.5V_{P-P}$	1, 3	+25°C	-	20	%
Settling Time	TS(0.1)	$A_V = +2$, to 0.1% $V_{OUT} = 2V$ to 0V	1	+25°C	-	20	ns
	TS(0.05)	$A_V = +2$, to 0.05% $V_{OUT} = 2V$ to 0V	1	+25°C	-	33	ns
2nd Harmonic Distortion	HD2(30)	$A_V = +2$, f = 30MHz $V_{OUT} = 2V_{P-P}$	1	+25°C	-	-45	dBc
	HD2(50)	$A_V = +2$, f = 50MHz $V_{OUT} = 2V_{P-P}$	1	+25°C	-	-40	dBc
	HD2(100)	$A_V = +2$, f = 100MHz $V_{OUT} = 2V_{P-P}$	1	+25°C	-	-35	dBc
3rd Harmonic Distortion	HD3(30)	$A_V = +2$, f = 30MHz $V_{OUT} = 2V_{P-P}$	1	+25°C	-	-65	dBc
	HD3(50)	$A_V = +2$, f = 50MHz $V_{OUT} = 2V_{P-P}$	1	+25°C	-	-55	dBc
	HD3(100)	$A_V = +2$, f = 100MHz $V_{OUT} = 2V_{P-P}$	1	+25°C	-	-45	dBc

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot-to-lot and within lot variation.

2. Measured between 10% and 90% points.

3. For 200ps input transition times. Overshoot decreases as input transition times increase, especially for $A_V = +1$. Please refer to Performance curves.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Spec Number **511084-883**

Die Characteristics

DIE DIMENSIONS:
  63 x 44 x 19 mils $\pm$ 1 mils
  1600μm x 1130μm x 483μm $\pm$ 25.4μm

METALLIZATION:
  Type: Metal 1: AlCu(2%)/TiW   Type: Metal 2: AlCu(2%)
  Thickness: Metal 1: 8kÅ $\pm$ 0.4kÅ   Thickness: Metal 2: 16kÅ $\pm$ 0.8kÅ

GLASSIVATION:
  Type: Nitride
  Thickness: 4kÅ $\pm$ 0.5kÅ

WORST CASE CURRENT DENSITY:
  2.0 x 10^5 A/cm^2 at 47.5mA

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1112/883
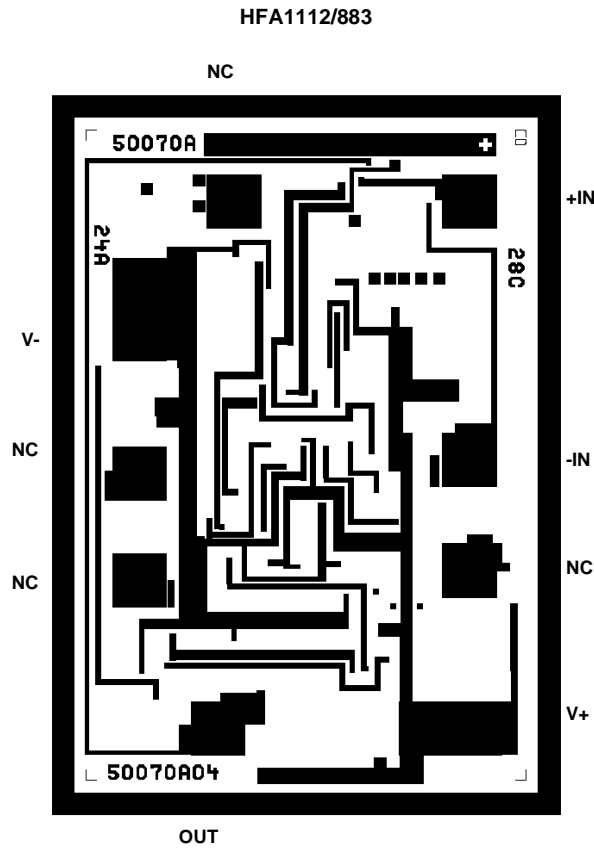
Test Circuit (Applies to Table 1)

$$V_{OS} = \frac{V_Y}{100}$$

$$+I_{BIAS} = \frac{V_Z}{100K}$$
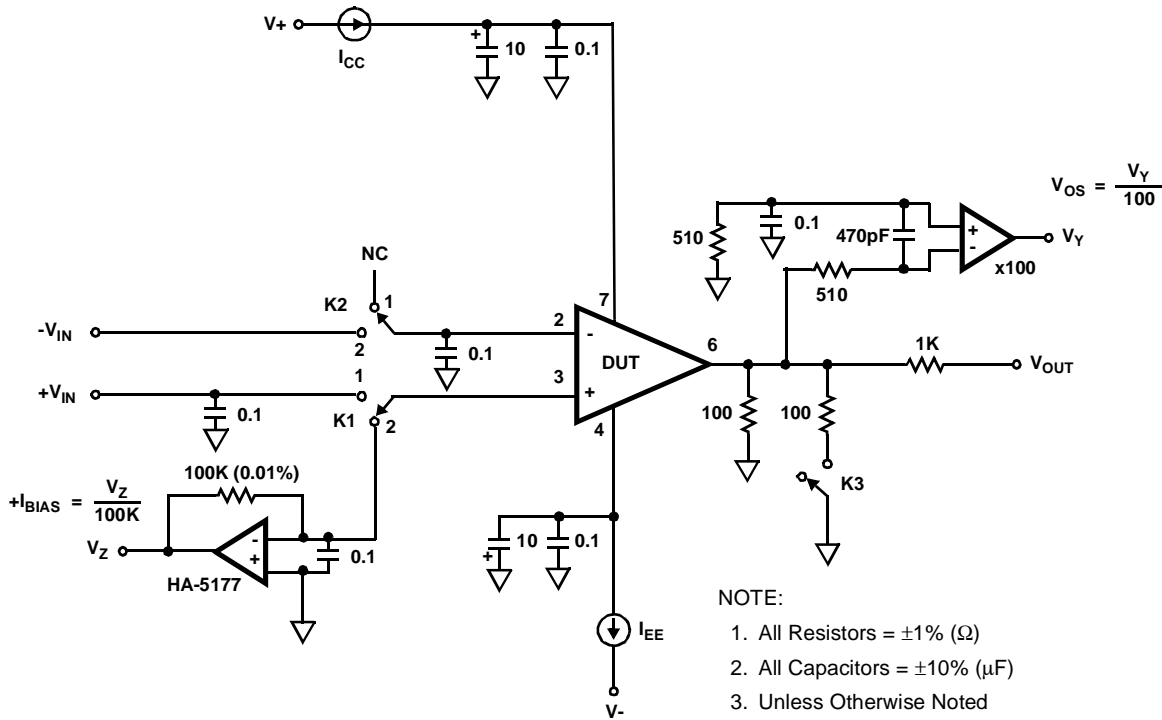
NOTE:

1. All Resistors = ±1% (Ω)
2. All Capacitors = ±10% (μF)
3. Unless Otherwise Noted
4. Chip Components Recommended
5. For A_V = +1, K1 = Position 1, K2 = Position 1
6. For A_V = +2, K1 = Position 1, K2 = Position 2, $-V_{IN}$ = 0V
7. For A_V = -1, K1 = Position 1, K2 = Position 2, $+V_{IN}$ = 0V

Test Waveforms

SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE (Applies to Table 3)

A_V = +1 or +2 TEST CIRCUIT
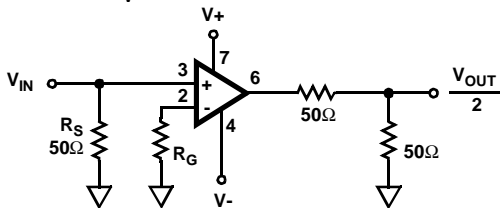
NOTE:

1. V_S = ±5V, R_G = 0Ω for A_V = +2, R_G = ∞ for A_V = +1
2. R_F = Internal, R_S = 50Ω
3. R_L = 100Ω For Small and Large Signals

A_V = -1 TEST CIRCUIT
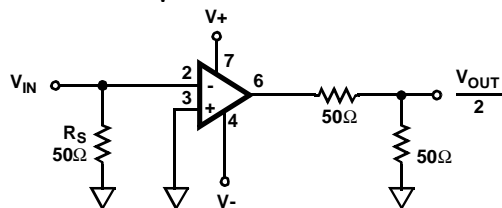
NOTE:

1. V_S = ±5V, A_V = -1
2. R_F = Internal
3. R_S = 50Ω, R_L = 100Ω For Small and Large Signals

LARGE SIGNAL WAVEFORM

SMALL SIGNAL WAVEFORM
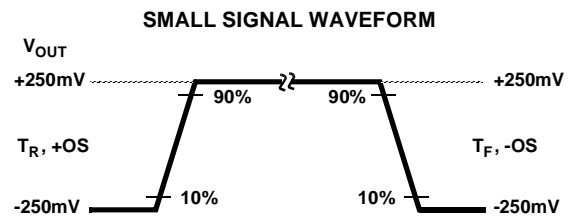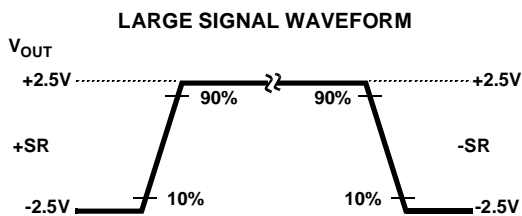
Burn-In Circuit

HFA1112MJ/883 CERAMIC DIP
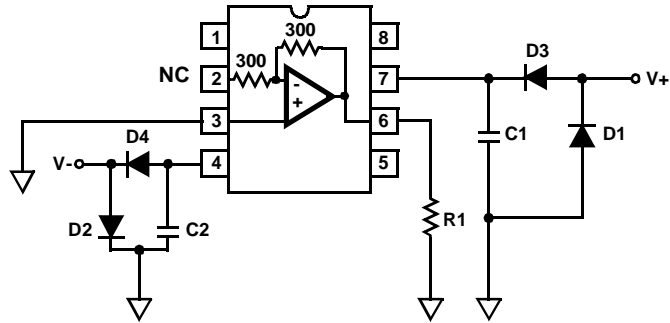
NOTE:

1. R1 = 100Ω, ±5% (Per Socket)

2. C1 = C2 = 0.01μF (Per Socket) or 0.1μF (Per Row) Minimum

3. D1 = D2 = 1N4002 or Equivalent (Per Board)

4. D3 = D4 = 1N4002 or Equivalent (Per Socket)

5. V+ = +5.5V ± 0.5V

6. V- = -5.5V ± 0.5V

Packaging
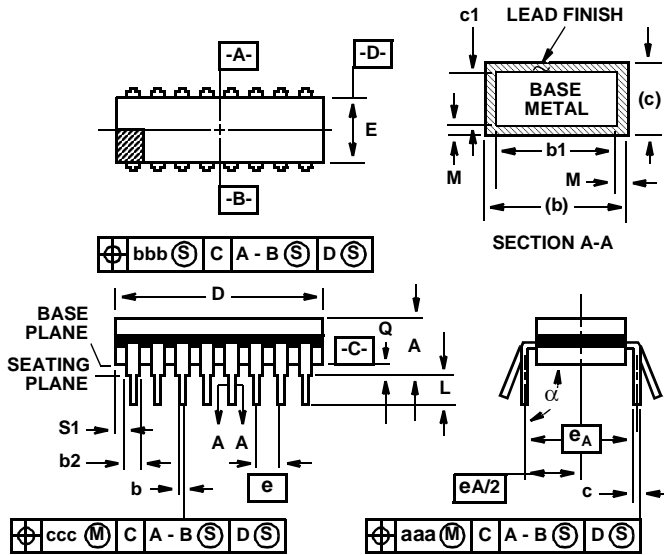
F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.

2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.

3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.

4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.

5. This dimension allows for off-center lid, meniscus, and glass overrun.

6. Dimension Q shall be measured from the seating plane to the base plane.

7. Measure dimension S1 at all four corners.

8. N is the maximum number of terminal positions.

9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

10. Controlling Dimension: Inch.

11. Lead Finish: Type A.

12. Materials: Compliant to MIL-M-38510.

Spec Number **511084-883**

DESIGN INFORMATION

Ultra High Speed
Programmable Gain Buffer Amplifier

February 2002

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

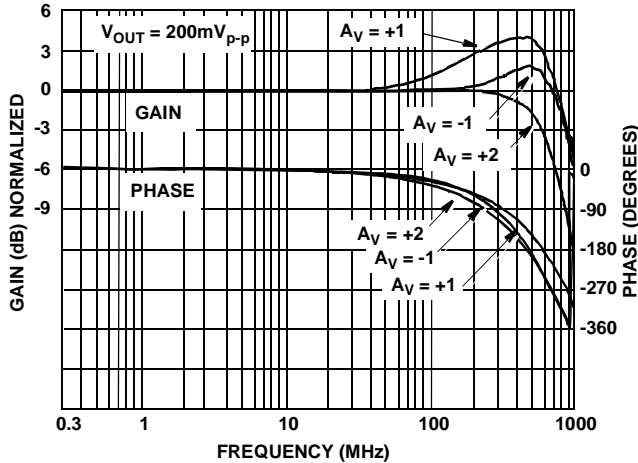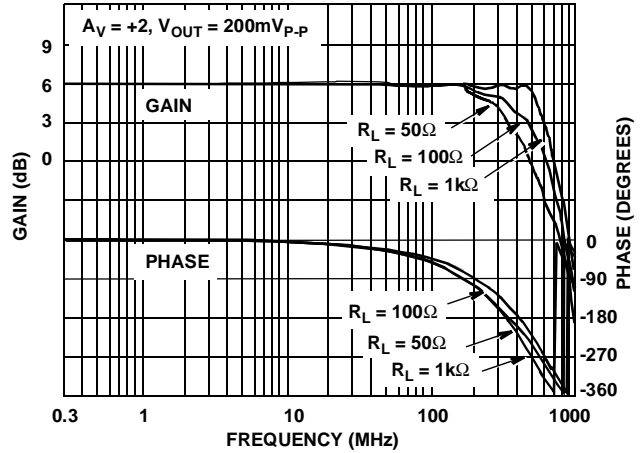### *Typical Performance Curves* $V_{SUPPLY} = \pm5V$, $R_L = 100\Omega$, $T_A = +25^oC$, Unless Otherwise Specified
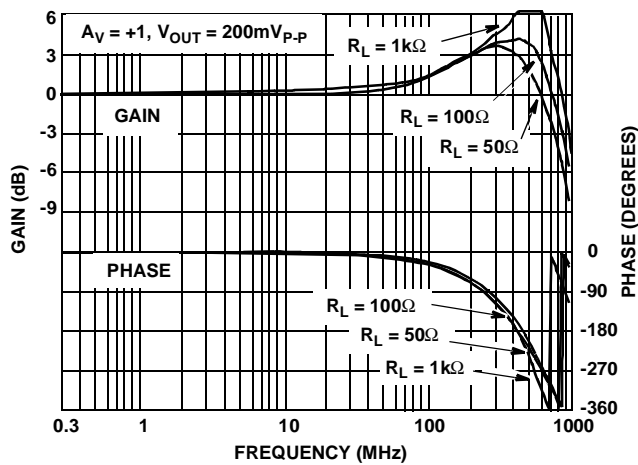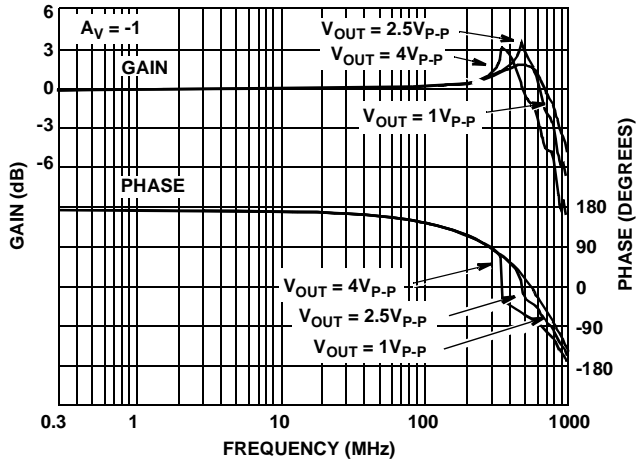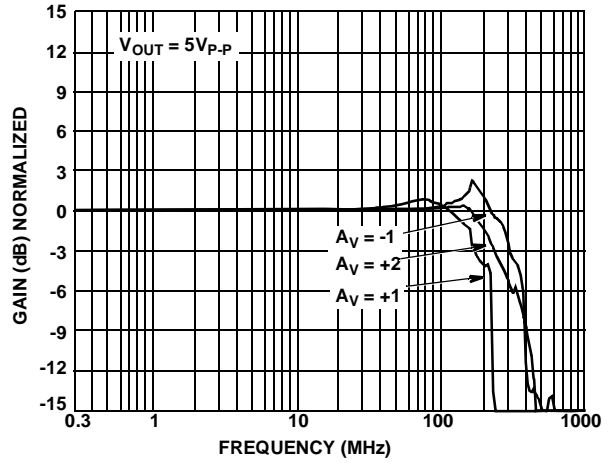
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_L = 100\Omega$, $T_A = +25^oC$, Unless Otherwise Specified **(Continued)**
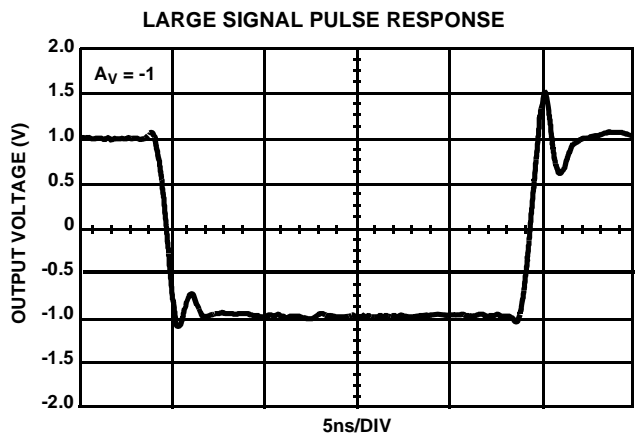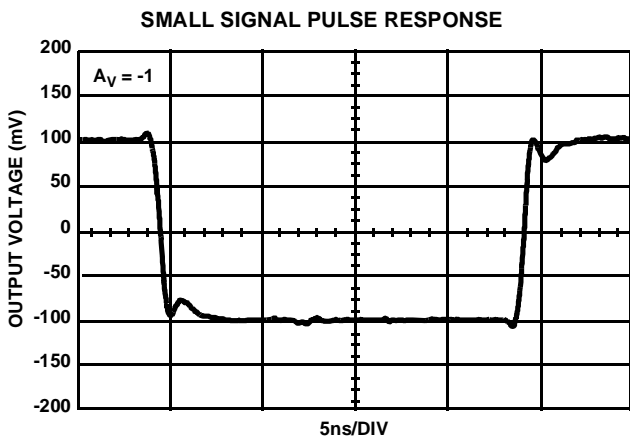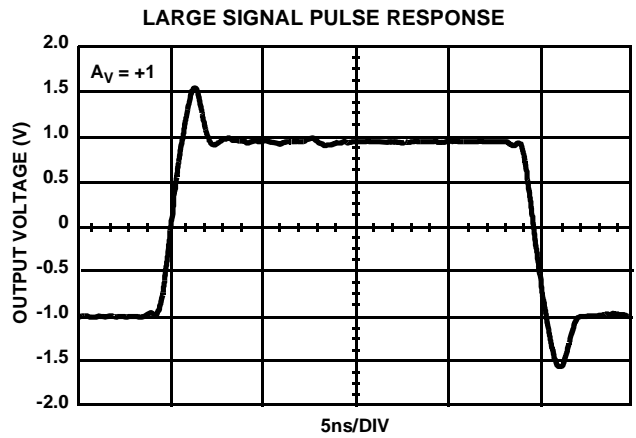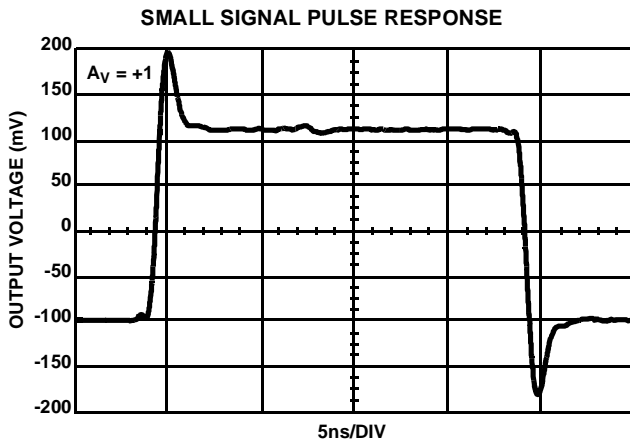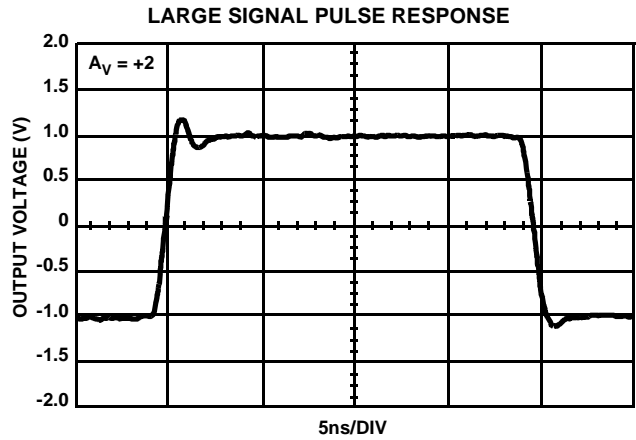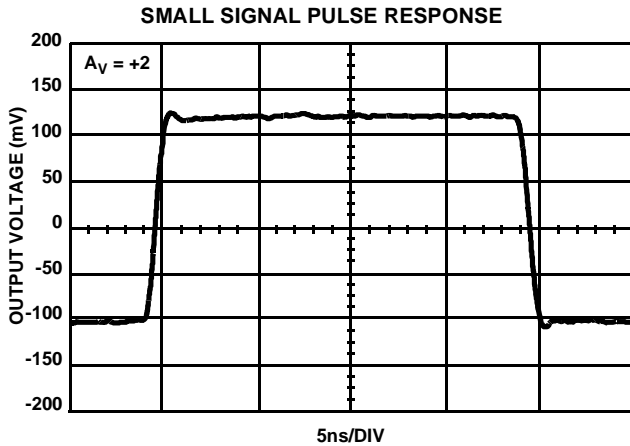
FREQUENCY RESPONSE

FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS
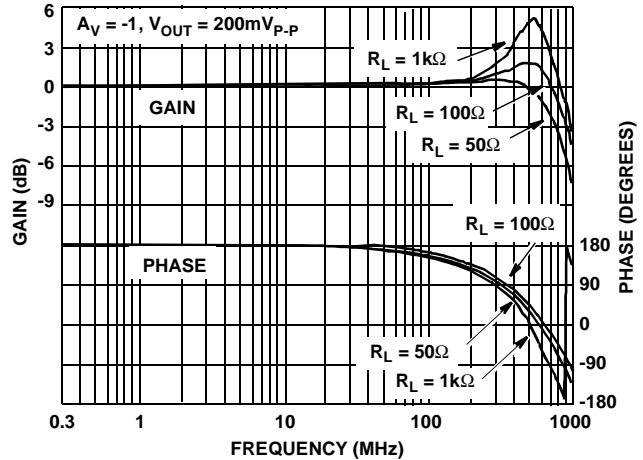
FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES
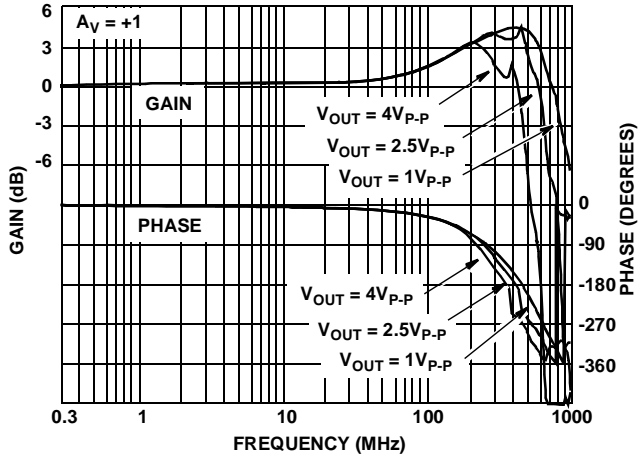
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DESIGN INFORMATION (Continued)

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Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, $T_A = +25^oC$, Unless Otherwise Specified **(Continued)**
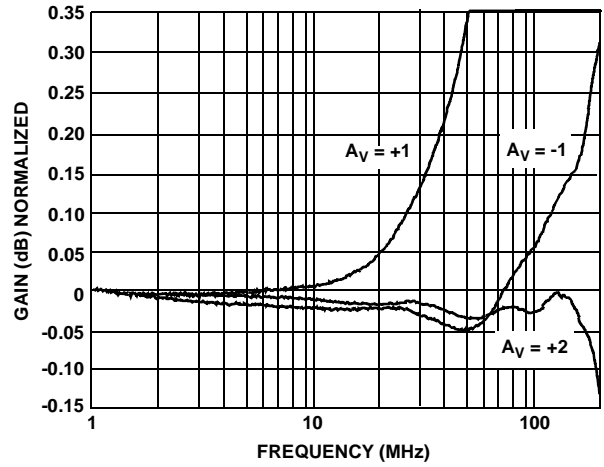
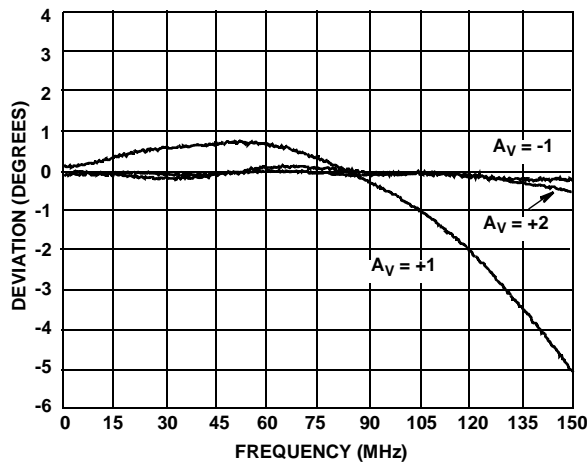**FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES**
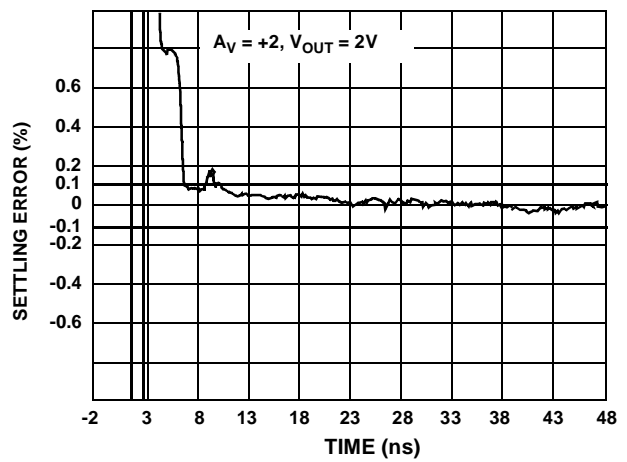
FULL POWER BANDWIDTH

-3dB BANDWIDTH vs TEMPERATURE
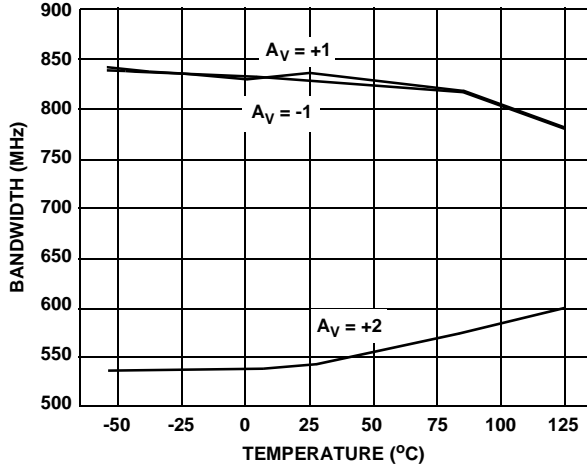
GAIN FLATNESS

DEVIATION FROM LINEAR PHASE

SETTLING RESPONSE

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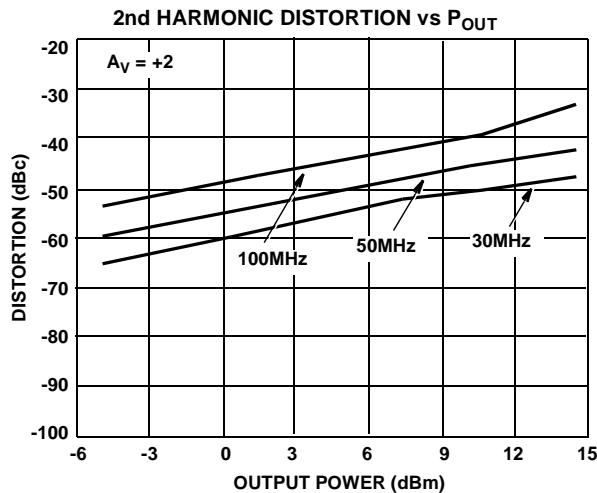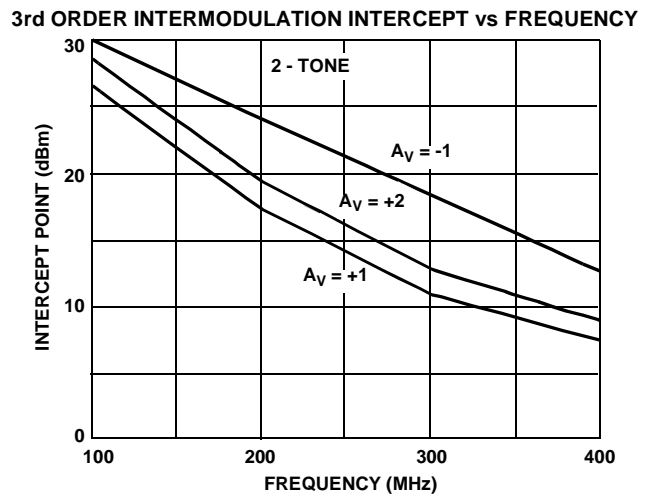
DESIGN INFORMATION (Continued)

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Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_L = 100\Omega$, $T_A = +25^oC$, Unless Otherwise Specified (Continued)

LOW FREQUENCY REVERSE ISOLATION (S_{12})

HIGH FREQUENCY REVERSE ISOLATION (S_{12})

1dB GAIN COMPRESSION vs FREQUENCY

3rd ORDER INTERMODULATION INTERCEPT vs FREQUENCY
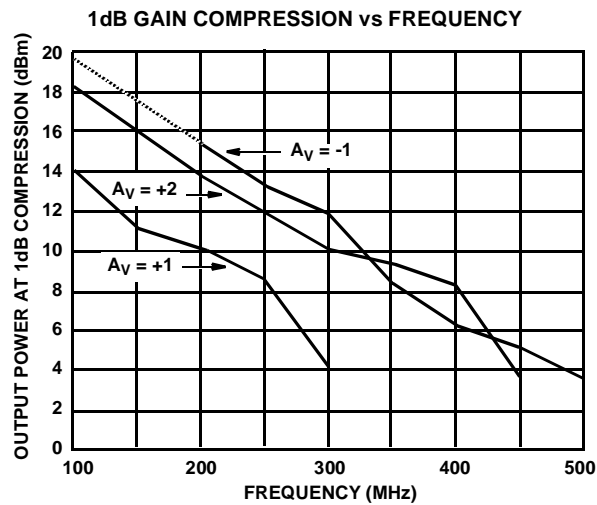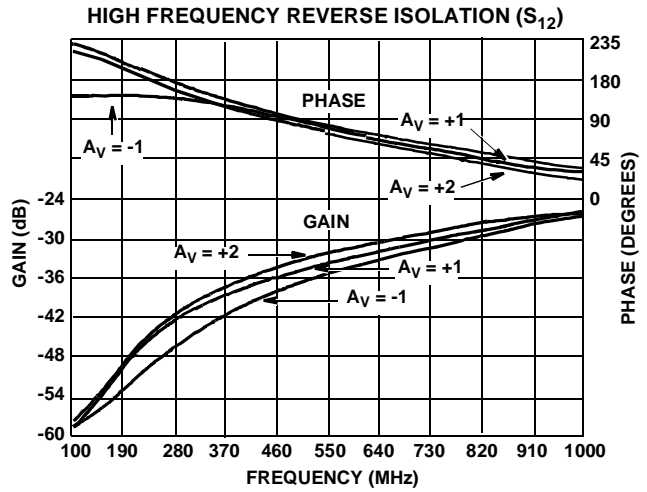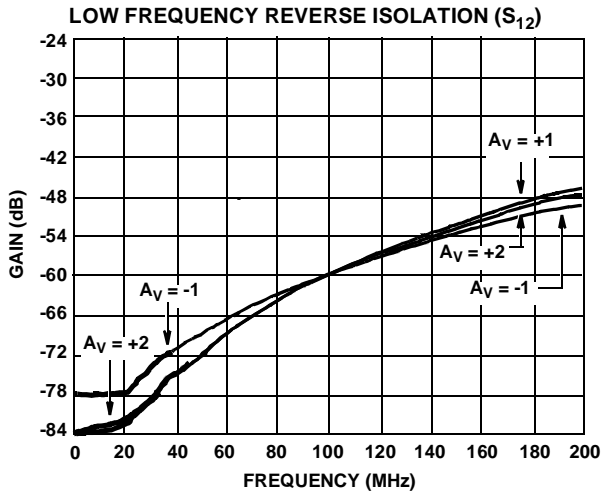
2nd HARMONIC DISTORTION vs P_{OUT}

3rd HARMONIC DISTORTION vs P_{OUT}

DESIGN INFORMATION (Continued)

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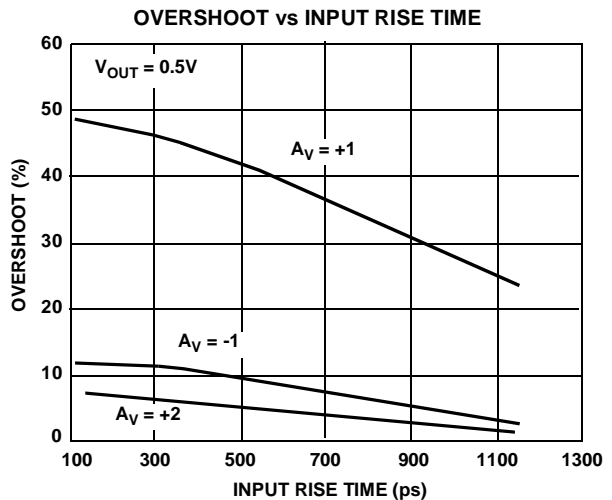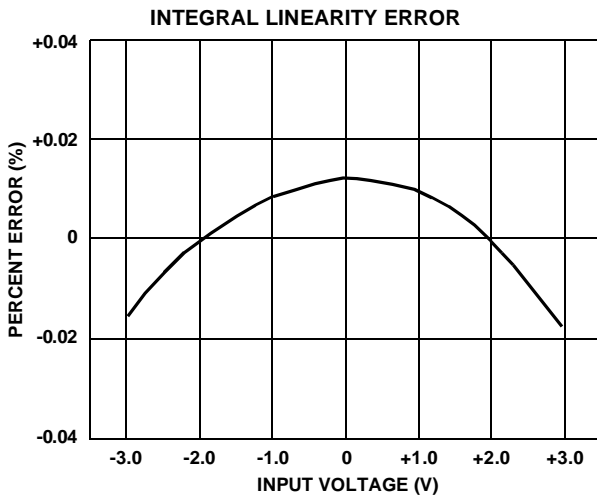
Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_L = 100\Omega$, $T_A = +25^oC$, Unless Otherwise Specified (Continued)

2nd HARMONIC DISTORTION vs P_{OUT}

$A_V = +1$

100MHz   50MHz   30MHz

DISTORTION (dBc) vs OUTPUT POWER (dBm)

3rd HARMONIC DISTORTION vs P_{OUT}

$A_V = +1$

100MHz   50MHz   30MHz

DISTORTION (dBc) vs OUTPUT POWER (dBm)

2nd HARMONIC DISTORTION vs P_{OUT}

$A_V = -1$

100MHz   50MHz   30MHz

DISTORTION (dBc) vs OUTPUT POWER (dBm)

3rd HARMONIC DISTORTION vs P_{OUT}

$A_V = -1$

100MHz   50MHz   30MHz

DISTORTION (dBc) vs OUTPUT POWER (dBm)

INTEGRAL LINEARITY ERROR

PERCENT ERROR (%) vs INPUT VOLTAGE (V)

OVERSHOOT vs INPUT RISE TIME

$V_{OUT} = 0.5V$

$A_V = +1$

$A_V = -1$

$A_V = +2$

OVERSHOOT (%) vs INPUT RISE TIME (ps)

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DESIGN INFORMATION (Continued)

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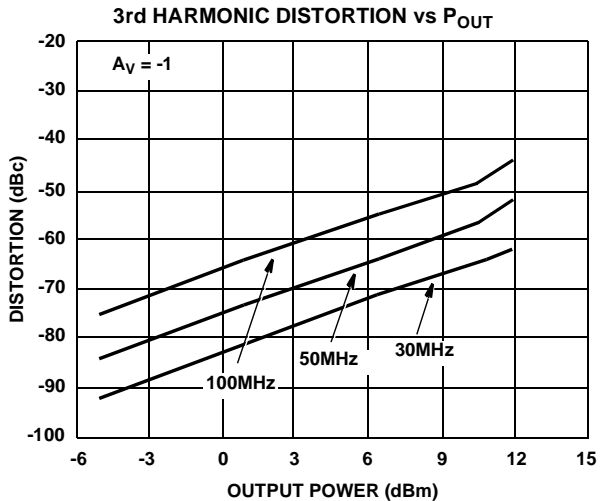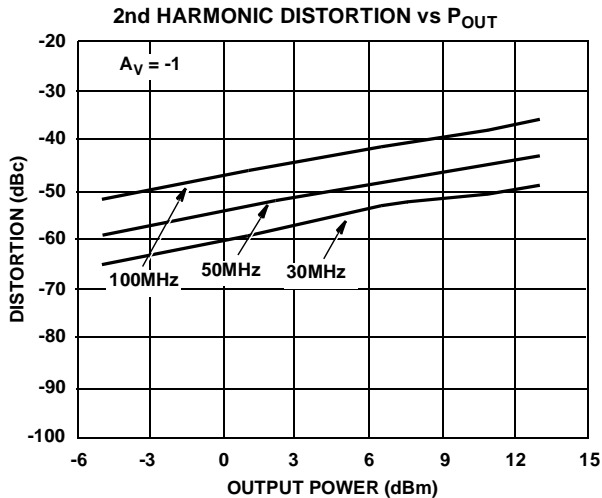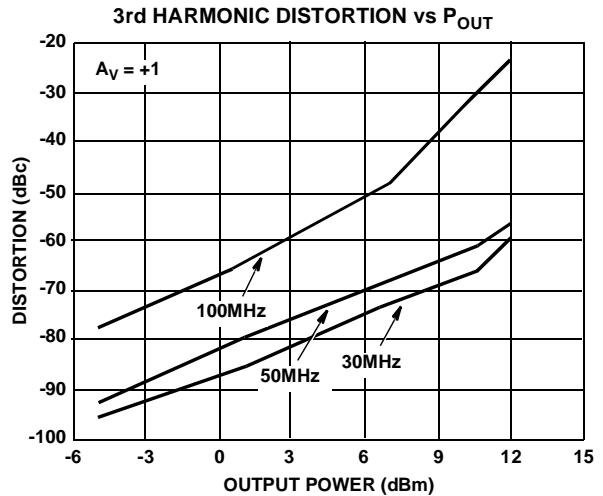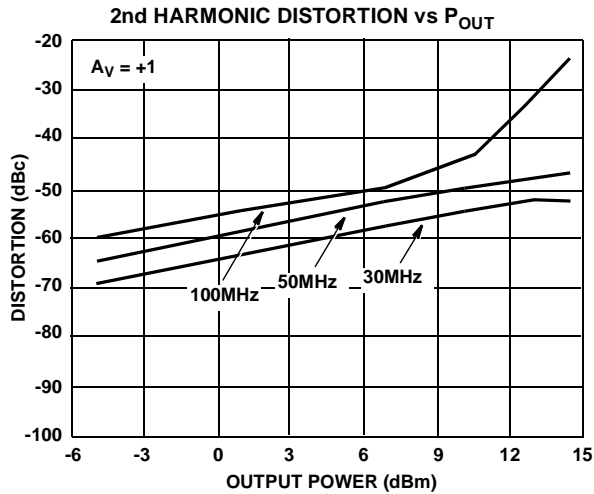
Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_L = 100\Omega$, $T_A = +25^oC$, Unless Otherwise Specified (Continued)

OVERSHOOT vs INPUT RISE TIME

$V_{OUT} = 1V$

$A_V = +1$

$A_V = -1$

$A_V = +2$

OVERSHOOT vs INPUT RISE TIME

$V_{OUT} = 2V$

$A_V = +1$

$A_V = +2$

$A_V = -1$

SUPPLY CURRENT vs SUPPLY VOLTAGE

SUPPLY CURRENT vs TEMPERATURE

OUTPUT VOLTAGE vs TEMPERATURE

$A_V = -1$

$+V_{OUT}$ ($R_L = 50\Omega$)

$+V_{OUT}$ ($R_L = 100\Omega$)

$|-V_{OUT}|$ ($R_L = 100\Omega$)

$|-V_{OUT}|$ ($R_L = 50\Omega$)

INPUT NOISE CHARACTERISTICS

eni

ini

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DESIGN INFORMATION (Continued)

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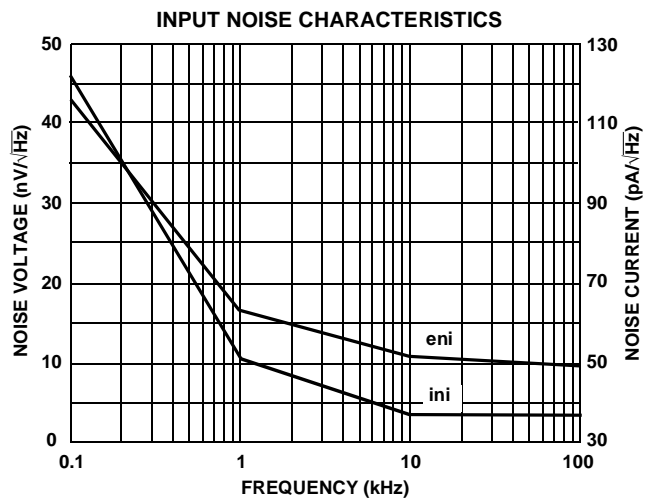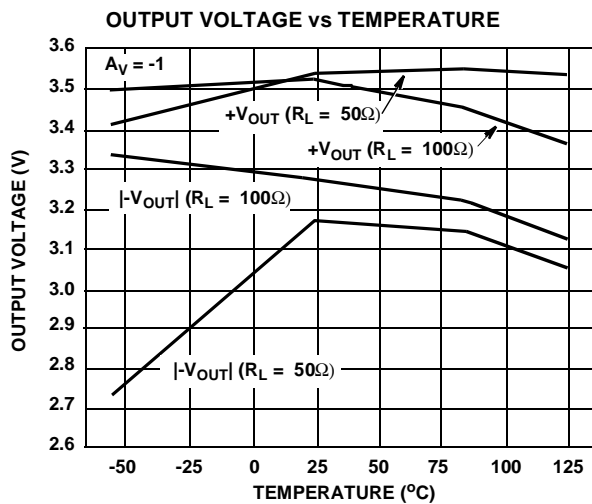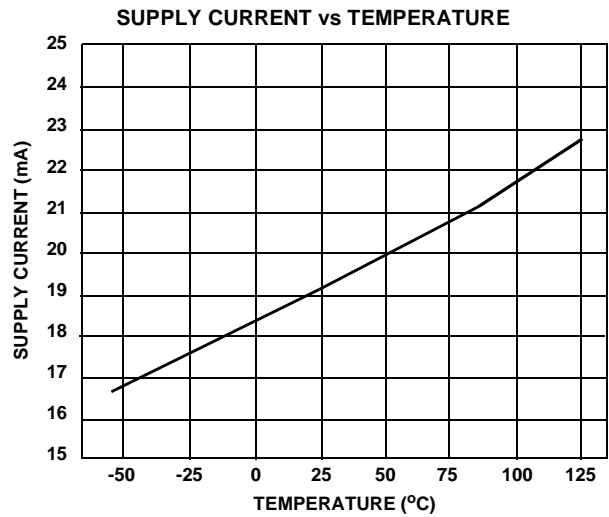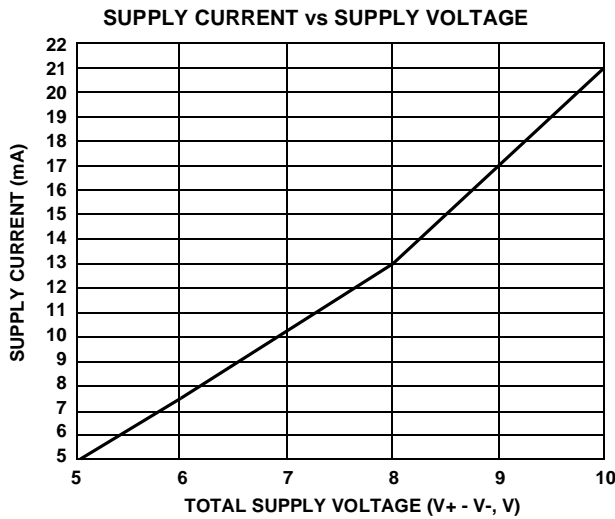
Application Information

Closed Loop Gain Selection

The HFA1112 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 50Ω, C_L = 30pF, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at A_V = +1, R_S = 5Ω, C_L = 340pF.
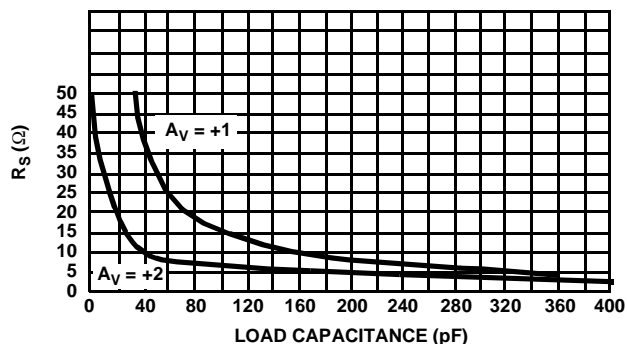

FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1112 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R2), and leave the connection open.

2. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards, please contact your local sales office.
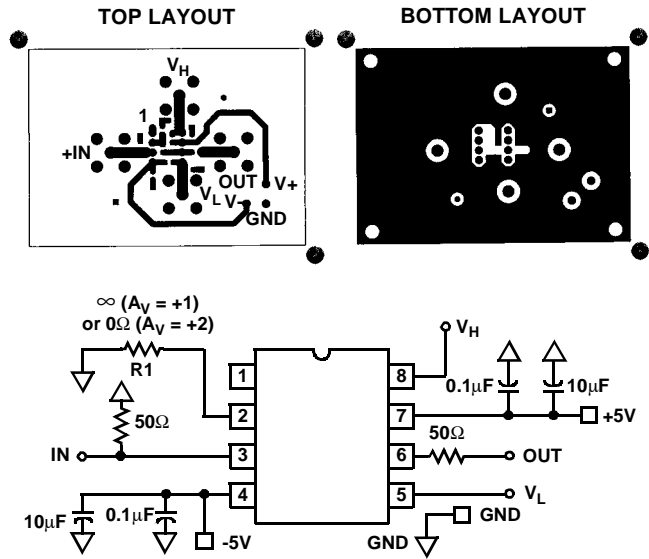
TOP LAYOUT   **BOTTOM LAYOUT**

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

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DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS
Device Characterized at: V_{SUPPLY} = ±5V, A_V = +1V/V, R_L = 100Ω, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Output Offset Voltage	V_{CM} = 0V	+25°C	8	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	µV/°C
+Input Current	V_{CM} = 0V	+25°C	25	µA
+Input Resistance	ΔV_{CM} = 2V	+25°C	50	kΩ
+Input Noise Voltage	f = 100kHz	+25°C	9	nV/$\sqrt{Hz}$
+Input Noise Current	f = 100kHz	+25°C	37	pA/$\sqrt{Hz}$
Input Common Mode Range		Full	±2.8	V
Gain	A_V = +1, V_{IN} = 2V	+25°C	0.99	V/V
Gain	A_V = +2, V_{IN} = 1V	+25°C	1.98	V/V
DC Non-Linearity	A_V = +2, ±2V Full Scale	+25°C	0.02	%
Output Current	A_V = -1, R_L = 50Ω	+25°C to +125°C	±60	mA
	A_V = -1, R_L = 50Ω	-55°C to 0°C	±50	mA
DC Closed Loop Output Resistance	A_V = +2	+25°C	0.3	Ω
Quiescent Supply Current	R_L = Open	Full	24	mA
-3dB Bandwidth	A_V = -1, V_{OUT} = 200mV_{P-P}	+25°C	800	MHz
	A_V = +1, V_{OUT} = 200mV_{P-P}	+25°C	850	MHz
	A_V = +2, V_{OUT} = 200mV_{P-P}	+25°C	550	MHz
Slew Rate	A_V = -1, V_{OUT} = 5V_{P-P}	+25°C	2400	V/µs
	A_V = +1, V_{OUT} = 5V_{P-P}	+25°C	1500	V/µs
	A_V = +2, V_{OUT} = 5V_{P-P}	+25°C	1900	V/µs
Full Power Bandwidth	A_V = -1, V_{OUT} = 5V_{P-P}	+25°C	300	MHz
	A_V = +1, V_{OUT} = 5V_{P-P}	+25°C	150	MHz
	A_V = +2, V_{OUT} = 5V_{P-P}	+25°C	220	MHz
Gain Flatness	To 30MHz, A_V = -1	+25°C	±0.02	dB
	To 30MHz, A_V = +1	+25°C	±0.10	dB
	To 30MHz, A_V = +2	+25°C	±0.015	dB
Gain Flatness	To 50MHz, A_V = -1	+25°C	±0.05	dB
	To 50MHz, A_V = +1	+25°C	±0.20	dB
	To 50MHz, A_V = +2	+25°C	±0.036	dB
Gain Flatness	To 100MHz, A_V = -1	+25°C	±0.10	dB
	To 100MHz, A_V = +2	+25°C	±0.07	dB
Linear Phase Deviation	To 100MHz, A_V = -1	+25°C	±0.13	Degrees
	To 100MHz, A_V = +1	+25°C	±0.83	Degrees
	To 100MHz, A_V = +2	+25°C	±0.05	Degrees
2nd Harmonic Distortion	30MHz, A_V = -1, V_{OUT} = 2V_{P-P}	+25°C	-52	dBc
	30MHz, A_V = +1, V_{OUT} = 2V_{P-P}	+25°C	-57	dBc
	30MHz, A_V = +2, V_{OUT} = 2V_{P-P}	+25°C	-52	dBc

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DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS
Device Characterized at: V_{SUPPLY} = ±5V, A_V = +1V/V, R_L = 100Ω, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
3rd Harmonic Distortion	30MHz, A_V = -1, V_{OUT} = 2V_{P-P}	+25°C	-71	dBc
	30MHz, A_V = +1, V_{OUT} = 2V_{P-P}	+25°C	-73	dBc
	30MHz, A_V = +2, V_{OUT} = 2V_{P-P}	+25°C	-72	dBc
2nd Harmonic Distortion	50MHz, A_V = -1, V_{OUT} = 2V_{P-P}	+25°C	-47	dBc
	50MHz, A_V = +1, V_{OUT} = 2V_{P-P}	+25°C	-53	dBc
	50MHz, A_V = +2, V_{OUT} = 2V_{P-P}	+25°C	-47	dBc
3rd Harmonic Distortion	50MHz, A_V = -1, V_{OUT} = 2V_{P-P}	+25°C	-63	dBc
	50MHz, A_V = +1, V_{OUT} = 2V_{P-P}	+25°C	-68	dBc
	50MHz, A_V = +2, V_{OUT} = 2V_{P-P}	+25°C	-65	dBc
2nd Harmonic Distortion	100MHz, A_V = -1, V_{OUT} = 2V_{P-P}	+25°C	-41	dBc
	100MHz, A_V = +1, V_{OUT} = 2V_{P-P}	+25°C	-50	dBc
	100MHz, A_V = +2, V_{OUT} = 2V_{P-P}	+25°C	-42	dBc
3rd Harmonic Distortion	100MHz, A_V = -1, V_{OUT} = 2V_{P-P}	+25°C	-55	dBc
	100MHz, A_V = +1, V_{OUT} = 2V_{P-P}	+25°C	-49	dBc
	100MHz, A_V = +2, V_{OUT} = 2V_{P-P}	+25°C	-62	dBc
3rd Order Intercept	100MHz, A_V = +2	+25°C	28	dBm
	300MHz, A_V = +2	+25°C	13	dBm
1dB Compression	100MHz, A_V = +2	+25°C	19	dBm
	300MHz, A_V = +2	+25°C	12	dBm
Reverse Isolation (S_{12})	40MHz	+25°C	-70	dB
	100MHz	+25°C	-60	dB
	600MHz	+25°C	-32	dB
Rise & Fall Time	A_V = -1, V_{OUT} = 0.5V_{P-P}	+25°C	500	ps
	A_V = +1, V_{OUT} = 0.5V_{P-P}	+25°C	480	ps
	A_V = +2, V_{OUT} = 0.5V_{P-P}	+25°C	700	ps
Overshoot	A_V = -1, V_{OUT} = 0.5V_{P-P}	+25°C	12	%
	A_V = +1, V_{OUT} = 0.5V_{P-P}	+25°C	45	%
	A_V = +2, V_{OUT} = 0.5V_{P-P}	+25°C	6	%
Settling Time	A_V = +2, to 0.1%, V_{OUT} = 2V to 0V	+25°C	13	ns
	A_V = +2, to 0.05%, V_{OUT} = 2V to 0V	+25°C	20	ns
	A_V = +2, to 0.02%, V_{OUT} = 2V to 0V	+25°C	36	ns
Overdrive Recovery Time	A_V = +2, V_{IN} = 5V_{P-P}	+25°C	8.5	ns
Differential Gain	A_V = +2, R_L = 150Ω, NTSC	+25°C	0.02	%
Differential Phase	A_V = +2, R_L = 150Ω, NTSC	+25°C	0.04	Degrees