Data Sheet | May 2003 | FN4727.3

Triple, 560MHz, Low Power, Video Operational Amplifier

The HFA1305 is a triple, high speed, low power current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 process.

These amplifiers deliver up to 560MHz bandwidth and 2500V/μs slew rate, on only 58mW of quiescent power. They are specifically designed to meet the performance, power, and cost requirements of high volume video applications. The excellent gain flatness and differential gain/phase performance make these amplifiers well suited for component or composite video applications. Video performance is maintained even when driving a double terminated cable (R_L = 150Ω), and degrades only slightly when driving two double terminated cables (R_L = 75Ω). RGB applications will benefit from the high slew rates, and high full power bandwidth.

The HFA1305 is a pin compatible, low power, high performance upgrade for the popular Intersil HA5013, and for the AD8073 and CLC5623, in ±5V applications.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1305IB	-40 to 85	14 Ld SOIC	M14.15
HA5025EVAL (Note)	High Speed Op Amp SOIC Evaluation Board		

NOTE: Requires a SOIC-to-DIP adapter. See "Evaluation Board" section inside.

Features

- Low Supply Current . . . . . 5.8mA/Op Amp
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth (A_V = +2) 560MHz
- Very Fast Slew Rate 2500V/μs
- Gain Flatness (to 50MHz) . . . . . ±0.03dB
- Differential Gain 0.02%
- Differential Phase . . . . . 0.03 Degrees
- All Hostile Crosstalk (5MHz) . . . . . -60dB
- Pin Compatible Upgrade to HA5013, AD8073 and CLC5623 in ±5V Supply Applications.

Applications

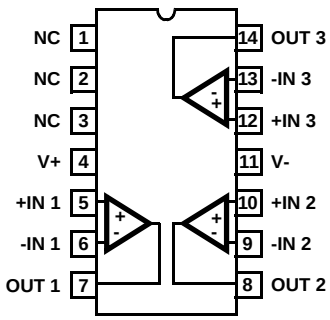
- Flash A/D Drivers
- Professional Video Processing
- Video Digitizing Boards/Systems
- Computer Video Plug-In Boards
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Pinout

HFA1305 (SOIC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (Note 2) . . . . . Short Circuit Protected
30mA Continuous
60mA $\leq$ 50% Duty Cycle
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	120

Moisture Sensitivity (see Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	$\mu V/^oC$
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	45	48	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	43	46	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	48	52	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	46	48	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	46	48	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	μA
		A	Full	-	10	25	μA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	$nA/^oC$
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	$\mu A/V$
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	$\mu A/V$
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	$\mu A/V$
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	1.2	-	$M\Omega$
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	0.8	-	$M\Omega$
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	0.8	-	$M\Omega$
Inverting Input Bias Current		A	25	-	2	7.5	μA
		A	Full	-	5	15	μA
Inverting Input Bias Current Drift		B	Full	-	60	200	$nA/^oC$
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	$\mu A/V$
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	$\mu A/V$
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	$\mu A/V$

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	60	-	Ω
Input Capacitance		B	25	-	1.4	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS Tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain		C	25	-	500	-	kΩ
AC CHARACTERISTICS (Note 3)							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Notes 3, 5)	A_V = +1	B	25	-	375	-	MHz
	A_V = -1	B	25	-	420	-	MHz
	A_V = +2	B	25	-	560	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P}, Notes 3, 5)	A_V = +1	B	25	-	160	-	MHz
	A_V = -1	B	25	-	260	-	MHz
	A_V = +2	B	25	-	165	-	MHz
Gain Flatness (V_{OUT} = 0.2V_{P-P}, Notes 3, 5)	A_V = +1, To 25MHz	B	25	-	±0.03	-	dB
	A_V = +1, To 50MHz	B	25	-	±0.03	-	dB
	A_V = +1, To 100MHz	B	25	-	±0.07	-	dB
	A_V = -1, To 25MHz	B	25	-	±0.03	-	dB
	A_V = -1, To 50MHz	B	25	-	±0.04	-	dB
	A_V = -1, To 100MHz	B	25	-	±0.09	-	dB
	A_V = +2, To 25MHz	B	25	-	±0.03	-	dB
	A_V = +2, To 50MHz	B	25	-	±0.03	-	dB
	A_V = +2, To 100MHz	B	25	-	±0.07	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk (A_V = +1, All Channels Hostile, Note 5)	5MHz	B	25	-	-60	-	dB
	10MHz	B	25	-	-56	-	dB
OUTPUT CHARACTERISTICS A_V = +2 (Note 3), Unless Otherwise Specified							
Output Voltage Swing (Note 5)	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 5)	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Impedance		B	25	-	0.2	-	Ω

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Second Harmonic Distortion (V_{OUT} = $2V_{P-P}$, Note 5)	10MHz	B	25	-	-51	-	dBc
	20MHz	B	25	-	-46	-	dBc
Third Harmonic Distortion (V_{OUT} = $2V_{P-P}$, Note 5)	10MHz	B	25	-	-63	-	dBc
	20MHz	B	25	-	-56	-	dBc
TRANSIENT CHARACTERISTICS A_V = +2 (Note 3), Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = $0.5V_{P-P}$, Note 3)	A_V = +1	B	25	-	1.0	-	ns
	A_V = -1	B	25	-	-	-	ns
	A_V = +2	B	25	-	0.8	-	ns
Overshoot (V_{OUT} = $0.5V_{P-P}$, V_{IN} t_{RISE} = 1ns, Notes 3, 6)	A_V = +1, +OS	B	25	-	5	-	%
	A_V = +1, -OS	B	25	-	11	-	%
	A_V = -1, +OS	B	25	-	7	-	%
	A_V = -1, -OS	B	25	-	8	-	%
	A_V = +2, +OS	B	25	-	5	-	%
	A_V = +2, -OS	B	25	-	10	-	%
Slew Rate (V_{OUT} = $5V_{P-P}$ at A_V = +2, -1, V_{OUT} = $4V_{P-P}$, at A_V = +1, Notes 3, 5)	A_V = +1, +SR	B	25	-	1230	-	V/µs
	A_V = +1, -SR	B	25	-	1350	-	V/µs
	A_V = -1, +SR	B	25	-	2500	-	V/µs
	A_V = -1, -SR	B	25	-	1900	-	V/µs
	A_V = +2, +SR	B	25	-	1700	-	V/µs
	A_V = +2, -SR	B	25	-	1700	-	V/µs
Settling Time (V_{OUT} = +2V to 0V Step, Note 5)	To 0.1%	B	25	-	23	-	ns
	To 0.05%	B	25	-	30	-	ns
	To 0.025%	B	25	-	37	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2 (Note 3), Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.06	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 5)		A	25	-	5.8	6.1	mA/Op Amp
		A	Full	-	5.9	6.3	mA/Op Amp

NOTES:

3. The optimum feedback resistor depends on closed loop gain. See the “Optimum Feedback Resistor” table in the Application Information section for details.
4. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
5. See Typical Performance Curves for more information.
6. Undershoot dominates for output signal swings below GND (e.g., $2V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 2V condition. See the “Application Information” section for details.

Application Information

Performance

The amplifiers comprising the HFA1305 are high frequency current feedback amplifiers. As such, they are sensitive to feedback capacitance which destabilizes the op amp and causes overshoot and peaking. Unfortunately, the standard triple op amp pinout places the amplifier's output next to its inverting input, thus making the package capacitance an unavoidable parasitic feedback capacitor.

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1305 design is optimized for R_F = 510Ω (SOIC) at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). However, at higher gains the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better.

OPTIMUM FEEDBACK RESISTOR

GAIN (A_{CL})	R_F (Ω) SOIC	BANDWIDTH (MHz) SOIC
-1	360	420
+1	464 (+R_S = 649)	375
+2	510	560
+5	200	330
+10	180	140

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥ 50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot

The HFA1305 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figure 6). This undershoot isn't present for small bipolar signals, or large positive signals (see Figure 4 and Figure 5).

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and eventual instability. To reduce this capacitance the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 560MHz. By decreasing R_S as C_L increases (as illustrated in the curve), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases.

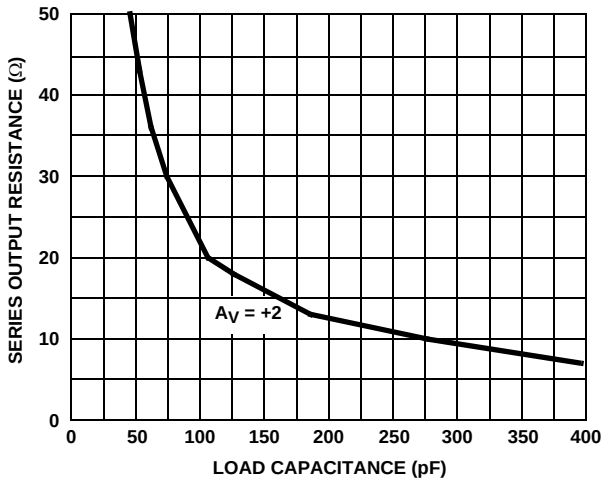


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1305IB (SOIC) may be evaluated using the HA5025 Evaluation Board and a SOIC to DIP adaptor like the Aries Electronics Part Number 14-350000-10.

The schematic for the SOIC amplifier 1 and the HA5025EVAL board layout are shown in Figure 2 and Figure 3. Resistors R_F, R_G, and $+R_S$ may require a change to values applicable to the HFA1305IB.

To order evaluation board (part number HA5025EVAL), please contact your local sales office.

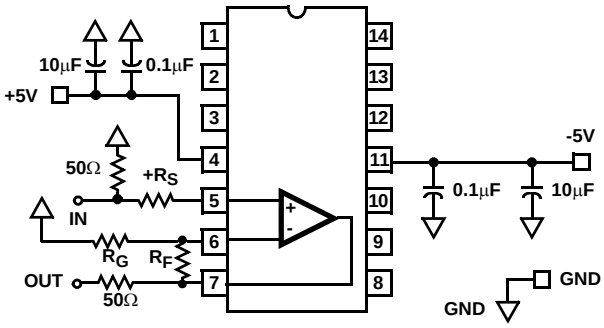
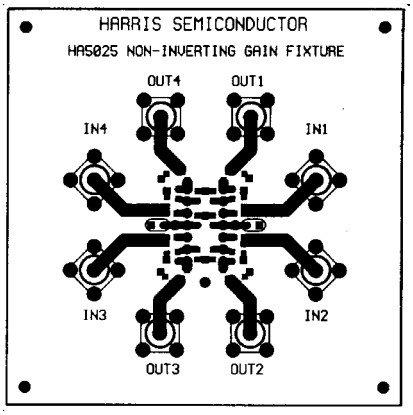


FIGURE 2. EVALUATION BOARD SCHEMATIC FOR SOIC

TOP LAYOUT



BOTTOM LAYOUT

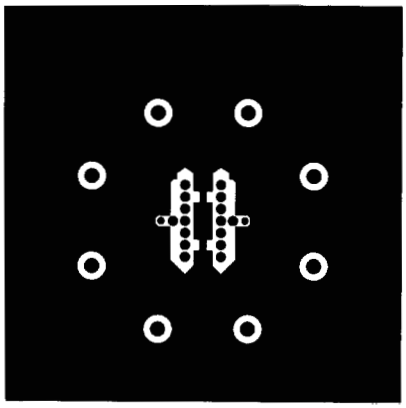


FIGURE 3. EVALUATION BOARD LAYOUT FOR SOIC

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified

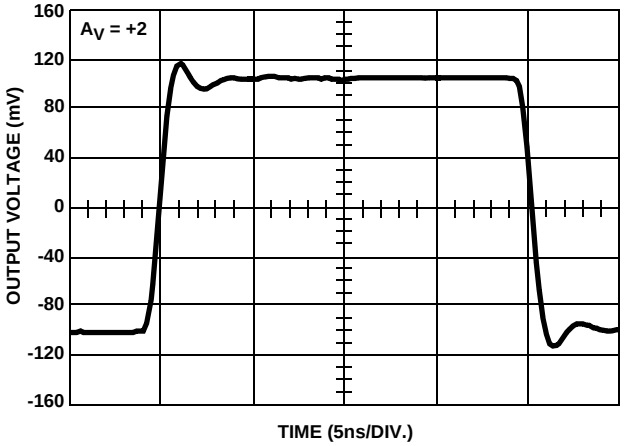


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

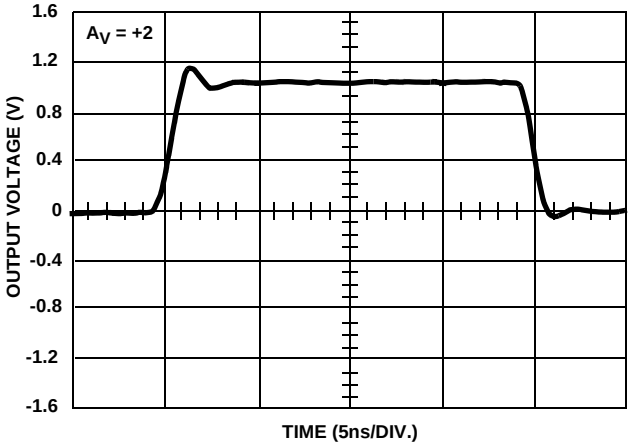


FIGURE 5. LARGE SIGNAL POSITIVE PULSE RESPONSE

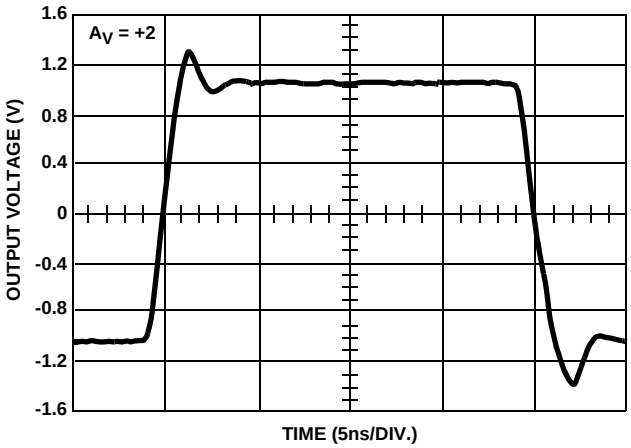


FIGURE 6. LARGE SIGNAL BIPOLAR PULSE RESPONSE

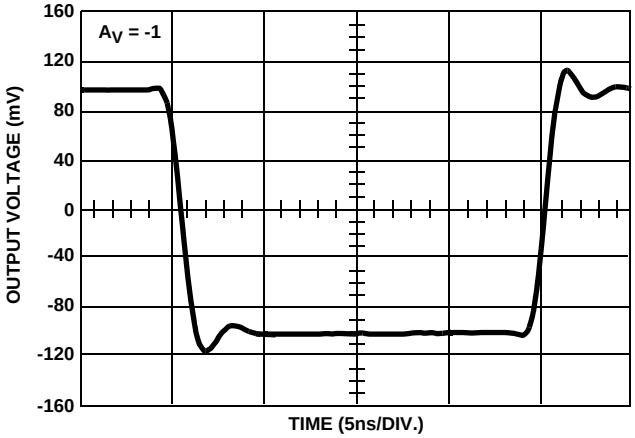


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

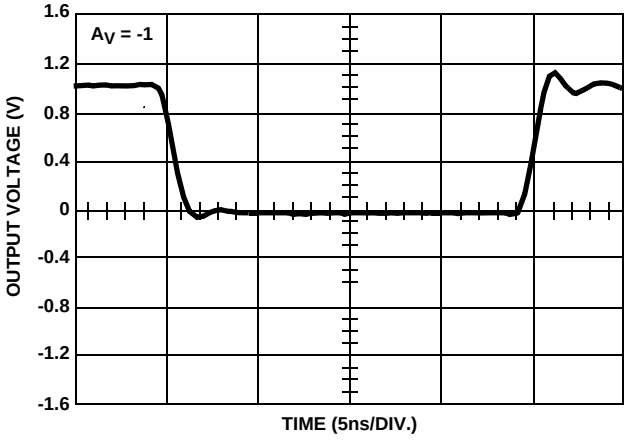


FIGURE 8. LARGE SIGNAL POSITIVE PULSE RESPONSE

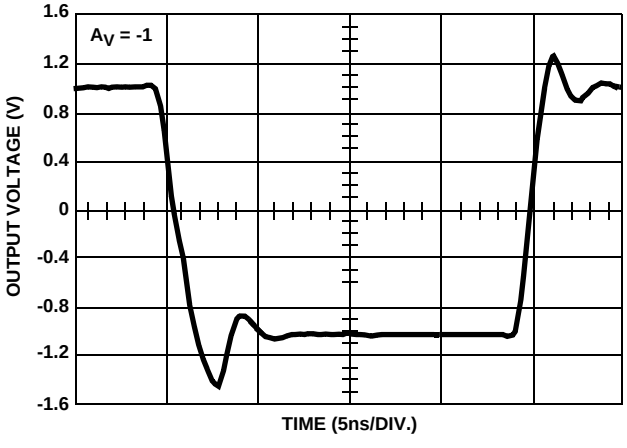


FIGURE 9. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

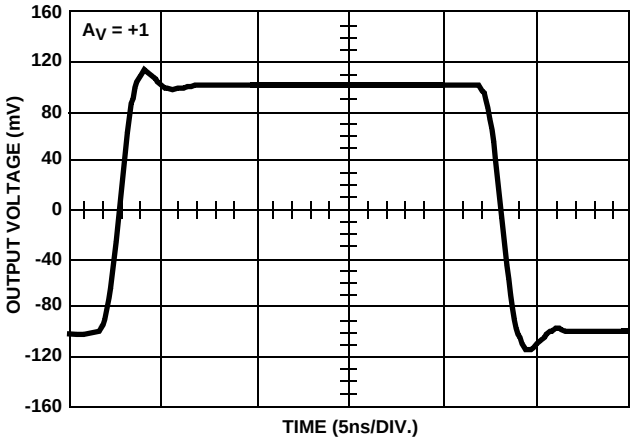


FIGURE 10. SMALL SIGNAL PULSE RESPONSE

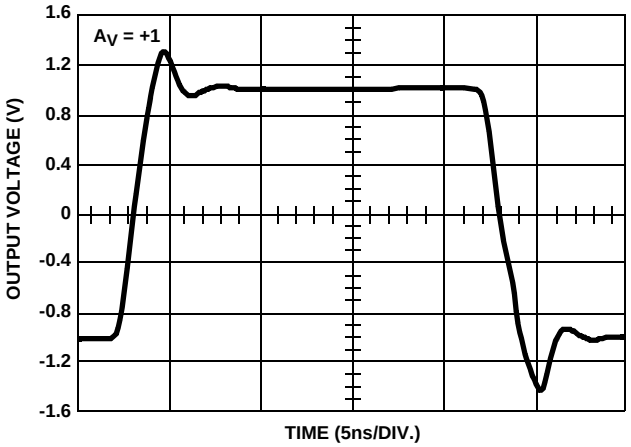


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

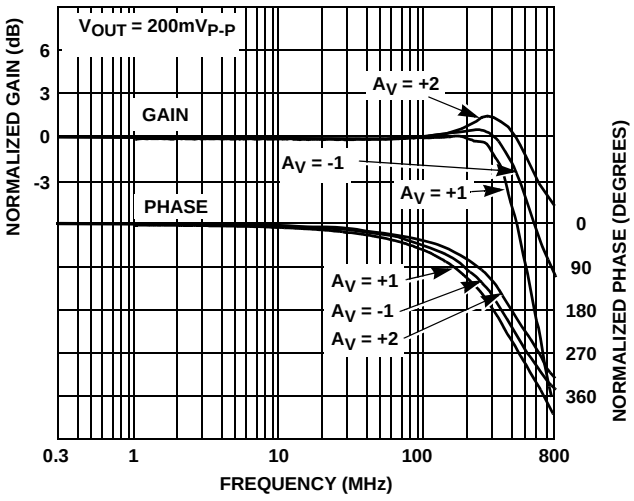


FIGURE 12. FREQUENCY RESPONSE

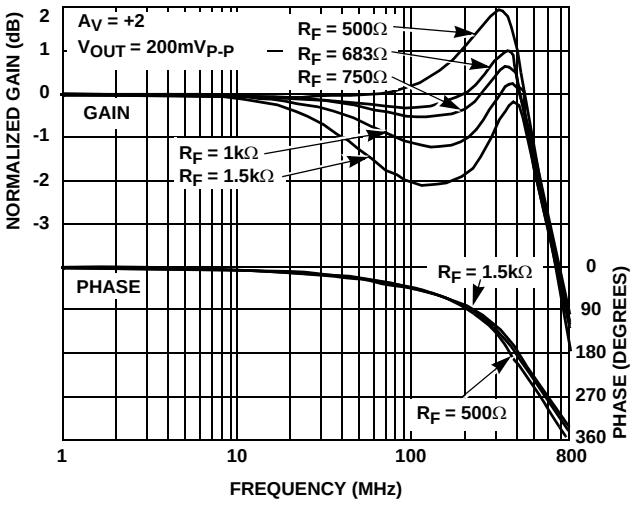


FIGURE 13. FREQUENCY RESPONSE vs FEEDBACK RESISTOR

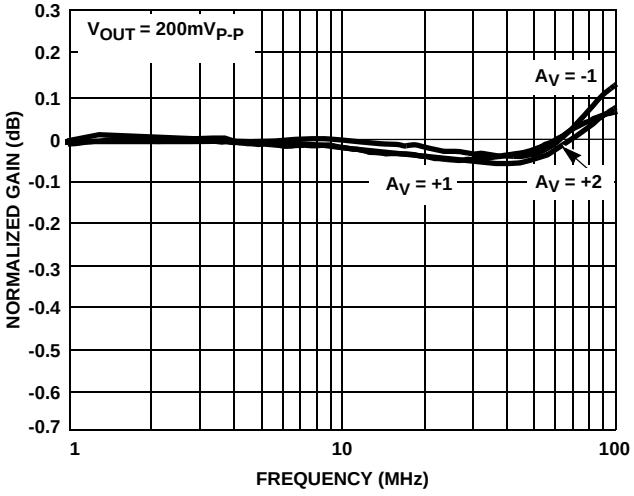


FIGURE 14. GAIN FLATNESS

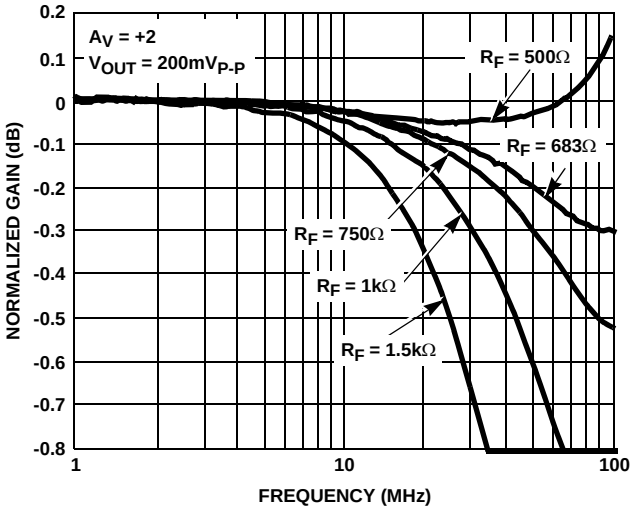


FIGURE 15. GAIN FLATNESS vs FEEDBACK RESISTOR

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

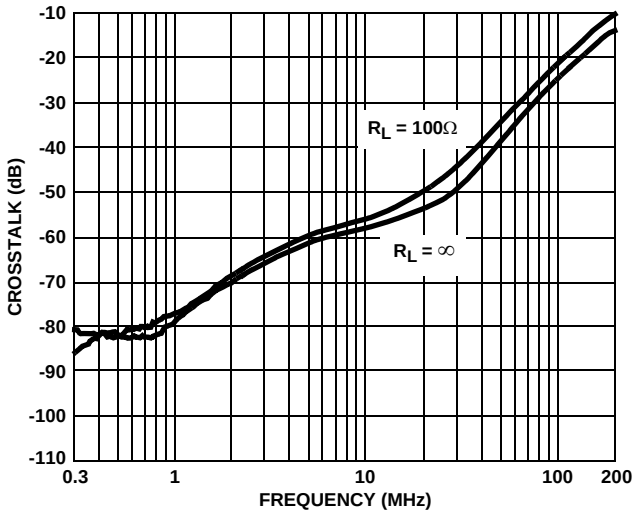


FIGURE 16. ALL HOSTILE CROSSTALK

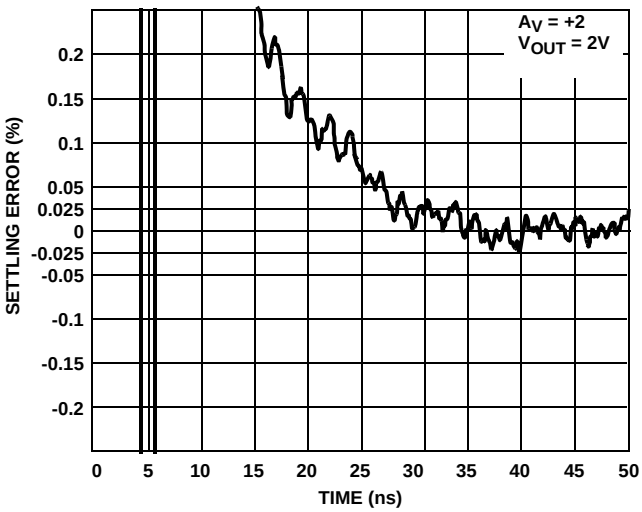


FIGURE 17. SETTLING RESPONSE

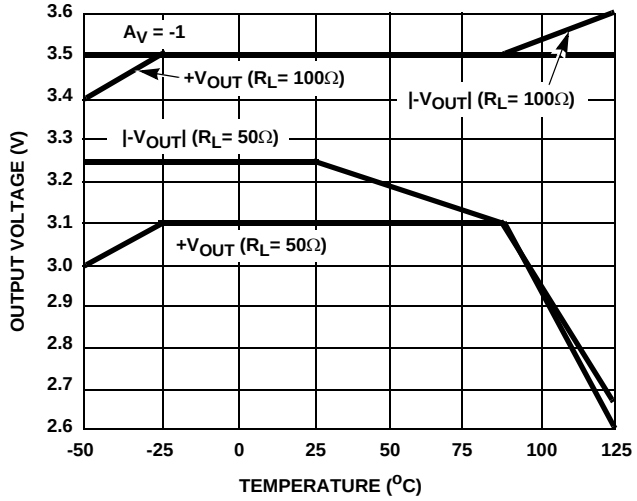


FIGURE 18. OUTPUT VOLTAGE vs TEMPERATURE

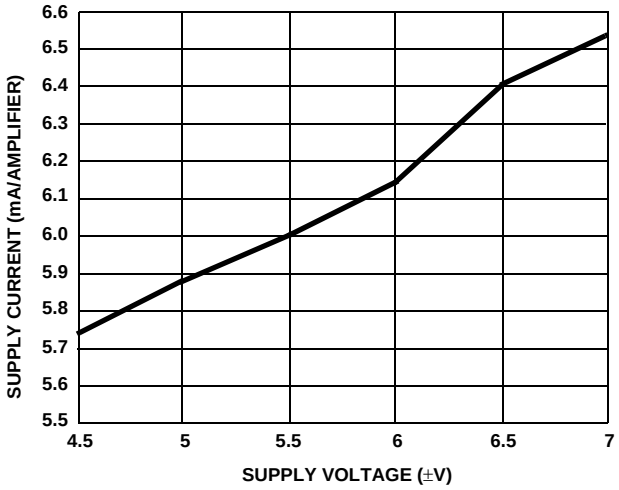


FIGURE 19. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS

79 mils x 118 mils
2000μm x 3000μm

METALLIZATION

Type: Metal 1: AICu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AICu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (POWERED UP)

Floating (Recommend Connection to V-)

PASSIVATION

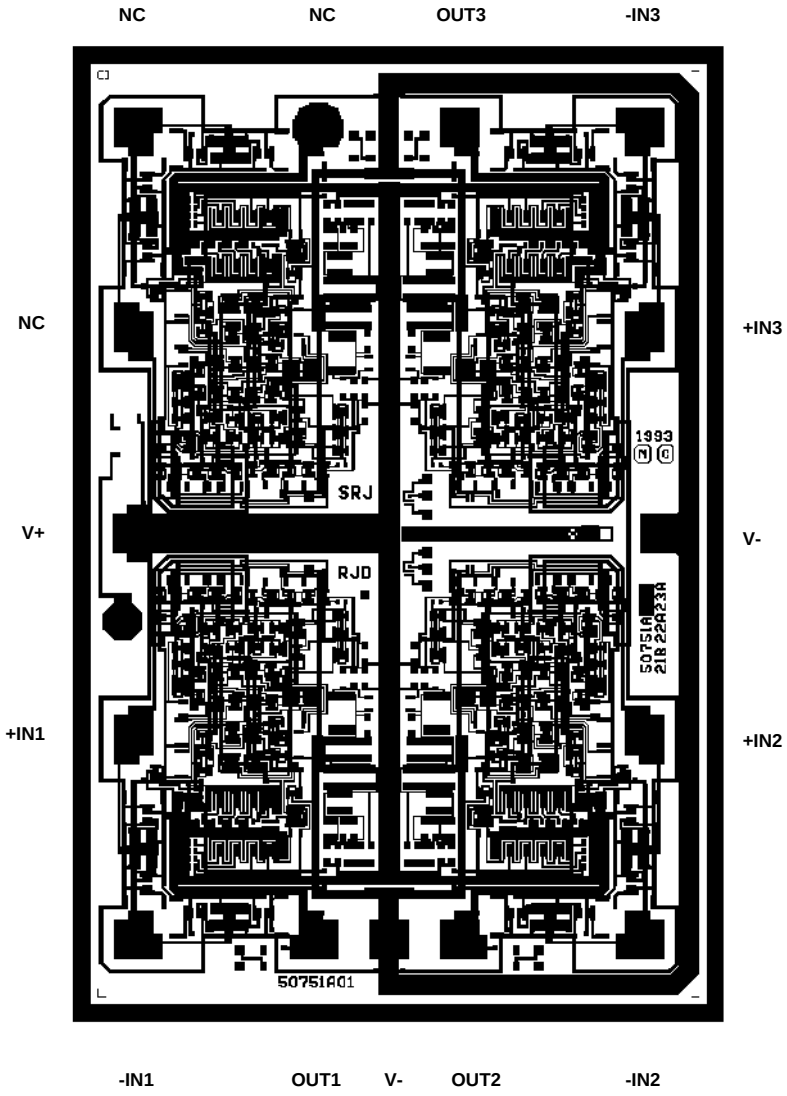
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT

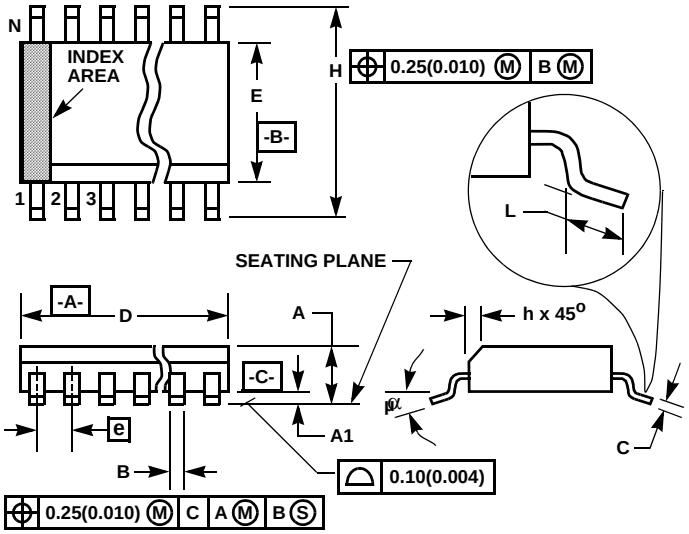
240

Metallization Mask Layout

HFA1305



Small Outline Plastic Packages (SOIC)



M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.