HI1396

OBSOLETE PRODUCT
FOR A POSSIBLE SUBSTITUTE PRODUCT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

September 2000

8-Bit, 125 MSPS, Flash A/D Converter

Features

- Differential Linearity Error ±0.5 LSB (Typ) or Less
- Integral Linearity Error ±0.5 LSB (Typ) or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate of 125 MSPS (Min)
- Low Input Capacitance (Typ) 18pF
- Wide Analog Input Bandwidth (Min for Full Scale Input) 200MHz
- Single Power Supply . . . . . -5.2V
- Low Power Consumption (Typ) 870mW
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50Ω Loads
- Direct Replacement for Sony CXA1396

Applications

- Video Digitizing
- HDTV (High Definition TV)
- Direct RF Down-Conversion
- Communication Systems
- Radar Systems
- Digital Oscilloscopes

Description

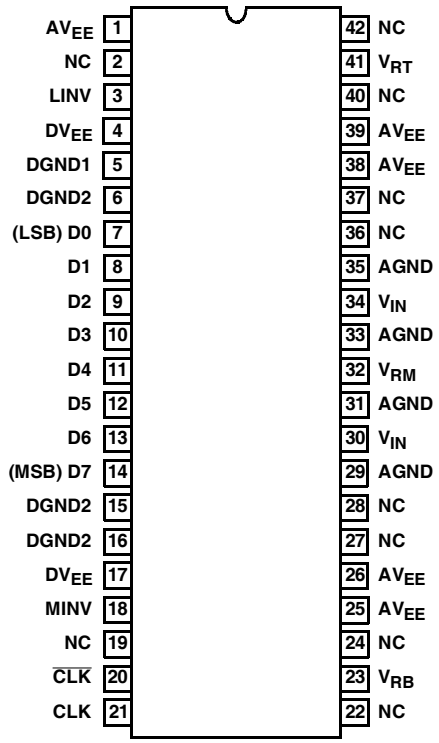
The HI1396 is an 8-bit, ultra high speed flash analog-to-digital converter IC capable of digitizing analog signals at the maximum rate of 125 MSPS. The digital I/O levels of the converter are compatible with ECL 100K/10KH/10K.

Part Number Information

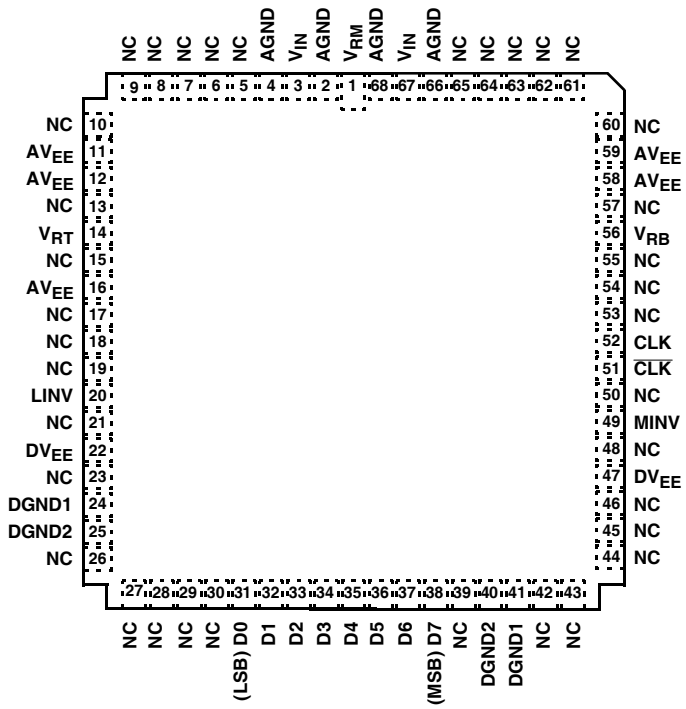
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI1396JCJ	-20 to 75	42 Ld SBDIP	D42.6
HI1396AIL	-20 to 100	68 Ld CLCC	J68.A

Pinouts

HI1396 (SBDIP)
TOP VIEW

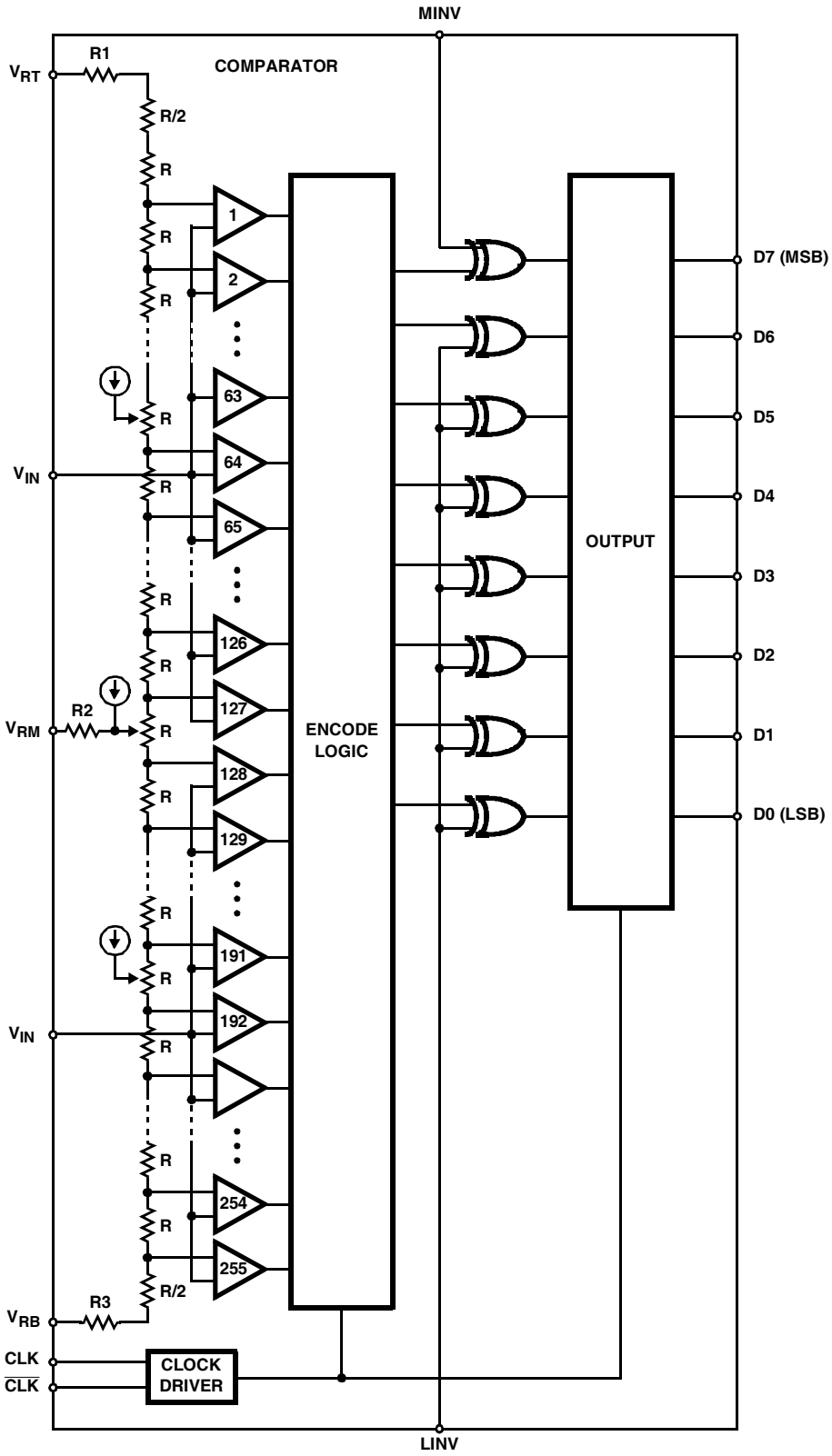


HI1396 (CLCC)
TOP VIEW



File Number **3576.4**

Functional Block Diagram



Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $V_{RT} = 0V$, $V_{RB} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, INL HI1396JCJ, HI1396AIL	f_C = 125 MSPS	-	±0.3	±0.5	LSB
Differential Linearity Error, DNL HI1396JCJ, HI1396AIL	f_C = 125 MSPS	-	-	±0.5	LSB
ANALOG INPUT					
Input Bandwidth	$V_{IN} = 2V_{P-P}$	200	-	-	MHz
Analog Input Capacitance, C_{IN}	$V_{IN} = 1V + 0.07V_{RMS}$	-	17	-	pF
Analog Input Resistance, R_{IN}		50	190	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	20	130	400	µA
REFERENCE INPUTS					
Reference Resistance, R_{REF}		75	110	155	Ω
Offset Voltage E_{OT} V_{RT}		8	19	32	mV
E_{OB} V_{RB}		0	15	24	mV
DIGITAL INPUTS					
Logic H Level, V_{IH}		-1.13	-	-	V
Logic L Level, V_{IL}		-	-	-1.50	V
Logic H Current, I_{IH}	Input Connected to -0.8V	0	-	50	µA
Logic L Current, I_{IL}	Input Connected to -1.6V	0	-	50	µA
Input Capacitance		-	7	-	pF
DIGITAL OUTPUTS					
Logic H Level, V_{OH}	R_L = 50Ω to -2V	-1.10	-	-	V
Logic L Level, V_{OL}	R_L = 50Ω to -2V	-	-	-1.62	V
TIMING CHARACTERISTICS					
Output Rise Time, t_r	R_L = 50Ω to -2V, 20% to 80%	0.5	0.9	1.2	ns
Output Fall Time, t_f	R_L = 50Ω to -2V, 20% to 80%	0.5	1.0	1.3	ns
Output Delay, t_{OD}		3.0	3.6	4.2	ns
H Pulse Width of Clock, t_{PW1}		4.0	-	-	ns
L Pulse Width of Clock, t_{PW0}		4.0	-	-	ns
DYNAMIC CHARACTERISTICS					
Maximum Conversion Rate, f_C	Error Rate 10^{-9} TPS (Note 2)	125	-	-	MSPS
Aperture Jitter, t_{AJ}		-	10	-	ps
Sampling Delay, t_{DS}		-	1.5	-	ns
Signal to Noise Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1MHz, Full Scale f_C = 125 MSPS	-	46	-	dB
	Input = 31.5MHz, Full Scale f_C = 125 MSPS	-	40	-	dB
Error Rate	Input = 31.249MHz, Full Scale Error > 16 LSB, f_C = 125 MSPS	-	-	10^{-9}	TPS (Note 2)
Differential Gain Error, DG	NTSC 40 IRE Mod. Ramp, f_C = 125 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{EE}		-230	-160	-	mA
Power Consumption	Note 3	-	870	-	mW

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $V_{RT} = 0V$, $V_{RB} = -2V$ (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. TPS: Times Per Sample.
3. $P_D = I_{EE} \bullet V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$
4. T_A specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed.

Timing Diagram

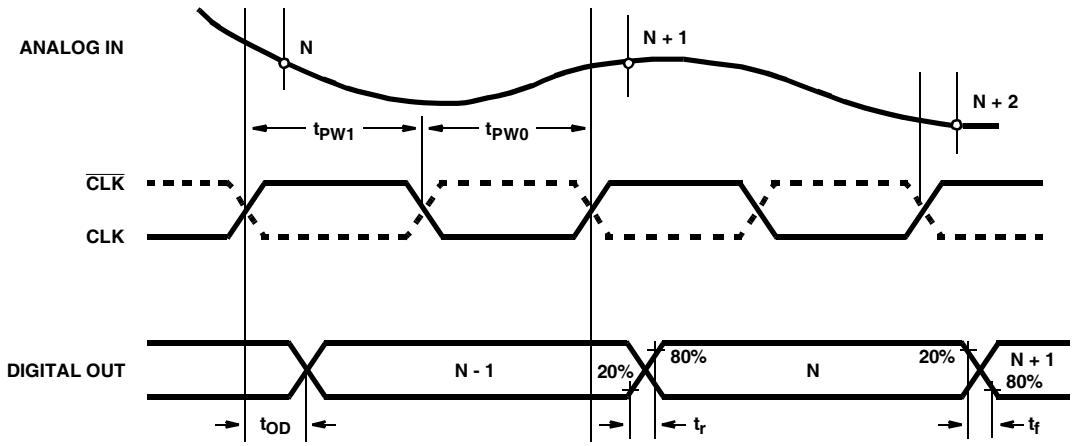
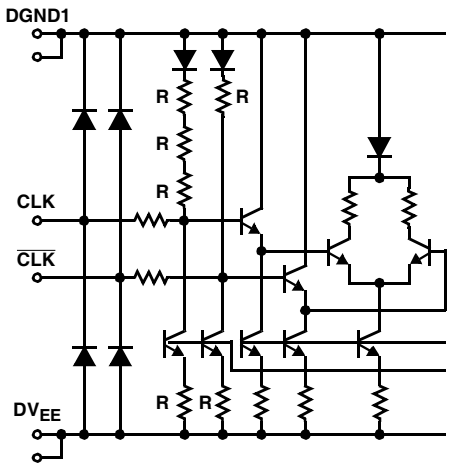
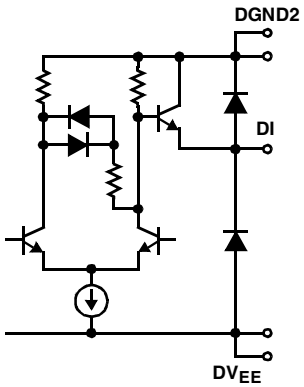


FIGURE 1.

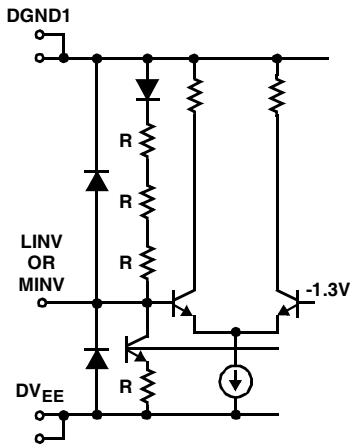
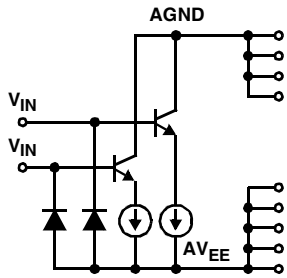
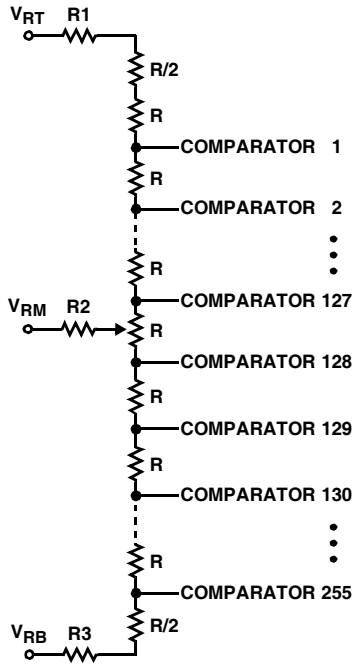
Pin Descriptions and I/O Pin Equivalent Circuits

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
29, 31, 33, 35	49, 51, 53, 55	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND1, DGND2.
1, 25, 26, 38, 39	41, 42, 62, 63, 67	AV_{EE}	-	-5.2V		Analog V_{EE} -5.2V (Typ). Internally connected to DV_{EE} (Resistance: 4Ω to 6Ω). Bypass with 0.1μF to AGND.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
21	35	CLK	I	ECL		CLK Input.
20	34	$\overline{CLK}$				Input complementary to CLK. When left open pulled down to -1.3V. Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain stable high speed operation.
5, 16	7, 24	DGND1	-	0V		Digital GND for internal circuits.
6, 15	8, 23	DGND2	-	0V		Digital GND for output transistors.
4, 17	5, 30	DV_{EE}	-	-5.2V		Digital V_{EE}. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω). Bypass with 0.1µF to DGND
7	14	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
8	15	D1				Data outputs. External pull-down resistors are required.
9	16	D2				
10	17	D3				
11	18	D4				
12	19	D5				
13	20	D6				
14	21	D7				MSB of data outputs. External pull-down resistor is required.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
3	3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see A/D Output Code Table). Pulled low when left open.
18	32	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see A/D Output Code Table). Pulled low when left open.
30, 34	50, 54	V_{IN}	I	V_{RT} to V_{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected.
23	39	V_{RB}	I	-2V		Reference voltage (bottom). Typically -2V. Bypass with a 0.1µF and 10µF to AGND.
32	52	V_{RM}	I	$V_{RB}/2$		Reference voltage mid point. Can be used as a pin for integral linearity compensation.
41	65	V_{RT}	I	0V		Reference voltage (top) typically 0V. When a voltage different from AGND is applied to this pin, bypass with a 0.1µF and 10µF to AGND.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	1, 2, 4, 6, 9-13, 25-29, 31, 33, 36-38, 40, 43-48, 56-61, 64, 66, 68	NC	-	-		Unused pins. No internal connections have been made to these pins. Connecting them to AGND or DGND on PC board is recommended.

A/D OUTPUT CODE TABLE

V_{IN} (Note 5)	STEP	MINV 1, LINV 1		0, 1		1, 0		0, 0	
		D7	D0	D7	D0	D7	D0	D7	D0
0V		000 • • • • • 00		100 • • • • • 00		011 • • • • • 11		111 • • • • • 11	
	0	000 • • • • • 00		100 • • • • • 00		011 • • • • • 11		111 • • • • • 11	
	1	000 • • • • • 01		100 • • • • • 01		011 • • • • • 10		111 • • • • • 10	
		• • •		• • •		• • •		• • •	
-1V	127	011 • • • • • 11		111 • • • • • 11		000 • • • • • 00		100 • • • • • 00	
	128	100 • • • • • 00		000 • • • • • 00		111 • • • • • 11		011 • • • • • 11	
		• • •		• • •		• • •		• • •	
	254	111 • • • • • 10		011 • • • • • 10		100 • • • • • 01		000 • • • • • 01	
	255	111 • • • • • 11		011 • • • • • 11		100 • • • • • 00		000 • • • • • 00	
-2V		111 • • • • • 11		011 • • • • • 11		100 • • • • • 00		000 • • • • • 00	

NOTE:

5. V_{RT} = 0V, V_{RB} = -2V.

Test Circuits

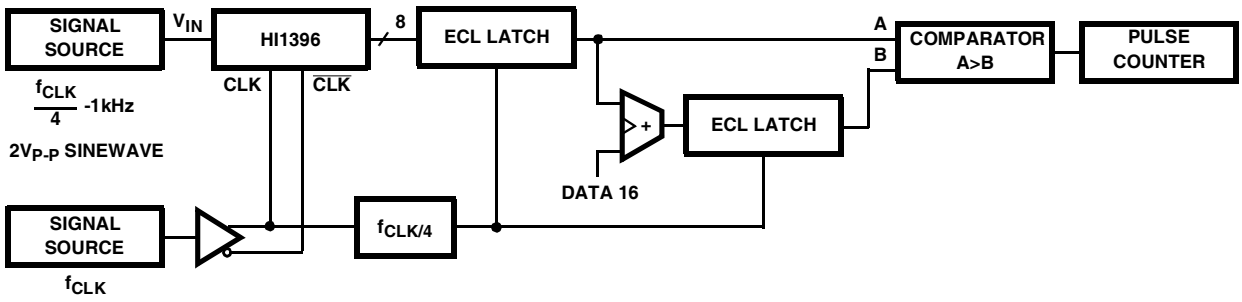


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

Test Circuits (Continued)

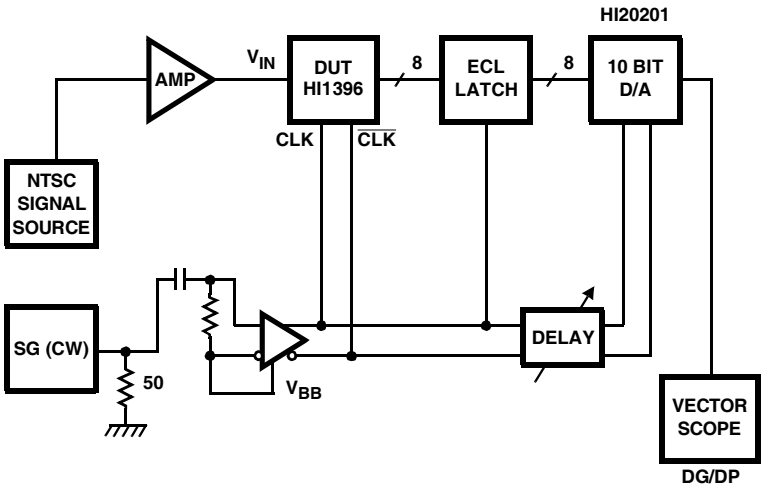


FIGURE 3. DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

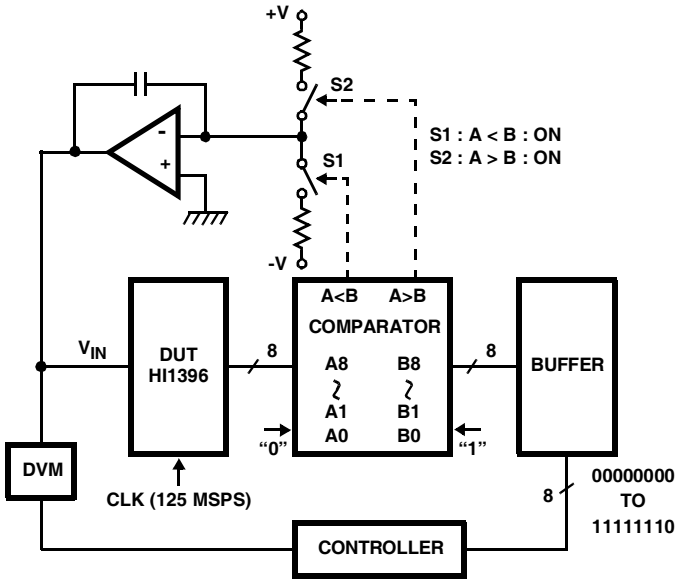


FIGURE 4. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

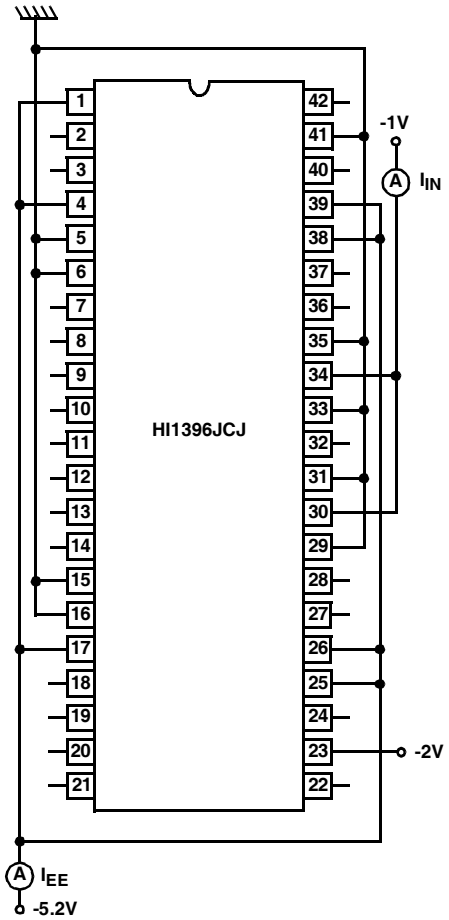


FIGURE 5A.

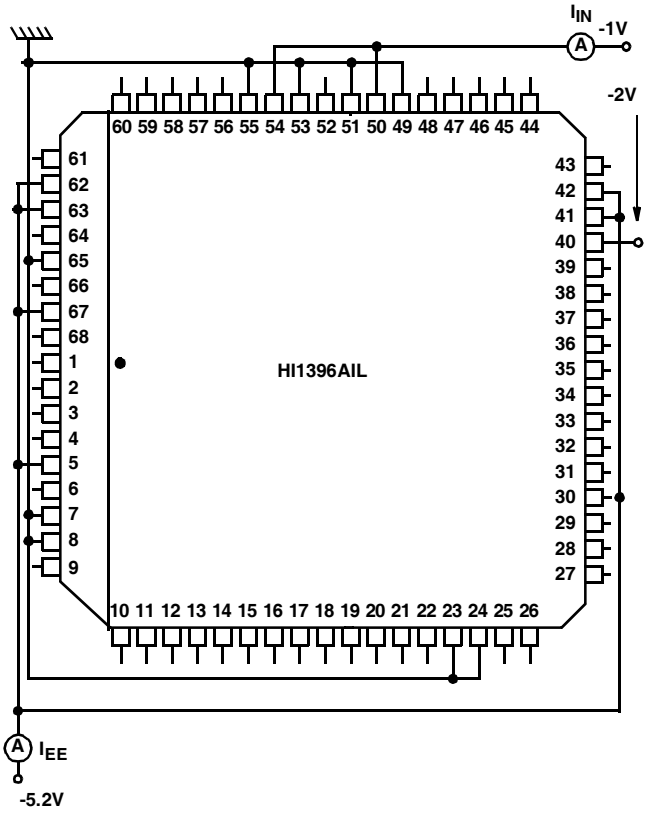


FIGURE 5B.

FIGURE 5. ANALOG INPUT BIAS AND POWER SUPPLY CURRENT TEST CIRCUITS

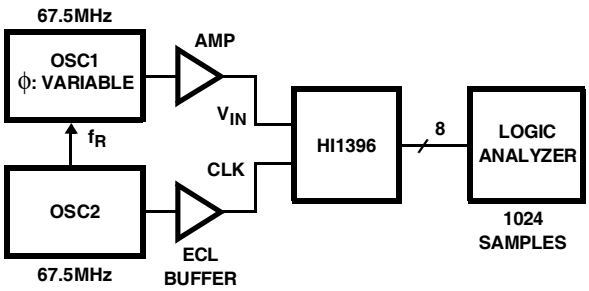
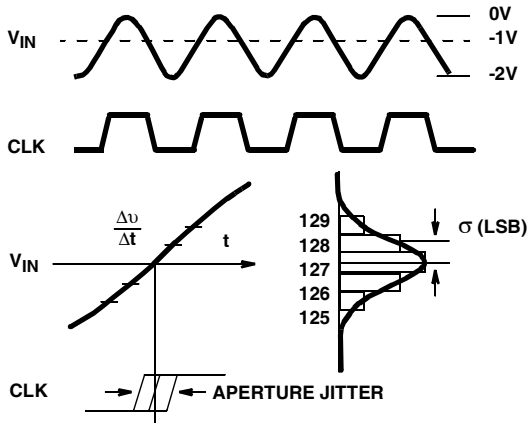


FIGURE 6A.



Aperture jitter is defined as follows:

$$t_{AJ} = \sigma / \frac{\Delta\upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right)$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 6B. APERTURE JITTER TEST METHOD

FIGURE 6. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT