HARRIS Semiconductor

NOT RECOMMENDED FOR NEW DESIGNS
See HI3086

HI1826

October 1998

6-Bit, 140 MSPS, Flash A/D Converter

Features

- **Ultra-High Speed Operation with Maximum Conversion Rate. . . . . 140 MSPS**
- **Low Input Capacitance 7pF**
- **Wide Analog Input Bandwidth (Min) 200MHz**
- **Low Power Consumption 225mW**
- **Low Error Rate**

Applications

- **RGB Graphics Processing**
- **Digital Data Storage Read Channels**
- **Digital Communications**

Description

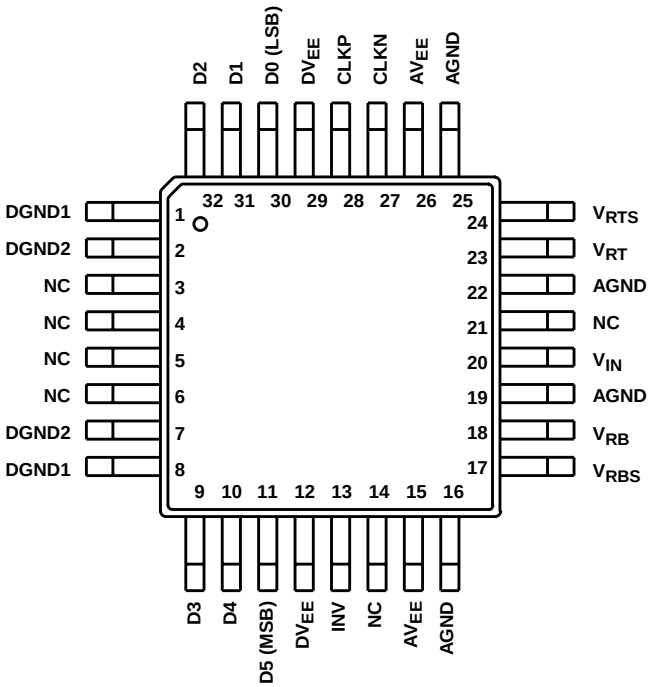
HI1826 is a 6-bit, 140 MSPS, flash A/D converter IC capable of digitizing analog signals at the maximum rate of 140 MSPS. The digital input/output level is compatible with the ECL 100K/10KH/10K.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HI1826JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S

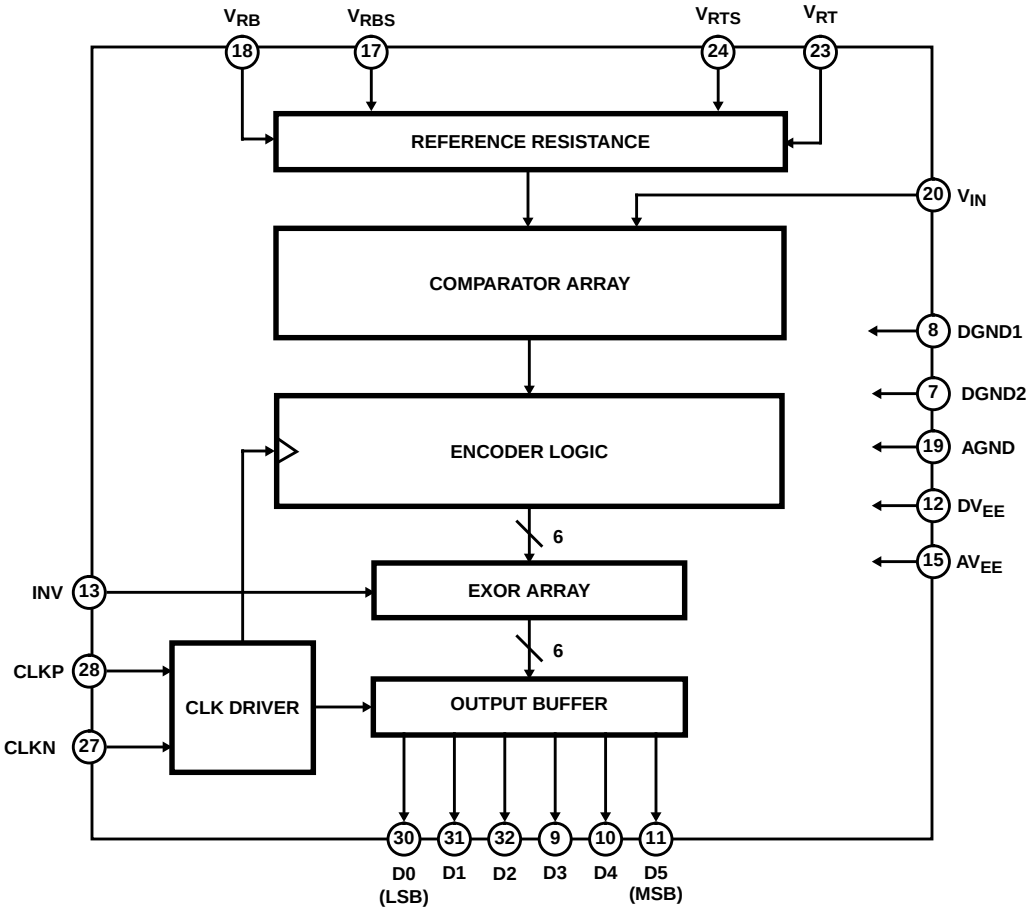
Pinout

HI1826
(MQFP)
TOP VIEW

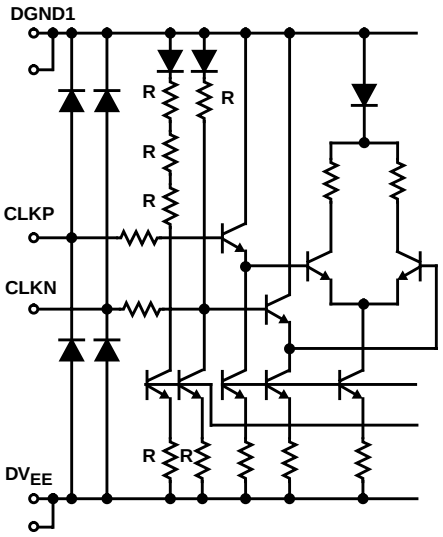
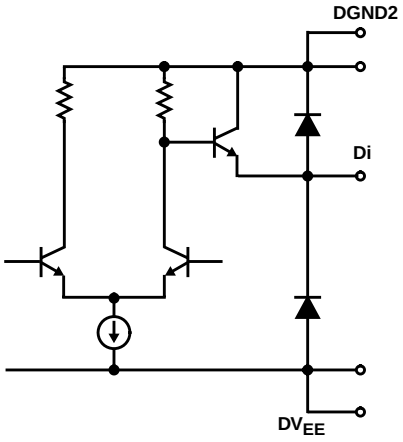


File Number **4107.2**

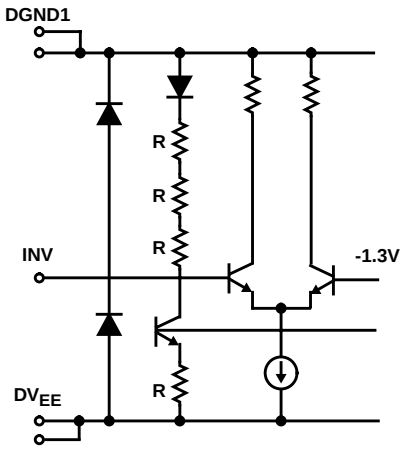
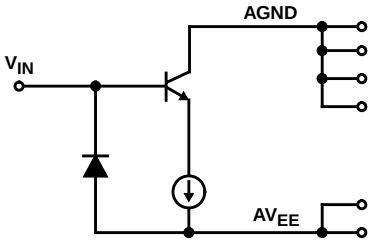
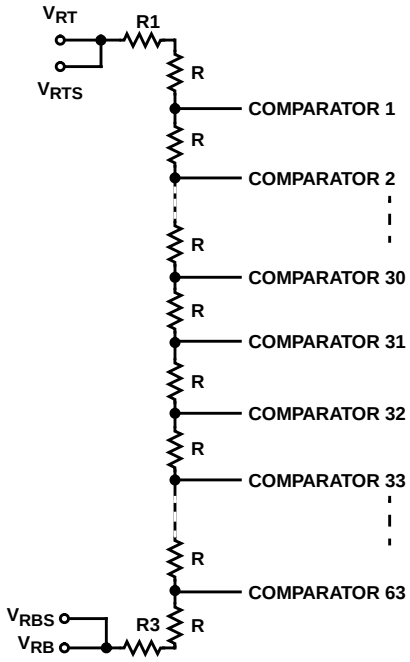
Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
16, 19, 22, 25	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Separated from DGND1 and DGND2.
15, 26	AV_{EE}	-	-5.2V		Analog V_{EE}. Typical voltage is -5.2V. Connected internally with DV_{EE}. (Resistance is 4 to 6Ω.) Connect to AGND through a ceramic chip capacitor of 0.1μF or more just near the pin.
28	CLKP	I	ECL		CLK Input.
27	CLKN				CLK Complementary Input. When left open, voltage goes to ECL threshold potential (-1.3V). Although only CLKP input can be used for operation with CLKN input open, complementary input is recommended in order to attain high speed and stable operation.
1, 8	DGND1	-	0V		Digital GND for Internal Circuits.
2, 7	DGND2	-	0V		Digital GND for Output Transistors.
12, 29	DV_{EE}	-	-5.2V		Digital V_{EE}. Connected internally with AV_{EE}. (Resistance is 4 to 6Ω.) Connect to DGND through a ceramic chip capacitor of 0.1μF or more just near the pin.
30	D0	O	ECL		LSB of Data Output. External pull-down resistor is required.
31	D1				Data Output. External pull-down resistors are required.
32	D2				
9	D3				
10	D4				
11	D5				MSB of Data Output. External pull-down resistor is required.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
13	INV	I	ECL		Output polarity inversion input for D0 (LSB) to D5 (MSB). (Refer to the output code table.) When left open, Low levels maintained.
20	V_{IN}	I	V_{RT} to V_{RB}		Analog Input.
18	V_{RB}	I	-2V		Reference Voltage (Bottom) Force; typical voltage is -2V. Connect to AGND through a ceramic chip capacitor of 0.1µF or more and a tantalum capacitor of 10µF or more just near the pin.
17	V_{RBS}				Reference Voltage (Bottom) Sense.
23	V_{RT}	I	0V		Reference Voltage (Top) Force; typical voltage is 0V. When applying a voltage other than AGND to this pin, connect to AGND through a ceramic chip capacitor of 0.1µF for more and a tantalum capacitor of 10µF or more just near the pin.
24	V_{RTS}				Reference Voltage (Top) Sense.
3, 4 5, 6 14, 21	NC	-	-		Not Connected. Although not connected in the IC, it is recommended that these pins should be connected to AGND or DGND on printed circuit board.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}) . . . . . -7V to 0.5V
Reference Voltage (V_{RT}, V_{RB}) . . . . . -1.5V to 0.5V
| V_{RT} - V_{RB} | 2.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to 0.5V
Digital Input Voltage (CLKP, CLKN, INV) . . . . . -4V to 0.5V
| CLKP - CLKN | 2.7V
Digital Output Current (I_{D0} to I_{D5}) . . . . . -30mA to 0mA

Operating Conditions

Temperature Range (T_A) . . . . . -20^oC to 75^oC
Supply Voltage
AV_{EE}, DV_{EE} . . . . . -5.5V to -4.95V
AV_{EE}, DV_{EE} . . . . . -0.05V to 0.05V
AGND, DGND . . . . . -0.05V to 0.05V
Reference Voltage
V_{RT} . . . . . -0.1V to 0.1V
V_{RB} . . . . . -2.2V to -1.8V
Analog Input Voltage (V_{IN}) . . . . . V_{RB} to V_{RT}
Clock Pulse Width
t_{PW1} 3.0ns
t_{PW0} 3.0ns

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{DD} = +5V$, $V_{RB} = 1.0V$, $V_{RT} = 2.0V$, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	n		6	6	6	bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	f_C = 140MHz	-0.25	-	+0.25	LSB
Differential Linearity Error	E_{DL}	f_C = 140MHz	-0.25	-	+0.25	LSB
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	$V_{IN} = -1V + 0.07V_{RMS}$	-	7	18	pF
Analog Input Resistance	R_{IN}		300	-	-	kΩ
Input Bias Current	I_{IN}	V_{IN} = -1V	-	-	400	µA
REFERENCE INPUT						
Reference Resistance	R_{REF}		-	200	-	Ω
Offset Voltage V_{RT}	E_{OT}		-	-	20	mV
V_{RB}	E_{OB}		-	-	20	mV
DIGITAL INPUT						
Logic High Level	V_{IH}		-1.13	-	-0.65	V
Logic Low Level	V_{IL}		-2.1	-	-1.5	V
Logic High Current	I_{IH}	Apply -0.8V to Input	0	-	50	µA
Logic Low Current	I_{IL}	Apply -1.6V to Input	-50	-	50	µA
Input Capacitance			-	7		pF
SWITCHING CHARACTERISTICS						
Maximum Conversion Frequency	f_C	Error rate 1E-9 TPS (Note 1)	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	10	-	ps

Electrical Specifications V_{DD} = +5V, V_{RB} = 1.0V, V_{RT} = 2.0V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sampling Delay	t_{DS}		-	1.5	-	ns
High Pulse Width of Clock	t_{PW1}		3.0	-	-	ns
Low Pulse Width of Clock	t_{PW0}		3.0	-	-	ns
DIGITAL OUTPUT						
Logic High Level	V_{OH}	R_L = 100Ω to -2V	-1.10	-	-0.65	V
Logic Low Level	V_{OL}	R_L = 100Ω to -2V	-2.1	-	-1.6	V
Output Delay	t_{DO}	R_L = 100Ω to -2V	3.0	3.6	4.2	ns
Output Rise Time	t_r	R_L = 100Ω to -2V, 20% to 80%	-	0.8	-	ns
Output Fall Time	t_f	R_L = 100Ω to -2V, 20% to 80%	-	1.0	-	ns
DYNAMIC CHARACTERISTICS						
Analog Input Bandwidth		f_{CLK} = 140MHz, f_{IN} = 69.999MHz	200	-	-	MHz
Error Rate		Error Amplitude ≥ 4 LSB -3dB f_S	-	-	1E-09	TPS (Note 1)
S/N Ratio	SNR	f_{CLK} = 140MHz, f_{IN} = 1MHz	-	36	-	dB
		f_{CLK} = 140MHz, f_{IN} = 35MHz		34		dB
POWER SUPPLY						
Supply Current	I_{EE}	AV_{EE} = DV_{EE} = -5.2V	-60	-40	-25	mA
Power Consumption	P_D		-	225	-	mW

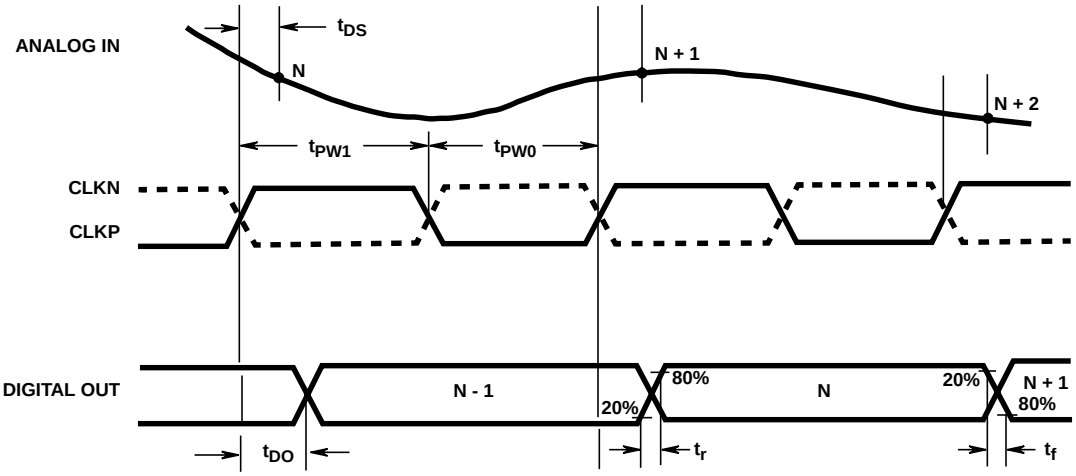
Note 1. TPS: Times Per Sample

Output Code Table

V_{IN} (NOTE)	STEP	INV: 1		INV:0	
		D5	D0	D5	D0
0V	0	000000		111111	
	1	000001		111110	
		•		•	
		•		•	
		•		•	
-1.0V	31	011111		100000	
	32	100000		011111	
		•		•	
		•		•	
		•		•	
	62	111110		000001	
-2.0V	63	111111		000000	

NOTE: V_{RT} = 0V, V_{RB} = -2V

Timing Diagram



Test Circuits

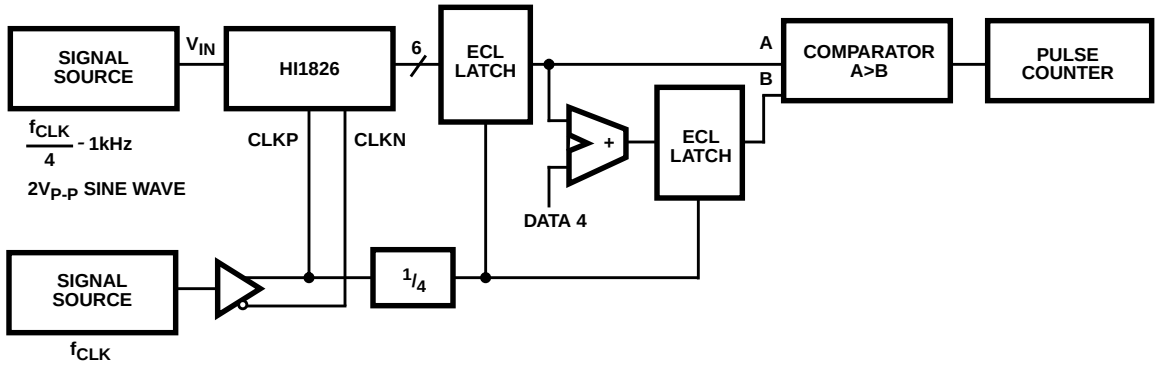


FIGURE 1. MAXIMUM CONVERSION RATE MEASUREMENT CIRCUIT

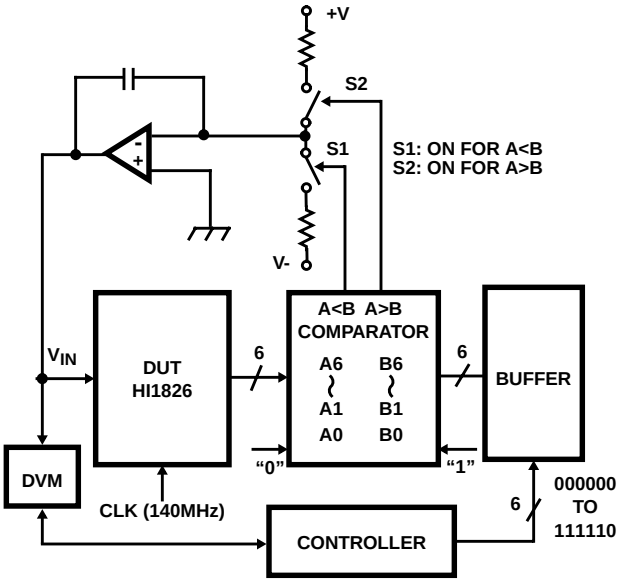


FIGURE 2. INTEGRAL LINEARITY ERROR MEASUREMENT CIRCUIT, DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT

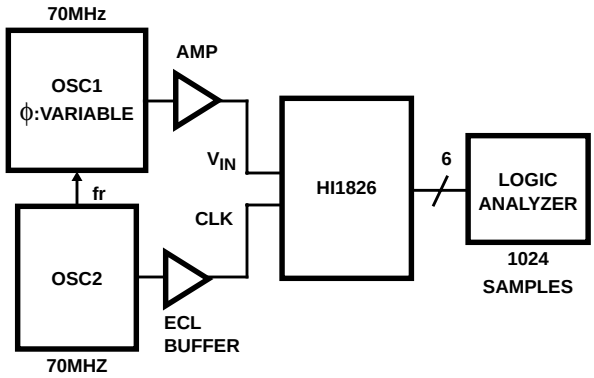


FIGURE 3. SAMPLING DELAY MEASUREMENT CIRCUIT APERTURE JITTER MEASUREMENT CIRCUIT

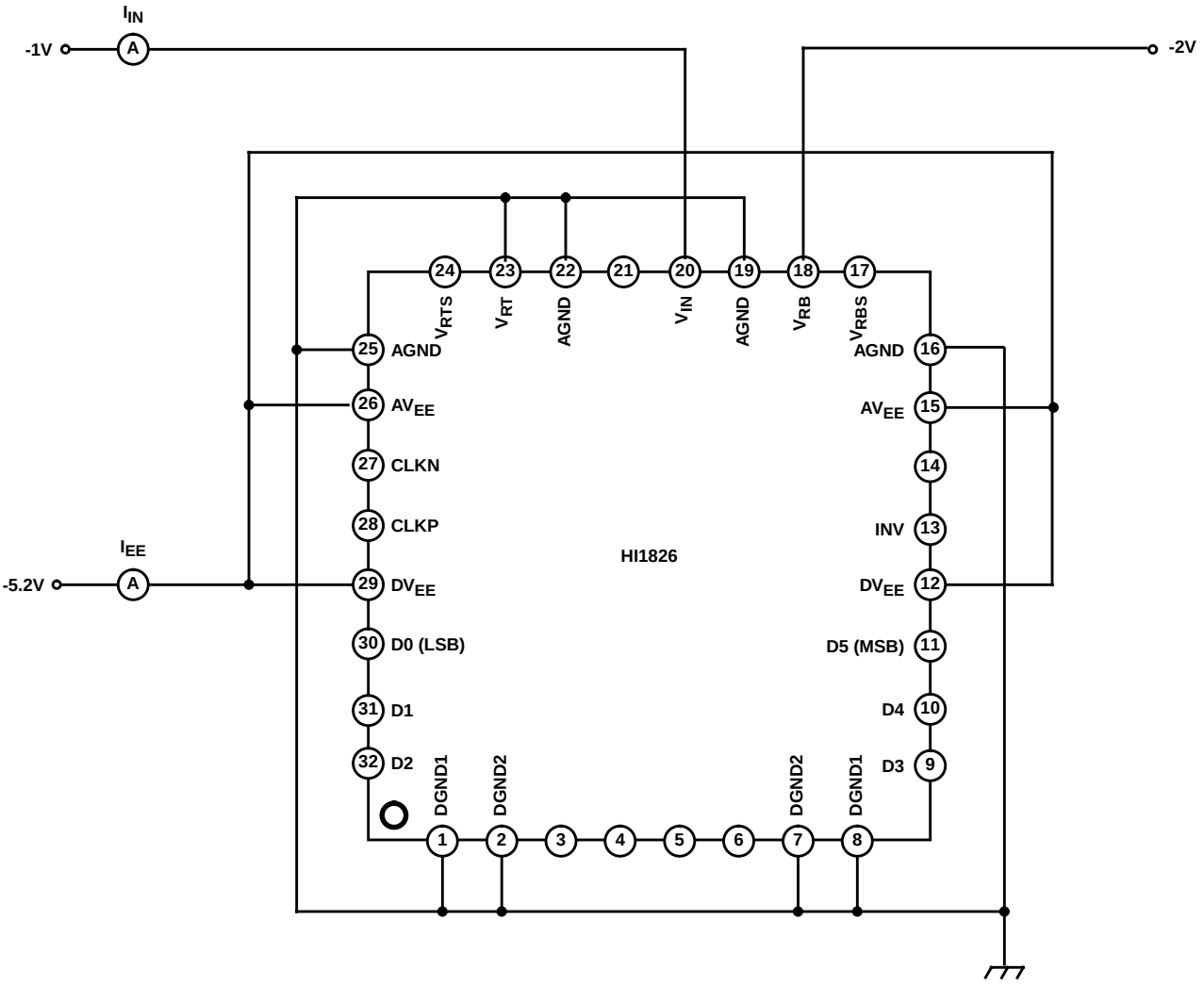


FIGURE 4. SUPPLY CURRENT MEASUREMENT CIRCUIT ANALOG INPUT BIAS CURRENT MEASUREMENT CIRCUIT