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HI2309

Triple 10-Bit, 50 MSPS, 3-Channel D/A Converter

January 1998

Features

• ResolutionTriple	10-Bit
Maximum Conversion Speed 5	0MHz
RGB 3-Channel Input/Output	
• Differential Linearity Error ± 0 .	5 LSB
• Low Power Consumption	00mW
• Power Supply	Single

Low Glitch

• Direct Replacement for Sony CXD2309

Applications

- Digital TV
- · Graphics Display
- **High Resolution Color Graphics**
- **Video Reconstruction**
- Instrumentation
- Image Processing
- I/Q Modulation

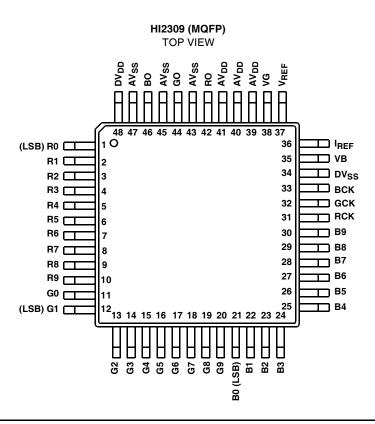
Description

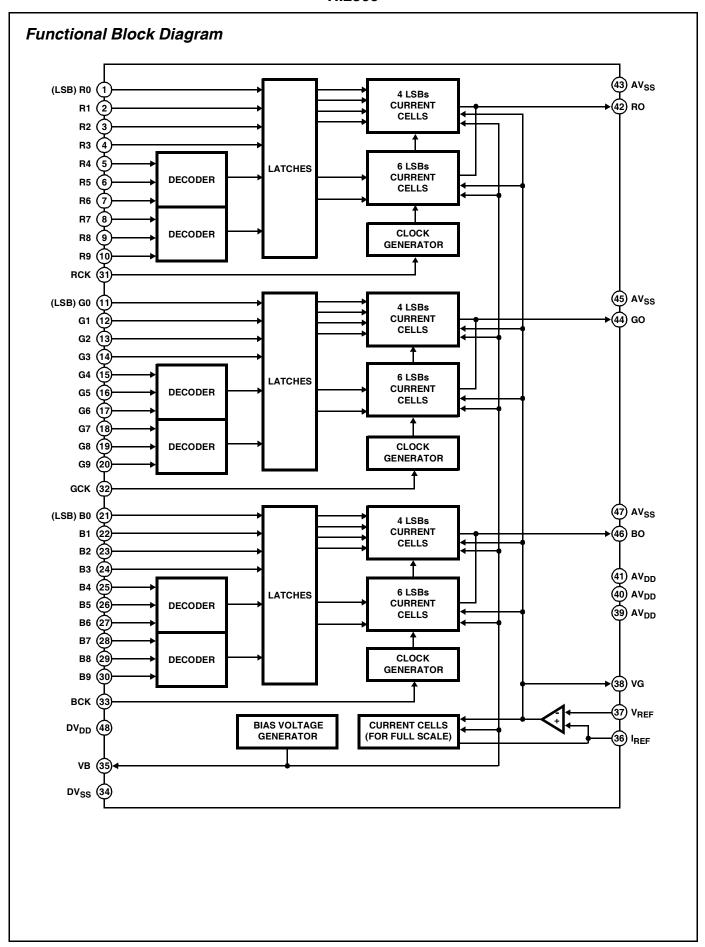
The HI2309 is a triple 10-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 10-bit, pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. Each channel clock input can be controlled individually, or connected together as one. The HI2309 also has BLANK video control signal.

Ordering Information

PART NUMBER	TEMP. RANGE (^O C)	PACKAGE	PKG. NO.
HI2309JCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S

Pinout





Pin Descriptions PIN NO. SYMBOL DESCRIPTION **EQUIVALENT CIRCUIT** 1 to 10 R0 to R9 Digital Input. DV_{DD} G0 to G9 11 to 20 B0 to B9 21 to 30 1 TO 30 DVSS RCLK 31 Clock pin. DV_{DD} GCLK 32 BCLK 33 (31) TO (33) DVSS Digital GND. 34 DVSS 35 VΒ ο DV_{DD} Connect an approximately $0.1 \mu F$ capacitor. 36 IREF Connect a "16R" resistor which is 16 times the AV_{DD} የ o AV_{DD} output resistance "R". 37 Sets an output full scale value. V_{REF} 38 VG Connect an approximately $0.1 \mu F$ capacitor. AVDD AVSS 39 to 41 AV_{DD} Analog V_{DD}. 42 RO Current Output. Output can be obtained by AV_{DD} connecting a resistor (200 Ω typical). 44 GO 46 во $_{\mathsf{AV}_{\mathsf{SS}}}$ AV_{DD} 43, 45, 47 Analog GND. 47, 48 DV_{DD} Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^{\circ}C$

Operating Conditions

Supply voltage	
AV _{DD} , AV _{SS} 4.75V to 5.29	5V
DV _{DD} , DV _{SS}	5V
Reference Input Voltage (V _{REF})	0V
Clock Pulse Width	
t _{PW1} · · · · · · · 10ns (M	in)
t _{PW0} · · · · · · 10ns (M	in)
Temperature Range (T _{OPR})20°C to 75°	οС

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{o}C/W$)
MQFP Package	94
Maximum Junction Temperature (Plastic Package)	150 ⁰ C
Maximum Storage Temperature Range6	5°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $f_{CLK} = 50 MHz$, $V_{DD} = 5 V$, $R = 200 \Omega$, $V_{REF} = 2.0 V$, $T_A = 25 °C$

PARA	METER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	10	-	Bit
Maximum Conversion	Speed	f _{MAX}		50	-	-	MHz
Linearity Error		EL		-2.0	-	2.0	LSB
Differential Linearity E	rror	E _D		-0.5	-	0.5	LSB
Output Full Scale Voltage		V _{FS}		1.8	1.92	2.0	V
Output Full Scale Current		I _{FS}		9.0	9.6	10	mA
Output Offset Voltage		Vos		-	-	1	mV
Supply Current		I _{DD}		-	40	50	mA
Digital Input Current	High Level	I _{IН}		-	-	5	μΑ
	Low Level	I _{IL}		-5	-	-	μΑ
Digital Input Voltage	High Level	V _{IH}	DV _{DD} = 4.75 to 5.25V	2.15	-	-	V
	Low Level	V _{IL}	DV _{DD} - 4.75 to 5.25V	-	-	0.85	V
Precision Guaranteed Output Voltage Range		V _{OC}		1.8	1.92	2.0	V
Setup Time		t _S		6	-	-	ns
Hold Time		t _H		3	-	-	ns
Propagation Delay Time		t _{PD}		-	14	-	ns
Glitch Energy		GE	For $R_{OUT} = 100\Omega$, $1V_{P-P}$ Output	-	50	-	pV/s
Cross Talk		СТ	For 10MHz Sine Wave Output	40	42	-	dB
SNR		SNR	For 1MHz Sine Wave Output	50	55	-	dB

NOTE:

2. Output full scale ratio = Full scale voltage for each channel Average of full scale voltage for each channel - 1 x 100%.

Test Circuits 10 RO TO R9 1 TO 10 RO (42 10-BIT **≨** 200 COUNTER 10 G0 TO G9 WITH AV_{SS}(43) 11 TO 20 LATCH ₩ 10 B0 TO B9 GO (44) OSCILLOSCOPE **≨** 200 (35) VB AV_{SS}(45) **0.1**μ ablaav $_{\mathsf{ss}}$ 7 BO (46 $\mathsf{DV}_{\mathsf{SS}}$ **≥** 200 CLK 50MHz SQUARE 31) RCK AV_{SS}(47) AV_{SS}

(32) GCK

(33) BCK

WAVE

FIGURE 1. MAXIMUM CONVERSION RATE TEST CIRCUIT

HI2309

VG(38

IREF

V_{REF} (37) 2V

 AV_{DD}

0.1μ

≹3.3K VAV_{SS}

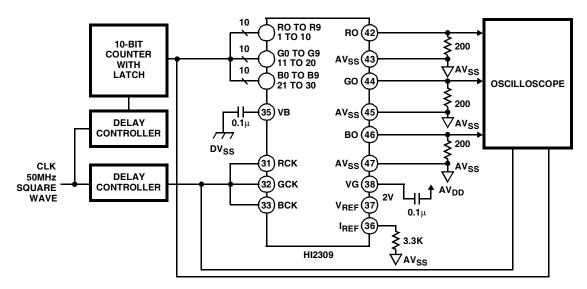


FIGURE 2. SETUP HOLD TIME GLITCH ENERGY TEST CIRCUIT

Test Circuits (Continued) DV_{DD} 10 RO TO R9 1 TO 10 RO (42 **₹**200 DIGITAL 10 G0 TO G9 WAVEFORM GENERATOR AV_{SS} (43) 11 TO 20 Vav_{ss} 10 B0 TO B9 GO (44 **SPECTRUM** 21 TO 30 **ANALYZER ₹**200 (35) VB AVSS (45 —||-0.1μ **∀**av_{ss} во (46 DV_{SS} 200 [↑]AV_{SS} CLK 31) RCK AVSS 50MHz VG (38 SQUARE (32) GCK AV_{DD} WAVE \mathbf{v}_{REF} (33) BCK **0.1**μ I_{REF} **⋛** 3.3K → AV_{SS} HI2309 FIGURE 3. CROSS TALK TEST CIRCUIT 10 RO TO R9 1 TO 10 RO (42 10-BIT **≨** 200 10 G0 TO G9 COUNTER AV_{SS} (43) WITH 11 TO 20 10 **▽**AV_{SS} B0 TO B9 21 TO 30 LATCH GO (44) OSCILLOSCOPE 200 --||-0.1μ 35) VB AV_{SS} (45) ablaav $_{\mathsf{SS}}$ BO (46 $\mathrm{DV}_{\mathrm{SS}}$ 200 CLK 50MHz 31) RCK AVSS (47 AV_{SS} SQUARE

32) GCK

33) BCK

WAVE

FIGURE 4. DC CHARACTERISTICS TEST CIRCUIT

HI2309

VG (38

V_{REF} (37)

IREF

 AV_{DD}

 $\mathbf{0.1}\mu$

≨ з.зк

Test Circuits (Continued)

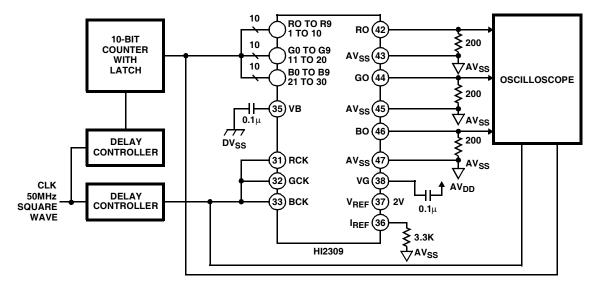


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT

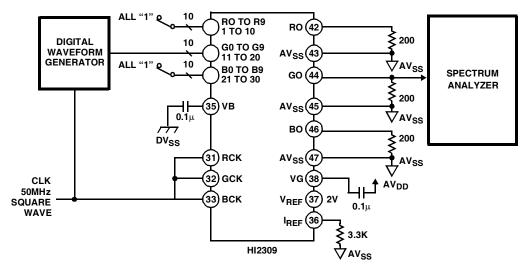
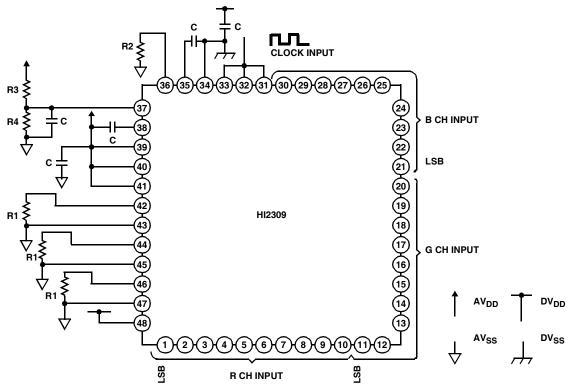


FIGURE 6. SNR TEST CIRCUIT

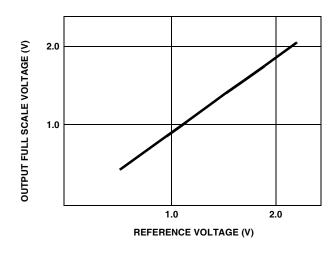
Application Circuit



- When the power supply (AV $_{DD}$ and DV $_{DD}$ is 5.0.
- R1 200Ω.
- R2 = $3.3k\Omega$.
- R3 = $3.0k\Omega$.
- R4 = $2.0k\Omega$.
- $C = 0.1 \mu F$.

Application circuits shown are typical examples illustrating the operation of the devices. Intersil cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Typical Performance Curves



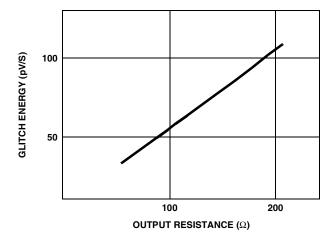
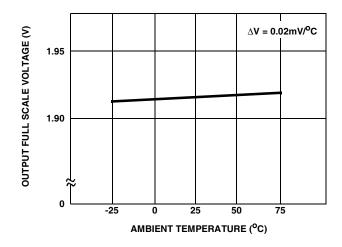


FIGURE 7. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

FIGURE 8. OUTPUT RESISTANCE vs GLITCH ENERGY

Typical Performance Curves (Continued)



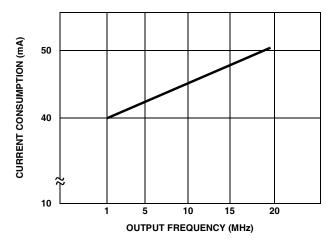


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

FIGURE 10. OUTPUT FREQUENCY vs CURRENT CONSUMPTION

Standard Measurement Conditions and Description

 $V_{DD} = 5.0V.$

 $V_{REF} = 2.0V.$

 $R = 200\Omega$.

 $16R = 3.3k\Omega$.

 $T_{\Delta} = 25^{\circ}C.$

V_{REF} in Figure 9 is fixed to 2V_{DC} without resistor dividing.

Input data in Figure 10 = all "0" and "1" of rectangular wave, clock frequency = 50MHz for a total value of three channels.

Notes On Operation

Selecting the Output Resistance:

HI2309 is a current output type D/A converter. To create the output voltage, connect the resistor to the current output pin.

Specifications:

Output full scale voltage V_{FS} Max = 2.0 [V].

Output full scale current IFS Max = 10 [mA].

Calculate the output resistance from $V_{FS} = I_{FS} \times R$. Connect a resistance sixteen times the output resistance to the reference current pin I_{REF} . In some cases, this value may not exist, a similar value can be used instead.

Note that the V_{FS} will be the following:

 $V_{FS} = V_{REF} \times 16 R/R'$.

R is the resistor to be connected to the IO and R' is the resistor to be connected to the I_{REF} . Power consumption can be reduced by increasing the resistance, but this will on the contrary, increase the glitch energy and data setting

time. Set the best values according to the purpose of use.

Correlation Between Data and Clock:

For HI2309 to display the desired performance as a D/A converter, the data transmitted from outside and the clock must be synchronized properly. Adjust the setup time (t_S) and hold time (t_H) as specified in "Electrical Characteristics."

 V_{DD}, V_{SS} :

Separate the analog and digital signals around the device to reduce noise effects. Bypass the V_{DD} pin to each GND with a $0.1\mu F$ ceramic capacitor as near as possible to the pin for both digital and analog signals.

Latch Up:

The AV_{DD} and DV_{DD} pins must be able to share the same power supply of the board. This is to prevent latch up caused by potential difference between the two pins when the power is turned on.

IREF Pin:

The I_{REF} pin is very sensitive to improve the AC Characteristics. Pay attention for capacitance component not to attach to this pin because its output may become unstable.

VG Pin:

It is recommended to use a $1\mu F$ capacitor to improve the AC Characteristics, though the typical capacitance value externally connected to the V_G Pin is $0.1\mu F.$