HM 65687A

64 K × 1 Ultimate CMOS SRAM

Introduction

The HM 65687A is a very low power CMOS static RAM organized as 65536 × 1 bit. It is manufactured using the MHS high performance CMOS technology named super CMOS.

With this process, MHS is the first to bring the solution for applications where fast computing and low consumption are mandatory, such as aerospace electronics, portable instruments or PC's.

Using an array of six transistors (6T) memory cells, the HM 65687A combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

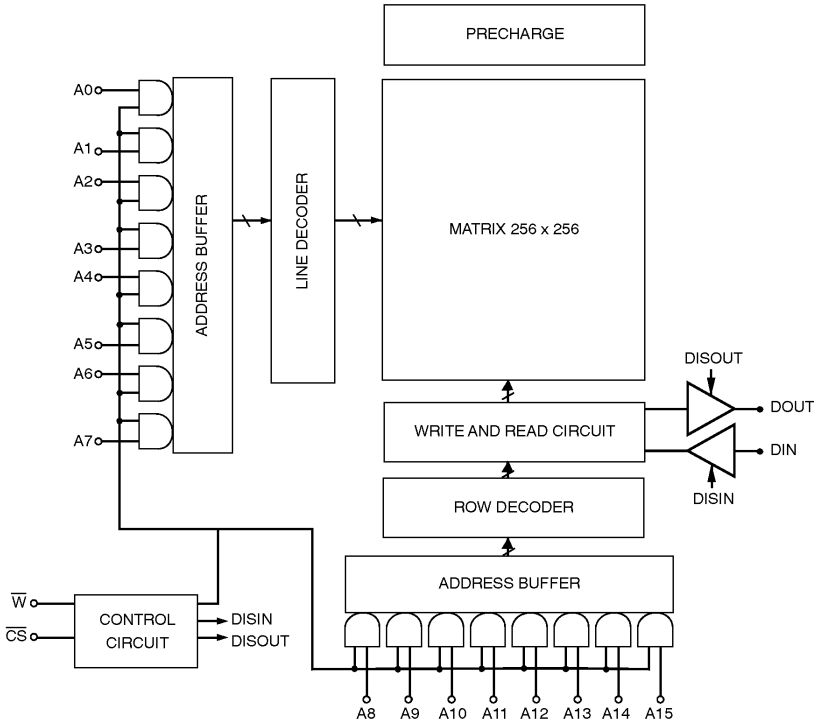
For military/space applications that demand superior levels of performance and reliability the HM 65687A is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

Features

- Access time
  commercial : 35/45 ns (max)
  military/industrial : 45/55 ns (max)
- Very low power consumption
  active : 175.0 mW (typ)
  standby : 0.5 µW (typ)
  data retention : 0.4 µW (typ)
- Wide temperature range :
  –55 to + 125°C
- 300 mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Single 5 volt supply
- Equal cycle and access time
- Gated inputs : no pull-up/down resistors are required

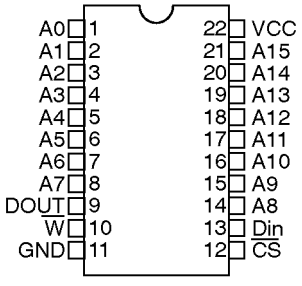
Interface

Block Diagram



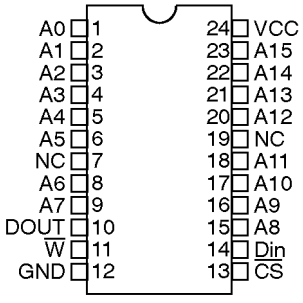
Pin Configuration

Plastic 300 mils, 22 pins, DIL.
Ceramic 300 mils, 22 pins, DIL.



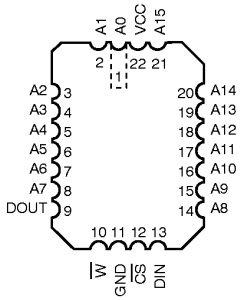
Pinout DIL 22 pins (top view)

SOIC & SOJ 300 mils, 24 pins



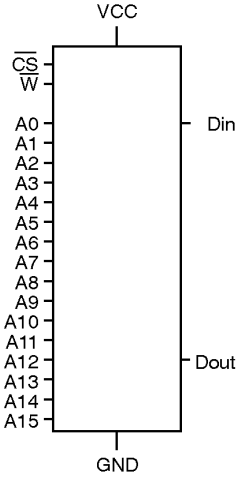
Pinout SO 24 pins (top view)

LCC, 22 pins.



Pinout LCC 22 pins (top view)

Logic Symbol



Pin Names

A0–A15: Address inputs	$\overline{W}$: Write enable
Din : Input	V_{CC} : Power
Dout : Output	GND : Ground
$\overline{CS}$: Chip select	

Truth Table

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = High impedance

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : . . . . . –0.3 V to +7.0 V
Input or Output voltage applied : . . . . (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : . . . . . –65°C to +150°C

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military (– 2)	V_{CC} ± 10 %	– 55°C to + 125°C
Industrial (– 9)	V_{CC} ± 10 %	– 40°C to + 85°C
Commercial (– 5)	V_{CC} ± 10 %	0°C to + 70°C

Recommended DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input Low Voltage	– 0.3	0.0	0.8	V
VIH	Input High Voltage	2.2	–	VCC + 0.3 V	V

Note : 1. VIL min = –0.3 V or –1.0 V pulse width 50 ns.

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	5	pF
Cout (2)	Output capacitance	–	–	7	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

DC Parameters

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (3)	Input leakage current	– 1.0	–	1.0	µA
IOZ (3)	Output leakage current	– 1.0	–	1.0	µA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Note : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled, $\overline{CS} \geq 2.2$ V.
4. Vcc min, IOL = 4.0 mA, IOH = –1.0 mA.

Consumption for Commercial Specification (–5) :

SYMBOL	PARAMETER	65687A B-5	65687A S-5	65687A -5	65687A C-5	UNIT	VALUE
ICCSB (5)	Standby supply current	10	15	10	15	mA	max
ICCSB1 (6)	Standby supply current	1.0	75	1.0	75	µA	max
ICCOP (7)	Operating supply current	65	75	65	75	mA	max

Consumption for Industrial Specification (–9) :

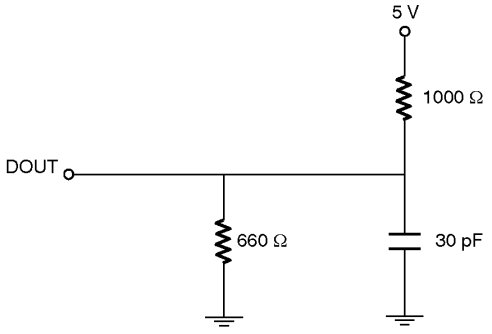
SYMBOL	PARAMETER	65687A B-9	65687A S-9	65687A -9	65687A C-9	UNIT	VALUE
ICCSB (5)	Standby supply current	15	20	15	20	mA	max
ICCSB1 (6)	Standby supply current	5.0	100.0	5.0	100.0	µA	max
ICCOP (7)	Operating supply current	75	100	75	100	mA	max

Consumption for Military Specification (–2) :

SYMBOL	PARAMETER	65687A B-2	65687A S-2	65687A -2	65687A C-2	UNIT	VALUE
ICCSB (5)	Standby supply current	15	20	15	20	mA	max
ICCSB1 (6)	Standby supply current	50.0	500.0	50.0	500.0	µA	max
ICCOP (7)	Operating supply current	75	100	75	100	mA	max

Notes : 5. $\overline{CS} \geq$ VIH.
6. $\overline{CS} \geq$ Vcc – 0.3 V, Iout = 0 mA.
7. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

Output Load

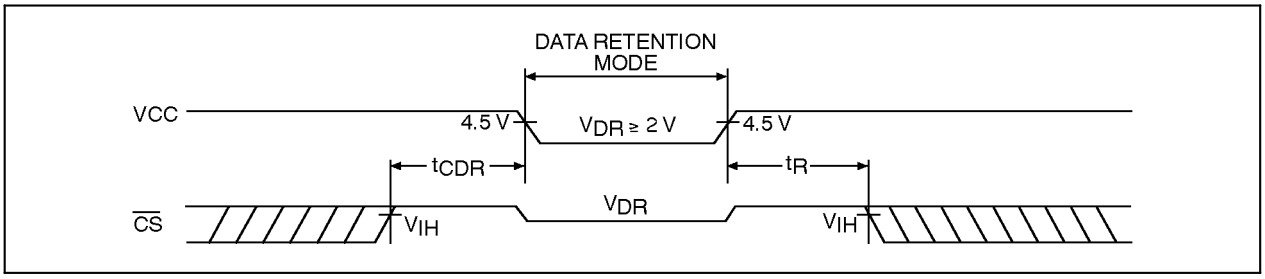


Data Retention Mode

MHS CMOS RAM's are designed with battery backup applications in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc – 0.2 V
2. $\overline{CS}$ must be kept between Vcc – 0.3 V and 70 % of Vcc during the power up and power down transitions
3. The RAM can begin operation > 35 ns after Vcc reaches the minimum operating voltage (4.5 V).

Timing



Data Retention Characteristics

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (8)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselected to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (9)	–	–	ns
ICCDR1(10)	Data retention current				
	@ 2.0 V : HM-65687A B-5	–	0.1	0.5	µA
	HM-65687A B-9	–	0.1	2.0	µA
	HM-65687A B-2	–	0.1	20.0	µA
	HM-65687AS/C-5	–	0.1	30.0	µA
	HM-65687AS/C-9	–	0.1	30.0	µA
	HM-65687AS/C-2	–	0.1	200.0	µA
ICCDR2(10)	Data retention current				
	@ 3.0 V : HM-65687A B-5	–	0.3	1.0	µA
	HM-65687A B-9	–	0.3	3.0	µA
	HM-65687A B-2	–	0.3	30.0	µA
	HM-65687AS/C-5	–	0.3	50.0	µA
	HM-65687AS/C-9	–	0.3	50.0	µA
	HM-65687AS/C-2	–	0.3	300.0	µA

Notes : 8. TA = 25C.
9. TAVAV = Read cycle time.
10. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

AC Parameters

AC Conditions :

Input pulse levels : . . . . . Gnd to 3.0 V
Input rise : . . . . . 5 ns
Input timing reference levels : . . . . . 1.5 V
Output load : . . . . . 1 TTL gate + 30 pF

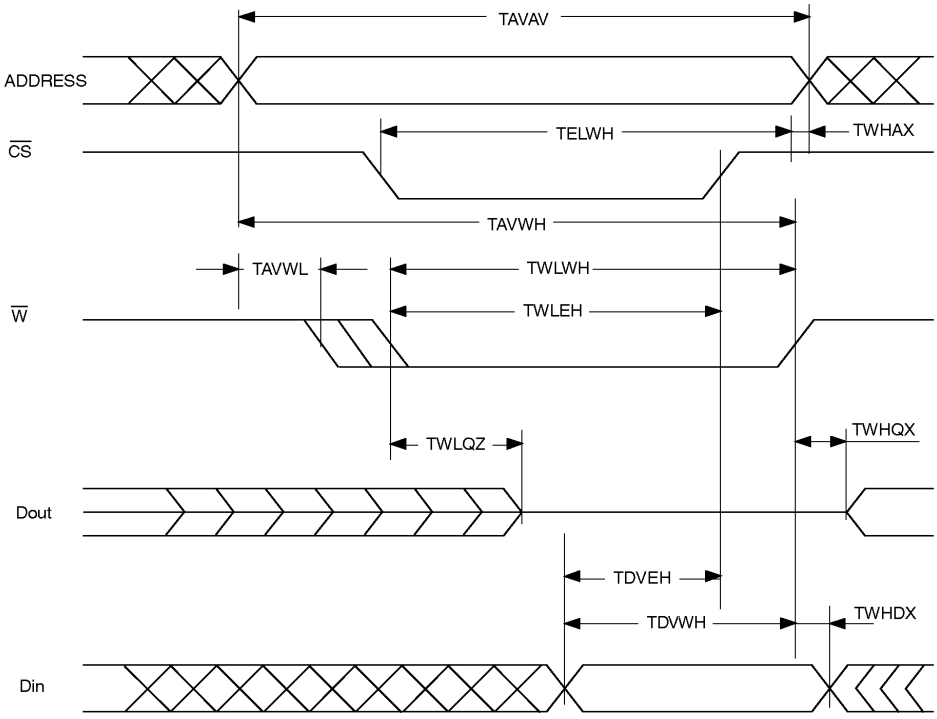
Write Cycle : Commercial Specification

SYMBOL	PARAMETER	65687A B-5	65687A S-5	65687A -5	65687A C-5	UNIT	VALUE
TAVAV	Write cycle time	35	35	45	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end to write	35	35	45	45	ns	min
TDVWH	Data set-up time	22	22	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	35	35	45	45	ns	min
TWLQZ	Write low to high Z	15	15	15	15	ns	max
TWLWH	Write pulse width	30	30	40	40	ns	min
TWHAX	Address hold to end of write	5	5	5	5	ns	min
TWHDX	Data hold time	3	3	3	3	ns	min
TWHQX	Write high to low Z	0	0	0	0	ns	min

Write Cycle : Industrial and Military Specification

SYMBOL	PARAMETER	65687A B-9/2	65687A S-9/2	65687A -9/2	65687A C-9/2	UNIT	VALUE
TAVAV	Write cycle time	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end to write	45	45	55	55	ns	min
TDVWH	Data set-up time	25	25	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	45	45	55	55	ns	min
TWLQZ	Write low to high Z	15	15	20	20	ns	max
TWLWH	Write pulse width	40	40	50	50	ns	min
TWHAX	Address hold to end of write	5	5	5	5	ns	min
TWHDX	Data hold time	3	3	3	3	ns	min
TWHQX	Write high to low Z	0	0	0	0	ns	min

Write Cycle (note 11)



Note : 11. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

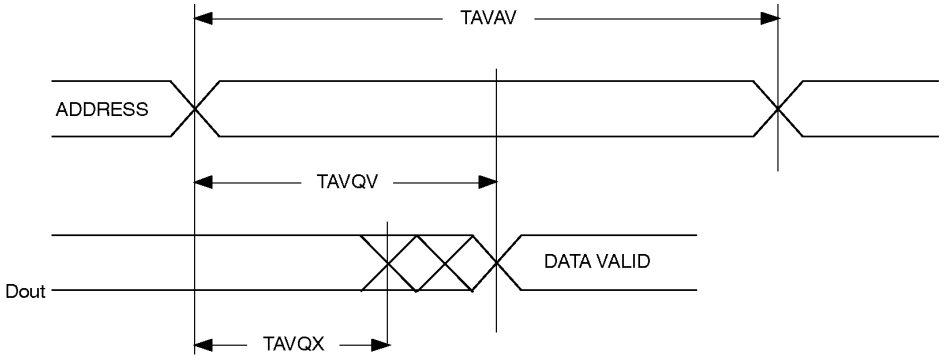
Read Cycle : Commercial Specification

SYMBOL	PARAMETER	65687A B-5	65687A S-5	65687A -5	65687A C-5	UNIT	VALUE
TAVAV	Read cycle time	35	35	45	45	ns	min
TAVQV	Address access time	35	35	45	45	ns	max
TAVQX	Address Valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	35	35	45	45	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	35	45	45	ns	max

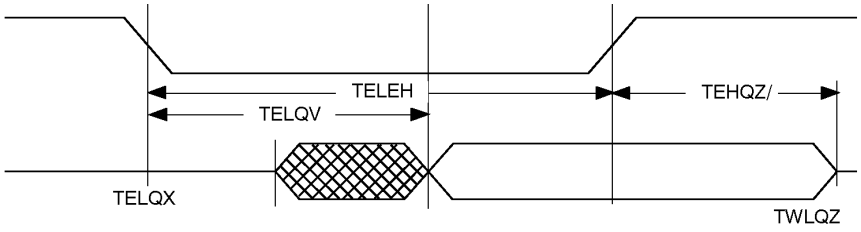
Read Cycle : Industrial and Military Specification

SYMBOL	PARAMETER	65687A B-9/2	65687A S-9/2	65687A -9/2	65687A C-9/2	UNIT	VALUE
TAVAV	Read cycle time	45	45	55	55	ns	min
TAVQV	Address access time	45	45	55	55	ns	max
TAVQX	Address Valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	45	45	55	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	45	45	55	55	ns	max

Read Cycle nb 1 (notes 12, 13)



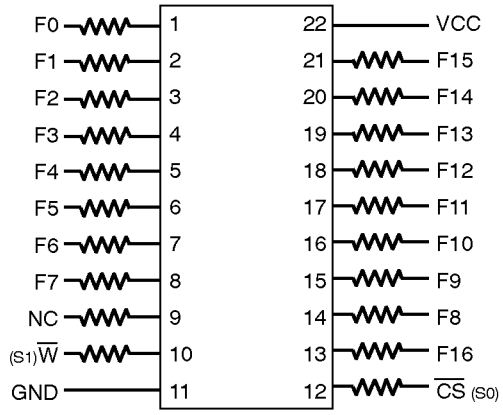
Read Cycle nb 2 (notes 12, 14)

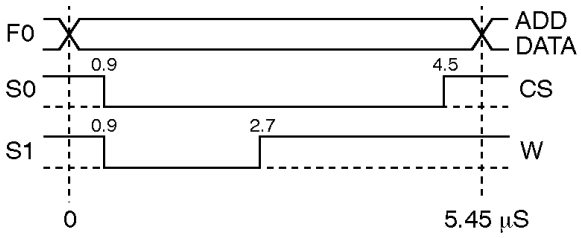


Notes : 12. $\overline{W}$ is high for read cycle.
13. Device is continuously selected, $\overline{CS}$ = VIL.
14. Address valid prior to or coincident with $\overline{CS}$ transition low.

Burn-in Schematics

64 K × 1
(without output enable)





VCC = 5 V (–0, + 0.5)
R = 1 KΩ per pin
F0 = 91.6 KHz ± 20%

Fn = 1/2 F n – 1
S0 & S1 : programmable signals for write/read cycles
NC : Non connected.

Ordering Information

PACKAGE		DEVICE TYPE	GRADE	LEVEL
HM	1	65687A	B	–5

1
- 0 – Chip form
- 1 – Ceramic 22 pins 300 mils
- 3 – Plastic 22 pins 300 mils
- 4 – LCC 32 pins rectangular
- T – SOIC 24 pins 300 mils
- U – SOJ 24 pins 300 mils

65687A
64 K × 1 Ultimate CMOS static RAM

B
- B : high speed/low current
- S : high speed/standard current
- Blank : standard speed/low current

–5
- –2 : Military
- –5 : Commercial
- –6 : 100% 25°C Probe
- –9 : Industrial
- /883 : MIL STD 883 class B or S
- DB : Dice Military program
- :R : Tape & Reel option
- :RD : Tape & Reel/Dry pack option
- :D : Dry pack option