National Semiconductor

PRELIMINARY

HS7067/HS7107 7 Amp, Multimode, High Efficiency Switching Regulator

General Description

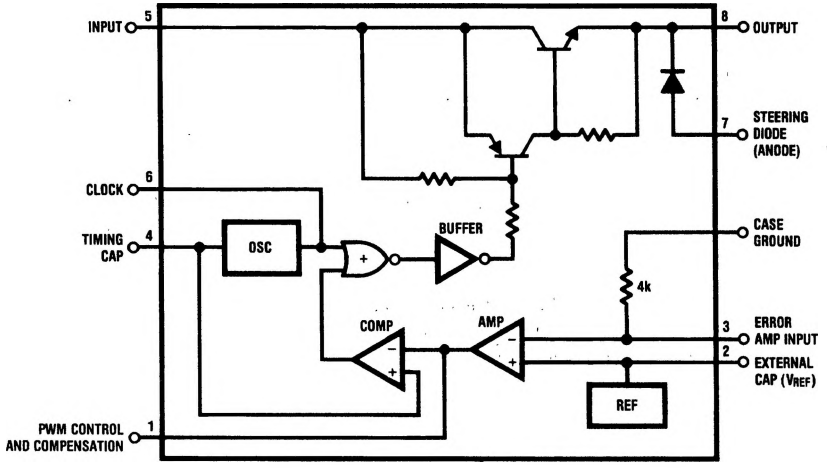
The HS7067/HS7107 is a hybrid high efficiency switching regulator with high output current capability. The device is housed in a standard TO-3 package containing a temperature compensated voltage reference, a pulse-width modulator with programmable oscillator frequency, error amplifier, high current, high voltage output switch and steering diode. The HS7067/HS7107 operates in a step-down, inverting, as well as in a transformer-coupled mode.

The HS7067/HS7107 can supply up to 7A of continuous output current over a wide range of input and output voltages.

Features

- HS7067—10V to 60V input
- HS7107—10V to 100V input
- 7A continuous output current
- Step-down, inverting, and transformer-coupled operation
- Frequency adjustable to 200 kHz
- High-efficiency (>75%)
- Standard 8-pin TO-3 package

Block and Connection Diagrams



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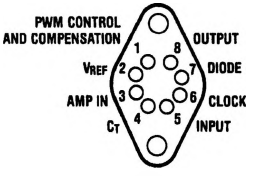
Metal Can Package



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Top View

Case is ground

Order Number HS7067CK, HS7067K, HS7107CK or HS7107K
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{IN}, Input Voltage
- HS7067: 65V
- HS7107: 105V

I_{OUT}, Output Current: 8A

T_J, Operating Temperature: 150°C

P_D, Internal Power Dissipation: 25W

T_A, Operating Temperature Range
- HS7067C/7107C: −25°C to +85°C
- HS7067/7107: −55°C to +125°C

T_{STG}, Storage Temperature Range: −65°C to +150°C

$V_R(V_{8-7})$, Steering Diode Reverse Voltage: 105V

$I_D(I_{7-8})$, Steering Diode Forward Current: 8A

Electrical Characteristics T_C = 25°C, V_{IN} = 20V (unless otherwise specified)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
$V_{IN}-V_{OUT}$	Min V_{IN}/V_{OUT} Differential	HS7067	10V ≤ V_{IN} ≤ $V_{IN(MAX)}$, I_{OUT} = 2A (Note 6)			3.0		V
		HS7107				3.0		V
V_S	Switch Saturation Voltage		I_C = 7.0A, V_{IN} = 10V	HS7107		1.6	TBD	V
				HS7607			1.9	V
			I_C = 2.0A, V_{IN} = 10V			1.0		V
V_F	Steering Diode On Voltage		I_D = 7.0A	HS7107		1.3	TBD	V
				HS7607		1.7	TBD	
			I_D = 2.0A			0.9		V
V_{IN}	Supply Voltage Range (Note 7)	HS7067	$T_{MIN} \le T_A \le T_{MAX}$		10		60	V
		HS7107	$T_{MIN} \le T_A \le T_{MAX}$		10		100	V
I_R	Steering Diode Reverse Current		V_R = 100V				60	μA
I_Q	Quiescent Current (Note 3)		0% Duty Cycle (V_3 = 3.0V)			6		mA
			100% Duty Cycle (V_3 = 0V)			26		mA
V_2	Reference Voltage on Pin 2		$T_{MIN} \le T_A \le T_{MAX}$		2.3	2.5	2.7	V
$V_{CLK\,H}$	Clock Output High		I_{CLK} = −750 μA		1.2	1.6		V
$V_{CLK\,L}$	Clock Output Low		I_{CLK} = 80 μA				0.9	V
ΔV_2	LIne Regulation of Reference Voltage on Pin 2		$V_{MIN} \le V_{IN} \le V_{MAX}$			5		mV
R_A	Resistance on Pin 3 to Ground		(Note 4)			4.0		kΩ
V_{OUT}	Feedback Resistor R_f Tol. ±1%			HS7107		4	TBD	%
				HS7067			9	
V_4	Voltage Swing—Pin 4					3.0		V
I_4	Charging Current—Pin 4					330		μA
I_{CLK}	Clock Input Current — Pin 6		V_{CLK} = 3.5V			1.75	4	mA
t_r	Transistor Current Rise Time		I_O = 2.0A (Note 6)			70		ns
			I_O = 7.0A (Note 6)			120		ns
t_f	Transistor Current Fall Time		I_O = 2.0A (Note 6)			100		ns
			I_O = 7.0A (Note 6)			160		ns
t_s	Diode Storage Time		I_O = 7.0A (Note 6)			120		ns
t_d	Delay Time		I_O = 7.0A (Note 6)			600		ns
f_{MAX}	Max Clock Frequency		(Note 5)				200	kHz

Electrical Characteristics $T_C = 25°C$, $V_{IN} = 20V$ (unless otherwise specified) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$Z_{PIN\ 1}$	Impedance at Pin 1	(Note 6)			5		MΩ
η	Efficiency	V_{OUT} = 5V, I_{OUT} = 1A	f_O = 25 kHz (Note 6)		80		%
			f_O = 200 kHz (Note 5)		70		%
θ_{JC}	Thermal Resistance	(Note 1)			4.0		°C/W

Note 1: θ_{JA} is typically 35°C/W for natural convection cooling.

Note 2: V_{OUT} and I_{OUT} refer to the output DC voltage and output current of a switching supply after the output LC filter as shown in *Figure 1*.

Note 3: Quiescent current depends on the duty cycle of the switching translator.

Note 4: This test includes the input bias current of the error amplifier.

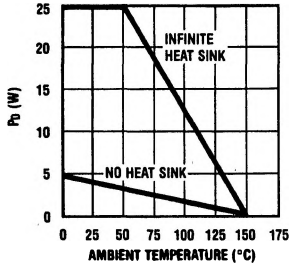
Note 5: Circuit configured as shown in *Figure 1*.

Note 6: These parameters are not tested. They are given for informational purposes only.

Note 7: Functionally tested at limits only (pass-fail).

Typical Performance Characteristics

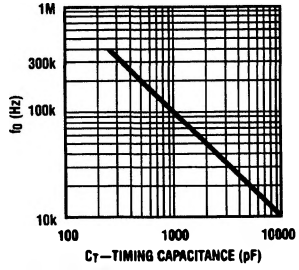
Power Derating Curve



θ_{JC} = 4°C/W

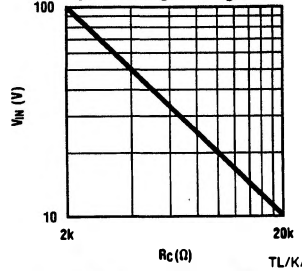
θ_{JA} = 35°C/W

Frequency vs Timing Capacitance



$$f_O = \frac{1}{10k \times C_T}$$

Typical Compensation Input Voltage vs R_C



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$$R_C = \left[\frac{200k}{V_{IN(MAX)}}\right] \Omega$$

$$C_C = \frac{\sqrt{LC} \times \sqrt{10}}{R_C} F$$

Typical Applications

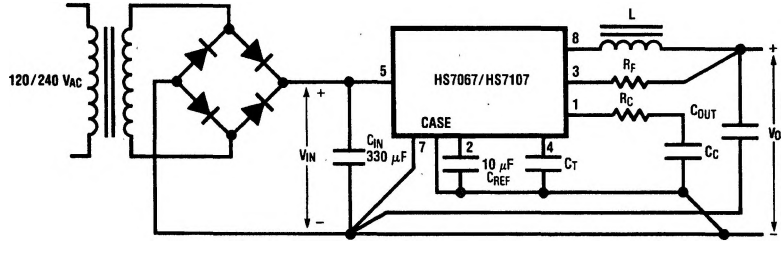
THE BUCK CONVERTER (Step Down)

The buck converter is the most common application in switching-power conversion. It allows to step down a voltage with a minimum of components and a maximum of efficiency (for further information on the theory of operation of a buck converter, see AN-343).

f_O	25 kHz	200 kHz
L	86 μH	21 μH
C_T	0.0039 μF	330 pF
C_C	0.2 μF	0.068 μF
R_f	4 kΩ	4 kΩ
R_C	5.7 kΩ	5.7 kΩ
C_{OUT}	1500 μF	680 μF

V_{IN} = 10V to 35V
V_{OUT} = 5V
I_{OUT} = 1A to 6A

Load Regulation = 40 mV
Line Regulation = 5 mV



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Typical Applications (Continued)

Design equations:

Following are the design equations for a buck converter application using the HS 7107/7067:

$$C_T = \frac{1}{10^4 \times f_O}$$

$$L_{MIN} = \frac{(V_{IN(MAX)} - V_O)\, V_O}{V_{IN(MAX)} \times f_O \times \Delta I} \quad \text{(Note 7, 9)}$$

$$C_{MIN} = \frac{\Delta I}{4\, f_O\, (e_O - \Delta I \times ESR)} \quad \text{(Note 8, 9)}$$

$$C_C = \frac{\sqrt{10\, LC}}{R_C}$$

$$R_C = \frac{2 \times 10^5}{V_{IN(MAX)}}$$

$$R_f = 4k\left(\frac{V_O - 2.5}{2.5}\right)\Omega$$

Note 7: L_{MIN} is the minimum value of output filter inductance, L, for stable operation.

Note 8: C_{MIN} is the minimum value of output filter capacitance, C, necessary to achieve an output ripple voltage, e_O. ESR is the Effective Series Resistance of the output filter capacitor, C, at the operating frequency, f_O.

Note 9: ΔI = Peak to Peak Ripple current through the inductor and the capacitor. $\frac{\Delta I}{2} < I_{O\,MIN}$ and $\frac{\Delta I}{2} < 7 - I_{O\,MAX}$.

Efficiency Equations

Since high efficiency is the principal advantage of switched-mode power conversion, switching regulator losses are an important design concern. Losses and efficiency of a buck converter can be calculated with the following equations.

Note: Pin 7 is grounded; I_O = average output current at pin 8

Switching Period (T)

$$T = \frac{1}{f_O} = t_{ON} + t_{OFF}$$

Duty Cycle (D)

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_O + V_F}{V_{IN} - V_S + V_F}$$

Transistor DC Losses (P_T)

$$P_T = V_S \times I_O \times D$$

Transistor Switching Losses (P_S)

$$P_S = (V_{IN} + V_F) \times I_O \times \frac{(t_r + t_f + 2t_S)\, f_O}{2}$$

Capacitor Losses (P_C)

$$P_C = ESR \times \left(\frac{V_O\,(T - DT)}{4L}\right)^2$$

Diode DC Losses (P_D)

$$P_D = V_f \times I_O \times (1 - D)$$

Drive Circuit Losses (D_L)

$$D_L = 0.02 \times V_{IN} \times D$$

Inductor Losses (P_L)

$$P_L = I_O{}^2 \times R_L \text{ (DC winding resistance)}$$

Power Output (P_O)

$$P_O = \frac{((V_{IN} - V_S)\, t_{ON}) - ((V_F)\, t_{OFF})}{t_{ON} + t_{OFF}} \times I_O$$

Efficiency (η)

$$\eta = \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_T + P_S + P_D + D_L + P_L + P_C}$$

TRANSFORMER COUPLED CONVERTERS

In addition to the implementation of a buck converter, the HS 7107/7067 can be used in various transformer coupled configurations. They can be used in various topologies such as: step-up, step-down, inverter, multiple outputs and isolated converters.

There are basically two different methods in implementing transformer coupled converters: the flyback and the foward topology

The Flyback Principle

Figure 1 shows a functional diagram of a flyback converter. Depending on the turn ratio N2/N1 and the feedback voltage, it can be implemented as a step-down or step-up converter.

When the switch is on, the current (I_p) flows through the primary winding creating a magnetic flux in the core and storing the energy. At this time, the voltage at the secondary keeps the same polarity (with respect to the dotted terminals), the diode is off and no current flows through it. When the switch is off, the voltage at the secondary and primary becomes reversed and the diode turns-on (I_d). The stored energy is then transferred to the load and the output filter capacitor. The energy stored in the capacitor will supply the load current during the next turn-on.

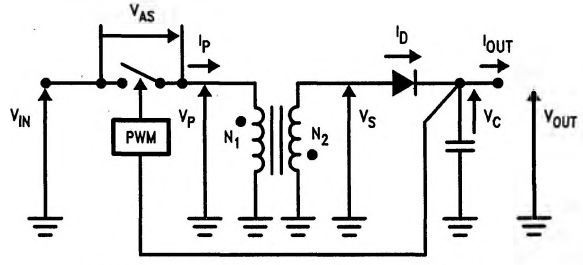

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FIGURE 1. Typical Flyback Functional Diagram

Typical Applications (Continued)

V_p = Voltage at primary
V_{as} = Voltage across the switch
V_s = Voltage at the secondary
I_p = Current at primary
I_d = Current through diode
I_c = Current through output cap
I_{out} = Output current of the converter
ΔI = Ripple current
D = $T_{on}/(T_{off} + T_{on})$
F = Switching frequency
V_{df} = Forward voltage drop of the diode
V_1 = $V_{out} \times N_1/N_2$ $V_2 = V_{in} + V_{out}\, N_1/N_2$
V_3 = Saturation voltage of the switch
V_4 = $V_{out} + V_{df}$ $V_5 = V_{in} \times N_2/N_1$

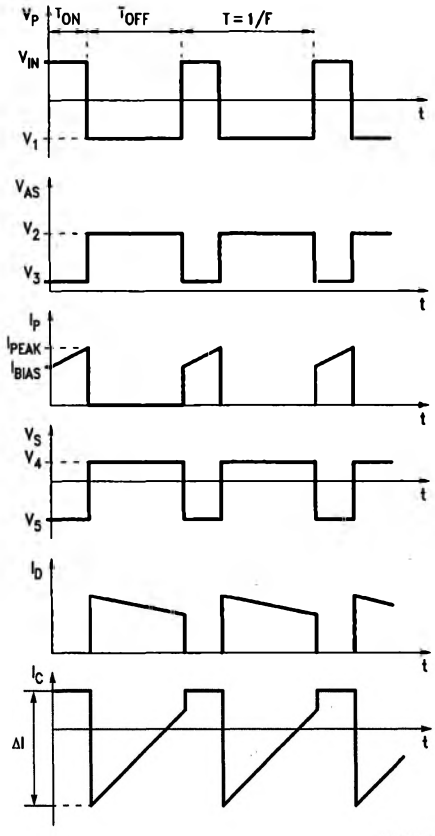

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FIGURE 2. Typical Flyback Waveforms

The load current is not supplied directly by the input source when the switch is on, but only by the energy stored in the output capacitor. The output voltage is monitored by the feedback loop which controls the duty cycle (D) through the PWM (Pulse Width Modulator) which in turn, modulates the amount of energy being transferred from the input to the output. *Figure 2* shows the waveforms of a continuous mode flyback converter (primary current I_p is DC biased).

The Forward Principle

The forward converter is a little more complex and requires more components than the flyback, but the output ripple voltage is smaller. *Figure 3* shows a simplified diagram of a forward converter.

When the switch turns-on, a voltage $V_5 = V_1 \times N_2/N_1$ appears at the secondary of the transformer. The diode D_2

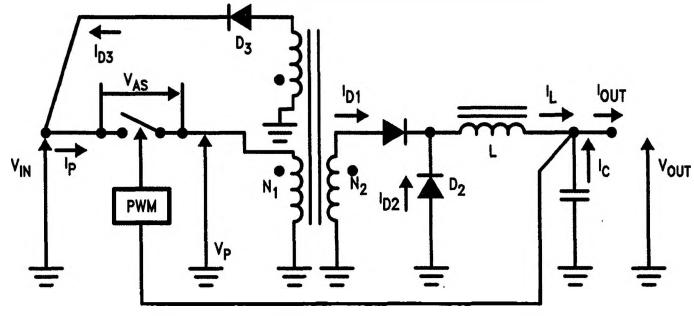

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FIGURE 3. Typical Forward Functional Diagram

Typical Applications (Continued)

is off while D_1 turns-on, allowing the current to flow through the inductor L (I_{d1} and I_L), storing energy in its core, and supplying the load current (I_{out}) and the capacitor current (I_c) at the same time. When the switch turns-off, the magnetic energy stored in the core of the inductor creates a current (I_{d2}) which flows through the diode D_2. The load current I_{out} therefore, equals to $I_{d2} + I_c$.

During the "off" time of the switch, some residual magnetism will stay in the core of the transformer and has to be removed before the next cycle, so that it does not accumulate, leading to core saturation.

A demagnetizing winding is used to "dump" the residual energy back to the input or output of the converter. The functional principle of the demagnetizing winding is similar to the flyback in the sense that, during the turn-off time, the residual magnetism will generate a reverse voltage at the demagnetizing winding (with respect to the dotted terminals) turning on the diode D_3.

In the forward mode, when the switch is off, the load current is supplied by the energy stored in the output capacitor and the choke inductor but when the switch is on, it is supplied by the input source through the transformer. This accounts for the lower output ripple voltage.

The output voltage is monitored by the feedback loop, which controls the duty cycle through the PWM, which in turn modulates the amount of energy being transferred from the input to the output.

V_p = Voltage at primary
V_{as} = Voltage across the switch
V_s = Voltage at secondary
I_p = Current at primary
I_{d1} = Current through diode D_1
I_{d2} = Current through diode D_2
I_{d3} = Current through diode D_3
I_L = Current through inductor L
I_c = Current through output cap
I_{out} = Output current of the converter
Δ_I = Ripple current
F = Switching frequency
D = $T_{on} / (T_{off} + T_{on})$
V_1 = $V_{in} \times N_1/N_3$ $V_3 = V_{in}$
V_2 = $V_{in} + V_1$
V_4 = Saturation voltage of the switch
V_5 = $V_{in} \times N_2/N_1$ $V_6 = V_{in} \times N_2/N_3$

Figure 4 shows the waveforms of the forward converter.

When the switch is off, $V_{as} = V_{in} + (V_{in} \times N_1/N_3)$ during the demagnetization time (T_d) and then, drops to $V_{as} = V_{in}$ as indicated in *Figure 4*.

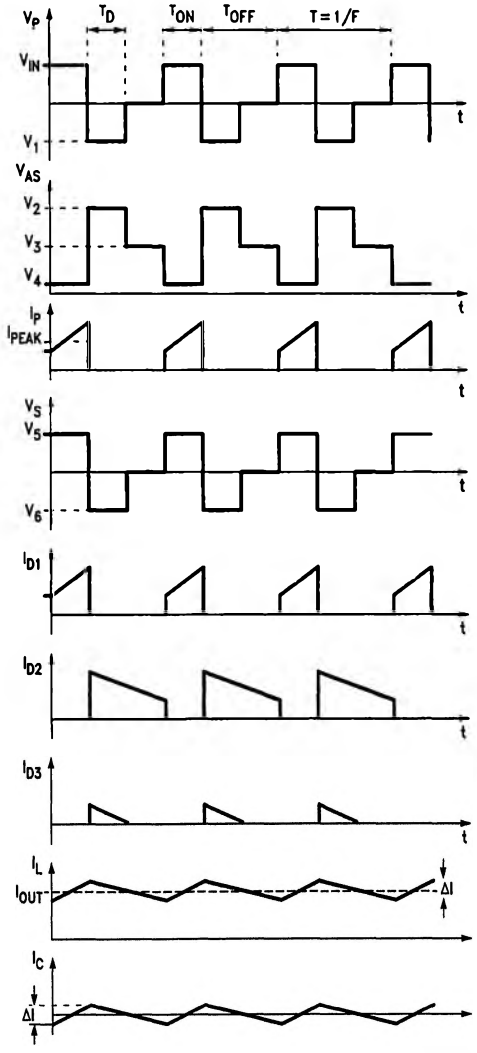

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FIGURE 4. Typical Forward Waveforms

Typical Applications (Continued)

With both flyback and forward topologies, it is possible to design an inverting converter by using an external op-amp (*Figure 5*).

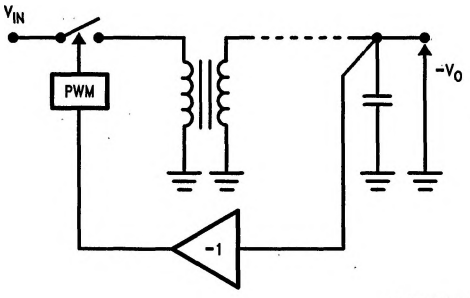

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FIGURE 5

Flyback Step-Up Application

Figure 6 shows flyback converter in a step-up mode where an input voltage of +12V to +30V will be converted into a regulated output voltage of +50V.

Performance Data

Parameter	Conditions	Result
Efficiency	V_{out} = 50V @300 mA V_{in} = 15V	82%
Line Regulation	V_{out} = 50V @300 mA 12V ≤ V_{in} ≤ 30V	0.2%
Load Regulation	V_{in} = 15V V_{out} = 50V 50 mA ≤ I_{out} ≤ 300 mA	0.2%

Isolated Flyback Converter

Figure 7 shows an isolated flyback converter using a sense winding for feedback. Although, in practice the line regulation is acceptable, the load regulation can be marginal if the coupling between the windings is poor. However, the sense winding cannot detect any ohmic voltage drop in the main output so, a heavier gauge wire should be used to reduce this regulation error. Also, the sense winding will not sense the non-linear voltage drop across the diode, and this accounts for most of the load regulation inaccuracy. Therefore, the sense winding method is only recommended for applications where load variations are small.

Figure 7 shows an isolated flyback converter with an output of 5V at 2A. The input voltage range is from +10V to +40V. The output can be adjusted to +5V by using the 5 kΩ trimpot.

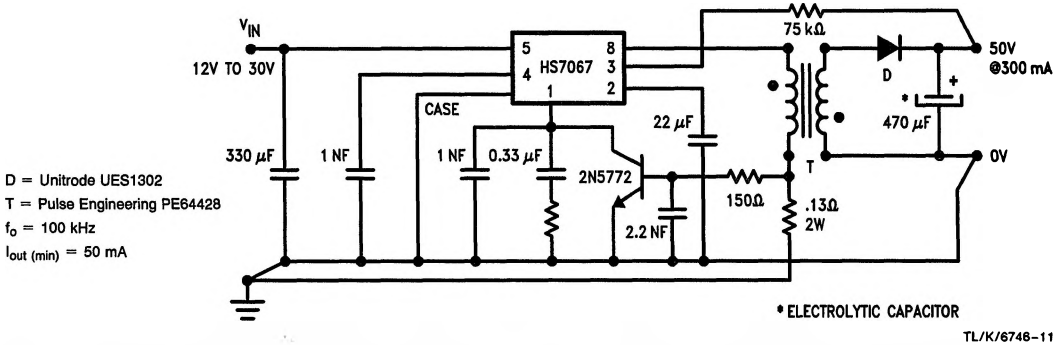
Performance Data

Parameter	Conditions	Result
Efficiency	V_{out} = 5V @ 2A V_{in} = 30V	75%
Line Regulation	V_{out} = 5V @ 2A 10V ≤ V_{in} ≤ 40V	5%
Load Regulation	V_{in} = 30V 1A ≤ I_{out} ≤ 2A	7%

Isolated Forward Converter

As described previously, forward converters exhibit lower output ripple voltage and the opto-coupler feedback scheme provides good regulation as well as input to output isolation.

An opto-coupler feedback is usually difficult to implement because the transfer function of the opto-coupler is non-linear, the current transfer ratio changes with time and temperture and also from one unit to another. *Figure 8* shows the circuit diagram of a 5V @ 3A power converter with an input voltage range of +14V to +30V using an isolated forward topology.



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A 12V to 60V input Voltage Range is possible by replacing the HS7067 with a HS7107. The converter will operate in a discontinuous mode above 30V with a 300 mA load (the transformer's secondary current drops to zero before the switch turns on) and therefore, may generate more switching noise.

FIGURE 6. Flyback Step-Up Converter

Typical Applications (Continued)

D_1 = International Rectifier 50SQ060
D_2 = 1N4148
$I_{out\ (min)}$ = 1A
f_O = 100 kHz
T = Transformer made of a core Fenoxcube 1811PA2503B7
Primary = 8 turns with 5 strands #29
Secondary = 6 turns with 15 strands #30
Sense = 25 turns with 1 strand #30
windings should be interleaved in order to improve the coupling and regulation.

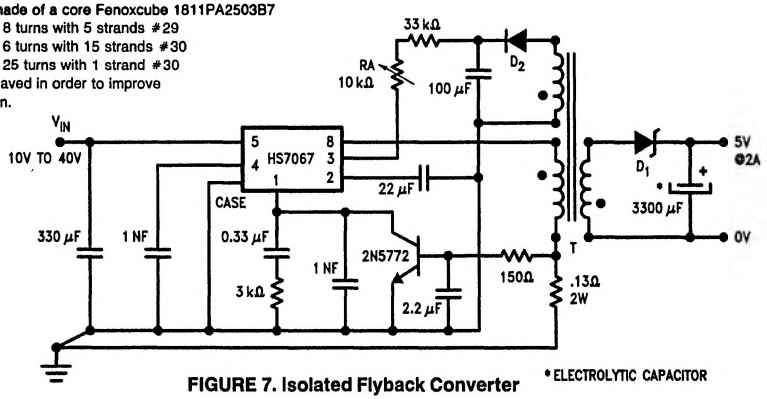
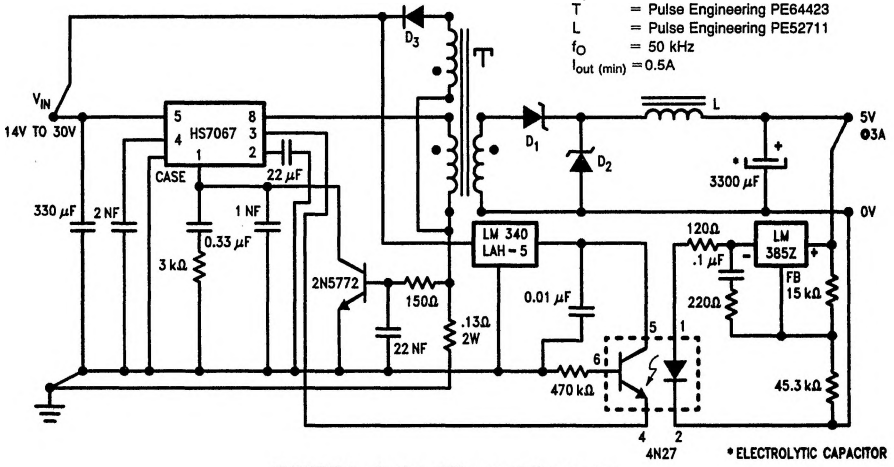


FIGURE 7. Isolated Flyback Converter *ELECTROLYTIC CAPACITOR TL/K/6746-12

D_1 = D_2 = International Rectifier 50SQ060
D_3 = Unitrode UES1302
T = Pulse Engineering PE64423
L = Pulse Engineering PE52711
f_O = 50 kHz
$I_{out\ (min)}$ = 0.5A



*ELECTROLYTIC CAPACITOR

FIGURE 8a. Isolated Forward Converter TL/K/6746-13

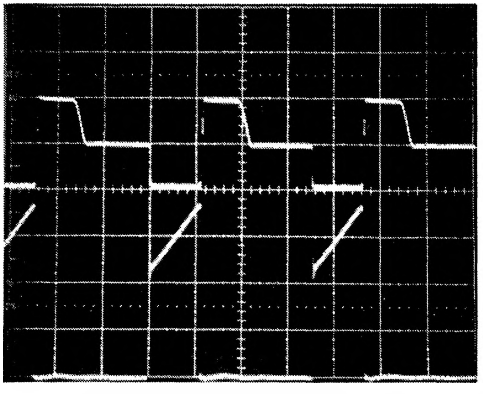


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Figure 8b shows the typical forward converter waveforms in continuous mode which can be observed using the circuit from *Figure 8a*. Top waveform is the voltage across the switch (20V/div). Bottom waveform is the current throughout the switch (1A/dv). Horizontal Scale = 5 µS/dir. V_{in} = 20V; V_{out} = 5V @ 3A.

Figure 8b.

Typical Applications (Continued)

An LM 385z (adjustable reference) is used as a comparator and error amplifier. This reference always wants to maintain 1.2V between pins 1 and 2 and will draw as much current as necessary from the opto-coupler to achieve this. Therefore, the feedback loop is virtually independent of the gain of the opto-coupler.

Performance Data

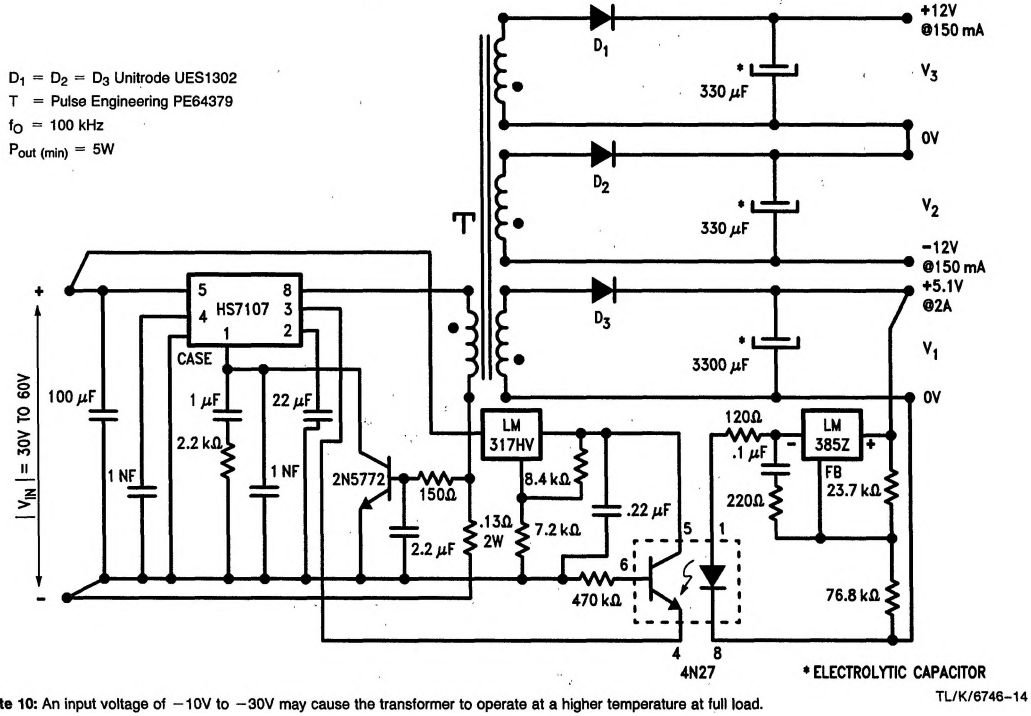
Parameter	Conditions	Result
Efficiency	V_{out} = 5V @ 3A V_{in} = 30V	78%
Line Regulation	V_{out} = 5V @ 3A 14V ≤ V_{in} ≤ 30V	0.1%
Load Regulation	V_{out} = 5V V_{in} = 20V 0.5A ≤ I_{out} ≤ 3A	0.1%

Isolated Telecom Converter

Figure 9 shows an isolated triple output converter which will transform a positive or negative input voltage of 32V to 60V to an uncommitted triple output of +12V, −12V, and 5V, which may be later referenced to the system ground. This converter is ideal for a step down converter of high positive voltage or high negative voltage such as −48V used in telecom circuits.

Performance Data

Parameter	Conditions	Result
Efficiency	V_1 = 5.1V @ 2A V_2 = −12V @ 150 mA V_3 = 12V @ 100 mA $\|V_{in}\|$ = 48V	62%
Line Regulation on Main Secondary	40V ≤ $\|V_{in}\|$ ≤ 60V V_1 = 5.1V @ 2A V_2 = −12V @ 150 mA V_3 = +12V @ 150 mA	0.8%
Load Regulation on Main Secondary	$\|V_{in}\|$ = 48V V_1 = 5.1V V_2 = 12V @ 150 mA V_3 = 12V @ 150 mA 0.5 ≤ I_{out} ≤ 2A	1%
Load Regulation on 12V Secondary for Simultaneous Load Changes	$\|V_{in}\|$ = 48V V_1 = 5.1V @ 2A V_2 = −12V V_3 = 12V 75 mA ≤ I_{out} ≤ 150 mA	5%



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Note 10: An input voltage of −10V to −30V may cause the transformer to operate at a higher temperature at full load.

FIGURE 9. Telecom Flyback Converter

Application Hints

DUTY CYCLE LIMITING

In a flyback converter, the error amplifier sees 0V at the output of the converter during the initial turn-on, and forces the duty cycle to 100% until it sees the output voltage rising to the final value; but no voltage will appear if the switch does not turn off (see flyback principle). The result is that the core will saturate, reducing the effective impedance of the transformer to about 0Ω, and destroying the pass transistor. To prevent this, the duty cycle must be limited to a value at which the core does not saturate. A diode connected between pins 1 and 2 (*Figure 10*), will limit the duty cycle to about 80%.

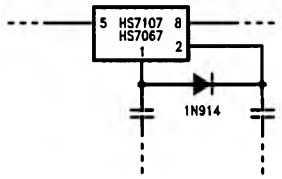

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FIGURE 10. Duty Cycle Limiting Circuit

SOFT START

For any converter, connecting a large capacitor (20 to 200 μF) between pin 2 and the case is recommended to allow the reference voltage to slowly reach its final value after start-up. This allows the HS 7067/7107 to start-up smoothly and minimizes the inrush current. The time constant can be calculated by:

$$T = 10^3 \times C$$

It is always a good practice to incorporate soft start and duty cycle limiting when designing a switching power converter, especially when a current limit circuitry is not utilized.

CURRENT LIMIT

The schematic in *Figure 11* shows how to protect the pass transistor against excessive current, by sensing the current through a series resistor, and shorting the PWM control voltage at pin 1 to ground, using transistor 2N5772 (this is made possible by the 5 MΩ output impedance of the error amplifier), which will cause the pass transistor to turn off.

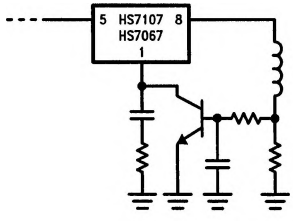

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FIGURE 11. Current Limit Circuitry

The sense resistor should be a low inductance type, otherwise the series inductance creates a high impedance at transients and activates the shutdown circuitry. If such a resistor cannot be found, a 0.1 μF connected in parallel with it will compensate the series inductance.

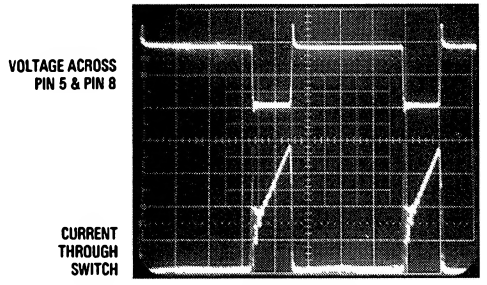
When such a circuitry is used, the duty cycle limiting diode becomes optional, but the soft start capacitor should still be at least 10 μF.

DECOUPLING AND GROUNDING

Special attention should be given to the decoupling of the HS 7107/7067 itself at the input (pin 5), where the capacitor must be at least 100 μF and connected as close to the device as possible. Large switching spikes at the input of the pass transistor can cause breakdown of the junction and destroy the device. (See Figure 12.)

The waveform at the top of the picture represents the voltage across the switch of a typical BUCK (step down) converter. When the switch is turned off, the current in the inductor falls to zero (see waveform at the bottom) and a switching spike occurs across the switch. This spike can reach several tens of volts on top of the normally expected voltage across the switch and lead to stress on the device if the overall voltage exceeds the maximum rating.

The picture below shows a spike of about ten volts with a 330 μF capacitor of average quality.



VERTICAL SCALE: 20 VOLTS/DIV
HORIZONTAL SCALE: 2 μS/DIV

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FIGURE 12

The reference voltage (pin 2) must be decoupled with at least 10 μF and the compensation network (pin 1) should be decoupled with a ceramic capacitor of 1 nF to 10 nF. Switching noise on the reference voltage pin (pin 2) or on the compensation pin (pin 1) can create different types of oscillations and instabilities.

Because of the high current and high voltage capability of the HS 7107/7067 a single point grounding or, at least a grounding where the force ground is separated from the circuit ground, is highly recommended.

Ordering Information (Transformers and Inductors)

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