

32-Channel Vacuum-Fluorescent Display Driver

Ordering Information

	Package Options		
Device	40 Pin Dip	44 Plastic Chip Carrier	Die
HV518	HV518P	HV518PJ	HV518X

Features

- 32 output lines
- 90V output swing
- Active pull-down
- Latches on all outputs
- \Box Up to 6MHz @ $V_{DD} = 5V$
- □ -40°C to +85°C operation

Absolute Maximum Ratings

Supply voltage, V _{DD} ¹	-0.5V to +6.0V
Supply voltage, V _{PP} ¹	-0.5V to +90V
Logic input levels ¹	-0.5V to V _{DD} +0.5V
Continuous total power dissipation ^{2,3}	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm(1/16 inch) from case for 10 seconds	260°C

Notes:

- 1. All voltages referenced to GND.
- 2. Duty cycle is limited by the total power dissipated in the package.
- 3. For operation above 25°C ambient, derate linearly to 85°C at 20mW/°C.

General Description

The HV518 is designed for vacuum fluorescent or DC plasma applications, where it can serve as a segment, digit or matrix display driver. Each device has 32 outputs, 32 latches and a 32 bit cascadable shift register.

Serial data enters the shift register on the LOW-to-HIGH transition of the clock input. With latch enable (\overline{LE}) HIGH, parallel data is transferred to the output buffers through a 32-bit latch. When \overline{LE} is low the data is stored in the latch. When STROBE is LOW, all outputs are enabled; if STROBE is HIGH, all outputs are LOW.

Electrical Characteristics

(over recommended ranges of operating free-air temperature and V_{DD} . Unless otherwise noted, $V_{PP} = 80V$)

Symbol	Parameter		Min	Тур	Max	Units	Conditions
I _{DD}	Supply current				10	mA	$V_{DD} = 5V, f_{CH} = 6.0 \text{ MHz}$
I _{DDQ}	Quiescent supply current				0.5	mA	$V_{DD} = 5.5V, V_{IN} = 0V$
I _{PP}	Supply current				12	mA	Output high, T _A = -40°C
				7	10	mA	Output high, $T_A = 0$ to +85°C
					500	μΑ	Outputs low
V _{OH}	High-level output voltage	HVoutput	70.0			V	I _{OH} = -25mA
		Serial output	4.5	4.9	5	V	$V_{DD} = 5V, I_{OH} = -20\mu A$
V _{OL}	Low-level output	HVoutput			5	V	I _{OL} = 1mA
		Serial output		0.06	0.8	V	I _{OL} =20μA
I _{IH}	High-level logic input current	•		0.1	1	μΑ	$V_{IH} = V_{DD}$
I _{IL}	Low-level logic input current			-0.1	-1	μА	$V_{IL} = 0V$

Note: The total number of ON outputs times the duty cycle must not exceed the allowable package power disspation.

Switching Characteristics ($V_{PP} = 80V$, $C_L = 50$ pF, $T_A = 25$ °C, unless otherwise noted)

Symbol	Parameter			Min	Max	Unit	Conditions
t _d	Delay time, Clock to data outp	ut	V _{DD} = 4.5V		600	ns	C _L =15 pF See Figure 4
t _{DHL}	Delay time, high-to-low-level,	from latch enable	V _{DD} = 4.5V		1.5	μS	See Figure 5
	HVoutput	from strobe			1		See Figure 6
t _{DLH}	Delay time, low-to-high-level	from latch enable	V _{DD} = 4.5V		1.5	μS	See Figure 5
	HVoutput	from strobe			1		See Figure 6
t _{THL}	Transition time, high-to-low-level, HVoutput		V _{DD} = 4.5V		3	μS	See Figure 6
t _{TLH}	Transition time, low-to-high-level, HVoutput		V _{DD} = 4.5V		2.5	μS	See Figure 6

Recommended Operating Conditions (T_A = 25°C, unless otherwise noted)

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic voltage supply		4.5	5.5	V
V_{PP}	High voltage supply		8	80	V
V _{IH}	High-level input voltage (See Fig.3.)	V _{DD} = 4.5V	3.5		V
V _{IL}	Low-level input voltage (See Fig. 3.)	$V_{DD} = 4.5V$		1	V
I _{OH}	High-level output current		-25		mA
I _{OL}	Low-level output current			2	mA
f _{CLK}	Clock frequency (see Figure 3)	$V_{DD} = 4.5V$		6.0	MHz
t _{w(CKH)}	Pulse duration , clock high	$V_{DD} = 4.5V$	83		ns
t _{w(CKL)}	Pulse duration , clock low	$V_{DD} = 4.5V$	83		ns
t _{su}	Setup time, data before clock	$V_{DD} = 4.5V$	75		ns
t _h	Hold time, data after clock	V _{DD} = 4.5V	75		ns
T _A	Operating free-air temperature		-40	85	°C

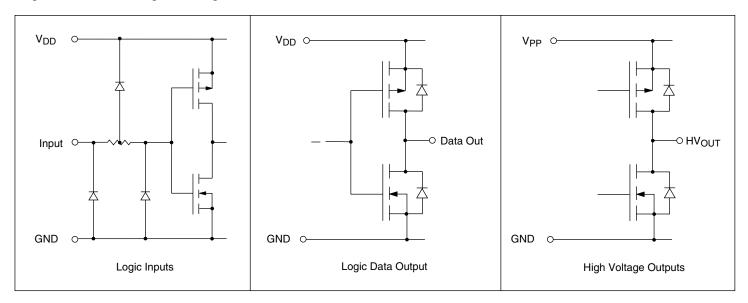
Note:

Power-up sequence should be the following:

- 1. Connect ground.
- 2. Apply V_{DD}.
- 3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
- Apply V_{PP}
- 5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits



Parameter Measurement Information

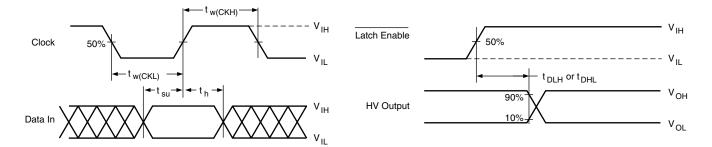


Figure 3: Input Timing Voltage Waveforms

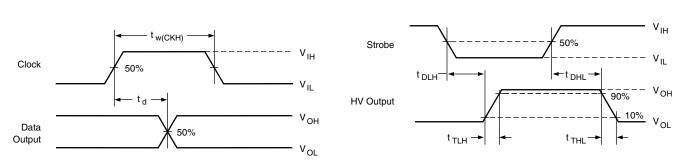


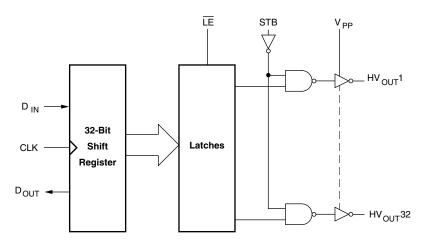
Figure 4

Figure 6: Switching-Time Voltage Waveforms

Figure 5

Note: For testing purposes, all input pulses have maximum rise and fall times of 30 nsec.

Block Diagram



Truth Tables

Input

Data In	CLK	Data Out
Н		Н
L		L
Х	No Change	*

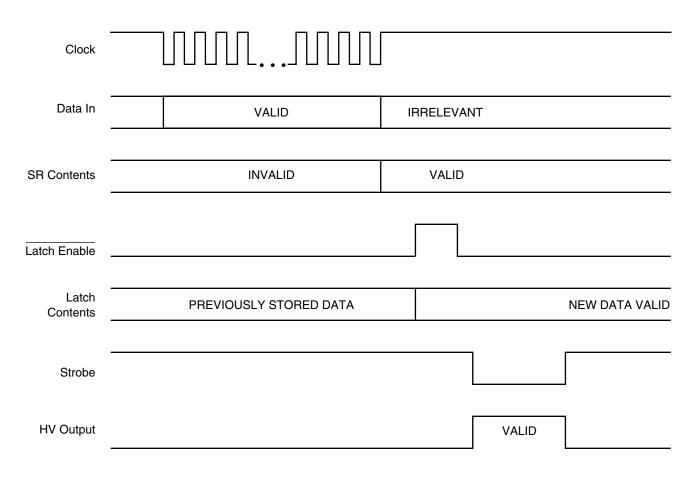
^{*} Previous state

Output

Data In	<u>LE</u>	STB	HV Outputs
Χ	Х	Н	All Low
Н	Н	L	High
L	Н	L	Low
Х	L	L	*

^{*} Previous state

Typical Operating Sequence



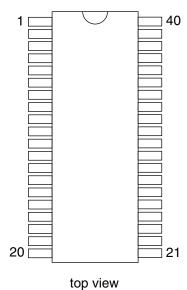
Pin Configurations

Package Outline

HV518

40 Pin Dual-In-Line Package

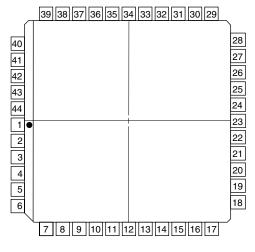
Pin	Function	Pin	Function
1	V_{PP}	21	Clock
2	Serial Out	22	ΙΕ
3	HV _{OUT} 32	23	HV _{OUT} 16
4	HV _{OUT} 31	24	HV _{OUT} 15
5	HV _{OUT} 30	25	HV _{OUT} 14
6	HV _{OUT} 29	26	HV _{OUT} 13
7	HV _{OUT} 28	27	HV _{OUT} 12
8	HV _{OUT} 27	28	HV _{OUT} 11
9	HV _{OUT} 26	29	HV _{OUT} 10
10	HV _{OUT} 25	30	HV _{OUT} 9
11	HV _{OUT} 24	31	HV _{OUT} 8
12	HV _{OUT} 23	32	HV _{OUT} 7
13	HV _{OUT} 22	33	HV _{OUT} 6
14	HV _{OUT} 21	34	HV _{OUT} 5
15	HV _{OUT} 20	35	HV _{OUT} 4
16	HV _{OUT} 19	36	HV _{OUT} 3
17	HV _{OUT} 18	37	HV _{OUT} 2
18	HV _{OUT} 17	38	HV _{OUT} 1
19	Strobe	39	Data In
20	GND	40	V_{DD}



40-pin DIP

HV518 44 Pin J-Lead Package

Pin	Function	Pin	Function
1	V_{PP}	23	Clock
2	Serial Out	24	<u>LE</u>
3	HV _{OUT} 32	25	HV _{OUT} 16
4	HV _{OUT} 31	26	HV _{OUT} 15
5	HV _{OUT} 30	27	HV _{OUT} 14
6	N/C	28	N/C
7	HV _{OUT} 29	29	N/C
8	HV _{OUT} 28	30	HV _{OUT} 13
9	HV _{OUT} 27	31	HV _{OUT} 12
10	HV _{OUT} 26	32	HV _{OUT} 11
11	HV _{OUT} 25	33	HV _{OUT} 10
12	HV _{OUT} 24	34	HV _{OUT} 9
13	HV _{OUT} 23	35	HV _{OUT} 8
14	HV _{OUT} 22	36	HV _{OUT} 7
15	HV _{OUT} 21	37	HV _{OUT} 6
16	HV _{OUT} 20	38	HV _{OUT} 5
17	HV _{OUT} 19	39	HV _{OUT} 4
18	N/C	40	HV _{OUT} 3
19	HV _{OUT} 18	41	HV _{OUT} 2
20	HV _{OUT} 17	42	HV _{OUT} 1
21	Strobe	43	Data In
22	GND	44	V_{DD}



top view