40-Channel Symmetric Row Driver

Ordering Information

Device	Package Options			
	80-Lead Ceramic Gullwing	**64-Lead 3-Sided Plastic Gullwing**	**Die in waffle pack**	**80-Lead Ceramic Gullwing** (MIL-STD-883 Processed*)
HV7224	HV7224DG	HV7224PG	HV7224X	RBHV7224DG

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ❏ Processed with HVCMOS® technology
- ❏ Symmetric row drive (reduces latent imaging in ACTFEL displays)
- ❏ Output voltage up to 240V
- ❏ Low-power level shifting
- ❏ Source/Sink current 70mA (min.)
- ❏ Shift Register Speed 3MHz
- ❏ Pin-programmable shift direction (DIR, SHIFT)
- ❏ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +7V
Supply voltage, V_{PP}		-0.5V to +260V
Logic input levels		-0.5V to V_{DD} +0.5V
Continuous total power dissipation[2]	Plastic Ceramic	1200mW 1900mW
Operating temperature range	Plastic Ceramic	-40°C to +85°C -55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 19mW/°C for ceramic.

General Description

The HV72 is a low-voltage serial to high-voltage parallel converters with push-pull outputs. It is especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays.

When the data reset pin (DR_{IO}) is at logic high, it will reset all the outputs of the internal shift register to zero. At the same time, the output of the shift register will start shifting a logic high from the least significant bit to the most significant bit. The DR_{IO} can be triggered at any time. The DIR and SHIFT pins control the direction of data shift through the device. When DIR is at logic high, DR_{IOA} is the input and DR_{IOB} is the output. When DIR is grounded, DR_{IOB} is the input and the DR_{IOA} is the output. See the Output Sequence Operation Table for output sequence. The POL and OE pins perform the polarity select and output enable function respectively. Data is loaded on the low to high transition of the clock. A logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low. All outputs will be in High-Z state if OE is at logic high. Data output buffers are provided for cascading devices.

Electrical Characteristics

(over recommended operating conditions of V_{DD} = 5V, V_{PP} = 240V, and T_A = 25°C unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			10	mA	f_{CLK} = 3MHz
I_{PP}	High voltage supply current			2.0	mA	Outputs low or High-Z
				4.0	mA	One Output High[1]
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	190		V	I_O= -70mA
		Data out	4.5		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}		50	V	I_O= 70mA
		Data out		0.5	V	I_O= 100µA
I_{IH}	High-level logic input current			1.0	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current			-1.0	µA	V_{IL} = 0V
I_{SAT}	Saturation current HV_{OUT}	P-Ch	-80		mA	
		N-Ch	75		mA	

Note:

1. Only one output can be turned on at a time.

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		3.0	MHz	
$t_{W (H/L)}$	Pulse width - clock high or low	150		ns	
t_{SUD}	Data set-up time before clock rises	50		ns	
t_{HD}	Data hold time after clock rises	50		ns	
t_{SUC}	HV_{OUT} delay from clock rises (Hi-Z to H or L)		1.0	µs	C_L = 330pF // R_L = 10kΩ
t_{SUE}	HV_{OUT} delay from $\overline{\text{Output Enable}}$ falls		600	ns	C_L = 330pF // R_L = 10kΩ
t_{HC}	HV_{OUT} delay from clock rises (H or L to Hi-Z)		2.0	µs	C_L = 330pF // R_L = 10kΩ
t_{HE}	HV_{OUT} delay from $\overline{\text{Output Enable}}$ rises		600	ns	C_L = 330pF // R_L = 10kΩ
t_{DHL}*	Delay time clock to data output falls		250	ns	C_L = 15pF
t_{DLH}*	Delay time clock to data output rises		250	ns	C_L = 15pF
t_{ONF}	HV_{OUT} fall time		2.0	µs	C_L = 330pF // R_L = 10kΩ
t_{ONR}	HV_{OUT} rise time		2.0	µs	C_L = 330pF // R_L = 10kΩ
t_{POW}	$\overline{\text{POL}}$ pulse width	3.0		µs	
t_{OEW}	$\overline{\text{Output Enable}}$ pulse width	3.0		µs	
	Slew rate, V_{PP} or GND		45	V/µs	One active output driving 4.7nF load

* The delay is measured from the trailing edge of the clock but the data is triggered by the rising edge of the clock. There is an internal delay for the data output which is equal to t_{WH}. Therefore the delay is measured from the trailing edge of the clock.

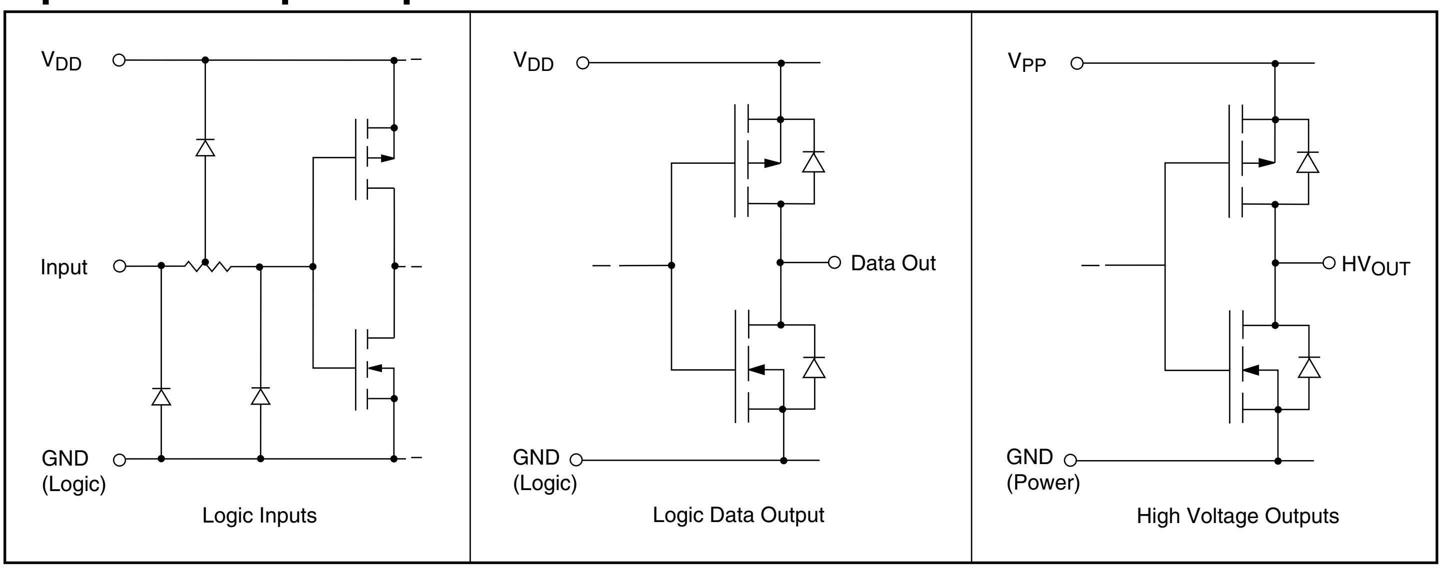
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		4.5	5.5	V
V_{PP}	High voltage supply†		0	240	V
V_{IH}	High-level input voltage		0.7 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		0	0.2V_{DD}	V
f_{CLK}	Clock frequency			3	MHz
I_O	High voltage output current			±70	mA
T_A	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	°C
I_{OD}	Allowable pulse current through output diode			±300	mA

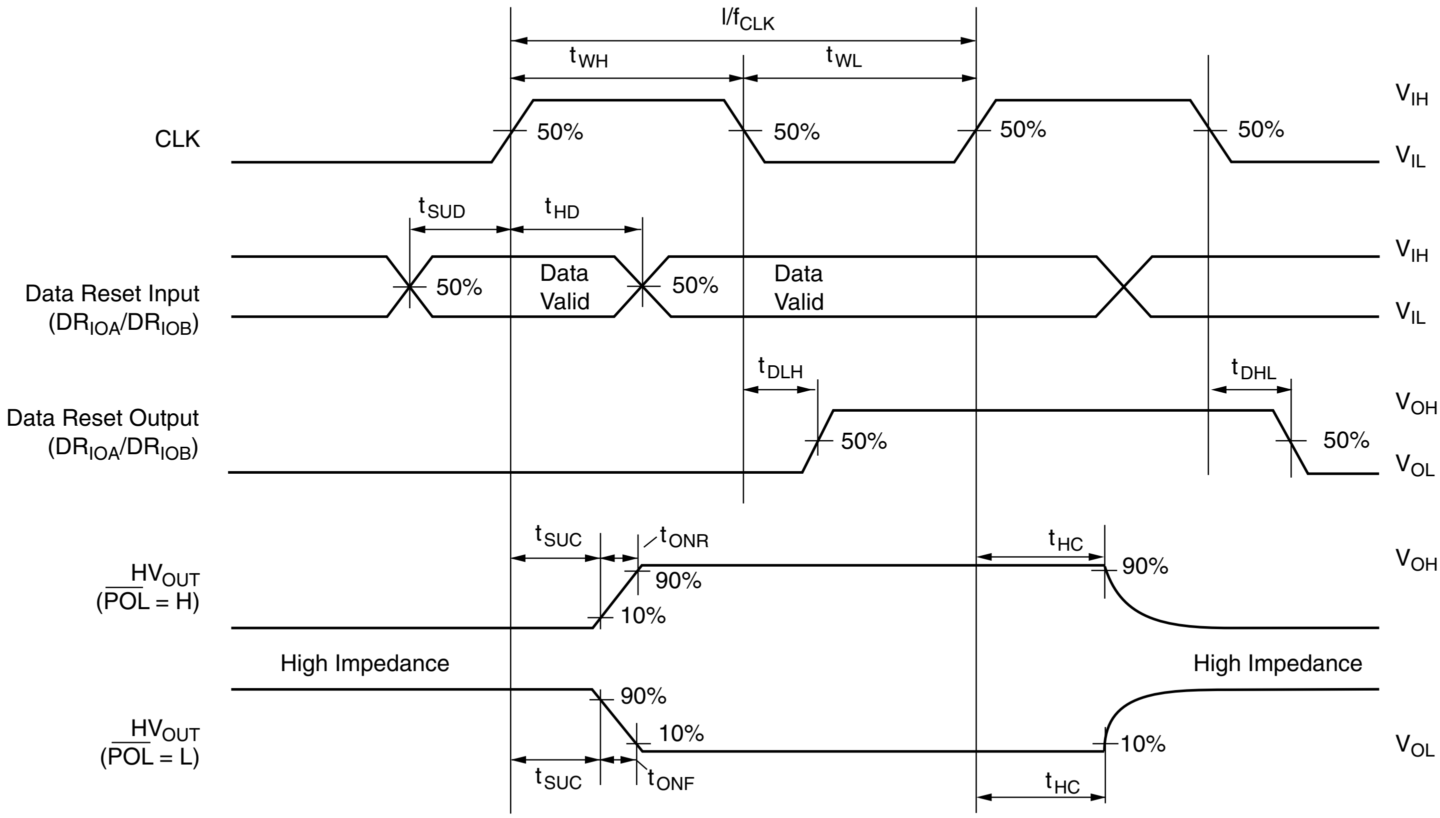
Notes:
† Output will not switch at V_{PP} = 0V.
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.
5. The V_{PP} should not drop below V_{DD} or float during operation.

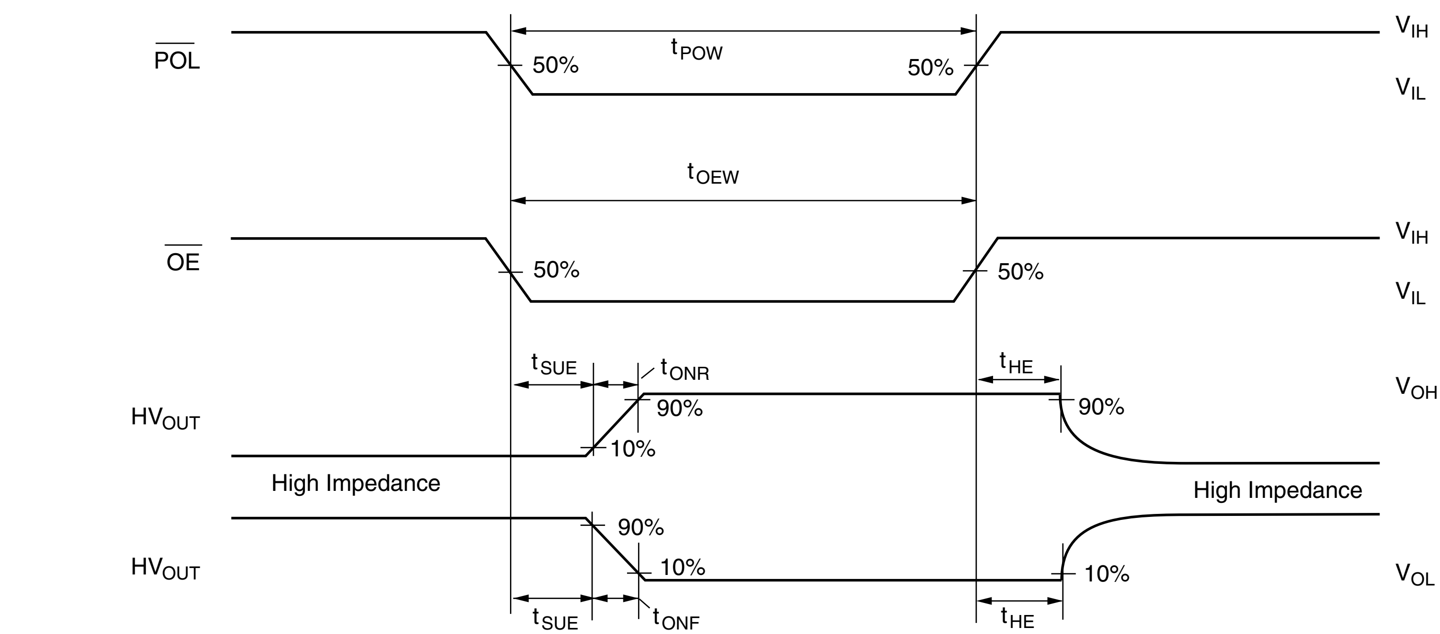
Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits

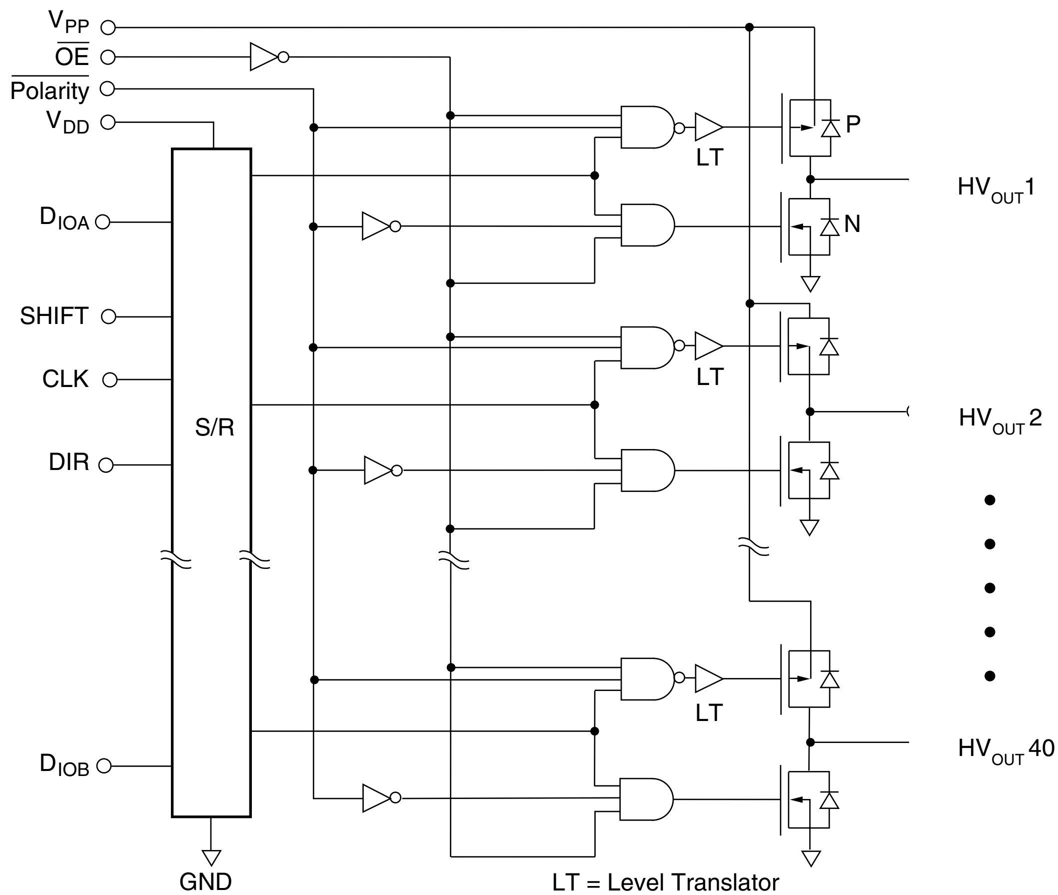


Switching Waveforms





Functional Block Diagram



Function Table

I/O Relations	Inputs					HV Outputs
	CLK	DIR	S/R Data	$\overline{POL}$	$\overline{OE}$	
O/P HIGH	X	X	H	H	L	H
O/P OFF	X	X	L	X	L	HIGH-Z
O/P LOW	X	X	H	L	L	L
O/P OFF	X	X	X	X	H	All O/P HIGH-Z

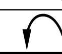
Notes:

H = logic high level, L = logic low level, X = irrelevant

Data input (DR_{IO}) loaded on the low-to-high transistion of the clock.

Only one active output can be set at a time.

Output Sequence Operation Table

DIR	Shift	Data Reset In	Data Reset Out	HV_{OUT}# Sequence	Direction*	Option (See pin-out on P. 12-158)
L	L	DR_{IOB}	DR_{IOA}[1]	40 → 1		A
H	L	DR_{IOA}	DR_{IOB}[2]	1 → 40		A
L	H	DR_{IOB}	DR_{IOA}[1]	20 → 1 → 40 → 21		B
H	H	DR_{IOA}	DR_{IOB}[2]	21 → 40 → 1 → 20		B

* Reference to package outline or chip layout drawing.

1.DR_{IOA} is DR_{IOB}delayed by 40 clock pulses.

2. DR_{IOB} is DR_{IOA} delayed by 40 clock pulses.

Pin Configurations

HV72

Option A:

Pin	Function	Pin	Function
1	HV_{OUT}1/40	33	N/C
2	HV_{OUT} 2/39	34	DR_{IOB}
3	HV_{OUT} 3/38	35	$\overline{OE}$
4	HV_{OUT} 4/37	36	NC
5	HV_{OUT} 5/36	37	$\overline{POL}$
6	HV_{OUT} 6/35	38	N/C
7	HV_{OUT} 7/34	39	V_{DD}
8	HV_{OUT} 8/33	40	N/C
9	HV_{OUT} 9/32	41	GND (Logic)
10	HV_{OUT} 10/31	42	GND (Power)
11	HV_{OUT} 11/30	43	N/C
12	HV_{OUT} 12/29	44	V_{PP}
13	HV_{OUT} 13/28	45	HV_{OUT} 21/20
14	HV_{OUT} 14/27	46	HV_{OUT} 22/19
15	HV_{OUT} 15/26	47	HV_{OUT} 23/18
16	HV_{OUT} 16/25	48	HV_{OUT} 24/17
17	HV_{OUT} 17/24	49	HV_{OUT} 25/16
18	HV_{OUT} 18/23	50	HV_{OUT} 26/15
19	HV_{OUT} 19/22	51	HV_{OUT} 27/14
20	HV_{OUT} 20/21	52	HV_{OUT} 28/13
21	V_{PP}	53	HV_{OUT} 29/12
22	N/C	54	HV_{OUT} 30/11
23	GND (Power)	55	HV_{OUT} 31/10
24	GND (Logic)	56	HV_{OUT} 32/9
25	DIR	57	HV_{OUT} 33/8
26	V_{DD}	58	HV_{OUT} 34/7
27	CLK	59	HV_{OUT} 35/6
28	N/C	60	HV_{OUT} 36/5
29	SHIFT	61	HV_{OUT} 37/4
30	N/C	62	HV_{OUT} 38/3
31	DR_{IOA}	63	HV_{OUT} 39/2
32	N/C	64	HV_{OUT} 40/1

Note:

Pin designation for DIR H/L, SHIFT = L.

Example: For DIR = H, pin 1 is HV_{OUT}1.
For DIR = L, pin 1 is HV_{OUT}40.

Pins 65–80 are NC (ceramic only).

HV72

Option B:

Pin	Function	Pin	Function
1	HV_{OUT} 20/21	33	N/C
2	HV_{OUT} 19/22	34	DR_{IOB}
3	HV_{OUT} 18/23	35	$\overline{OE}$
4	HV_{OUT} 17/24	36	N/C
5	HV_{OUT} 16/25	37	$\overline{POL}$
6	HV_{OUT} 15/26	38	N/C
7	HV_{OUT} 14/27	39	V_{DD}
8	HV_{OUT} 13/28	40	N/C
9	HV_{OUT} 12/29	41	GND (Logic)
10	HV_{OUT} 11/30	42	GND (Power)
11	HV_{OUT} 10/31	43	N/C
12	HV_{OUT} 9/32	44	V_{PP}
13	HV_{OUT} 8/33	45	HV_{OUT} 40/1
14	HV_{OUT} 7/34	46	HV_{OUT} 39/2
15	HV_{OUT} 6/35	47	HV_{OUT} 38/3
16	HV_{OUT} 5/36	48	HV_{OUT} 37/4
17	HV_{OUT} 4/37	49	HV_{OUT} 36/5
18	HV_{OUT} 3/38	50	HV_{OUT} 35/6
19	HV_{OUT} 2/39	51	HV_{OUT} 34/7
20	HV_{OUT} 1/40	52	HV_{OUT} 33/8
21	V_{PP}	53	HV_{OUT} 32/9
22	N/C	54	HV_{OUT} 31/10
23	GND (Power)	55	HV_{OUT} 30/11
24	GND (Logic)	56	HV_{OUT} 29/12
25	DIR	57	HV_{OUT} 28/13
26	V_{DD}	58	HV_{OUT} 27/14
27	CLK	59	HV_{OUT} 26/15
28	N/C	60	HV_{OUT} 25/16
29	SHIFT	61	HV_{OUT} 24/17
30	N/C	62	HV_{OUT} 23/18
31	DR_{IOA}	63	HV_{OUT} 22/19
32	N/C	64	HV_{OUT} 21/20

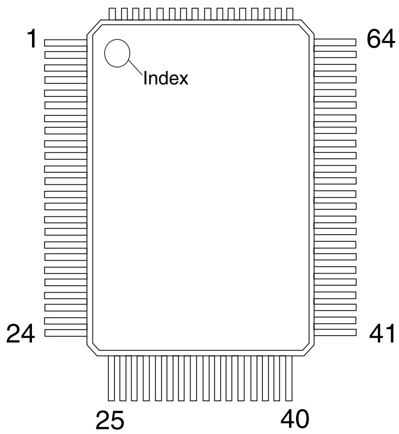
Note:

Pin designation for DIR L/H, SHIFT = H.

Example: For DIR = L, pin 1 is HV_{OUT}20.
For DIR = H, pin 1 is HV_{OUT}21.

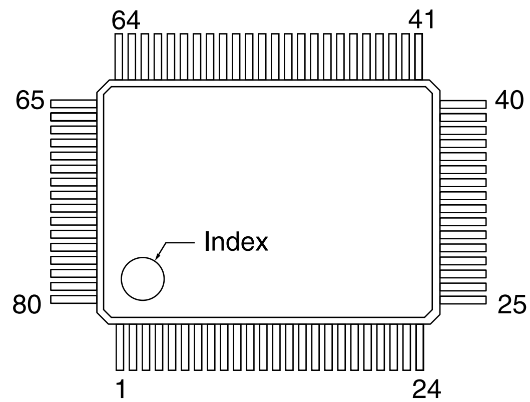
Pins 65–80 are NC (ceramic only).

Package Outline



top view

3-sided Plastic 64-pin Gullwing Package



top view

80-pin Ceramic Gullwing Package

Supertex inc.

1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 744-0100 • FAX: (408) 222-4895
www.supertex.com