

40MHz, 32-Channel Serial to Parallel Converter with Push-Pull Outputs

Ordering Information

| Device | Package Options | | |
|--------|-------------------------|--------------------------|-------------------|
| | 64 Pin Plastic Gullwing | 80-Lead Ceramic Gullwing | Die in Wafer Form |
| HV76 | HV7620PG | HV7620DG | HV7620XW |

Features

- Processed with HVCMOS® technology
- 5V CMOS logic and 12V supply rail
- Output voltage up to 200V
- Low power level shifting
- Source/sink current minimum 50mA
- 40MHz equivalent data rate
- Chip select
- Polarity function
- Forward and reverse shifting options (DIR pin)
- Latched outputs

General Description

The HV76 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

The device has 4 parallel 8-bit shift registers permitting data rate 4 times the speed of one. The data are clocked in simultaneously on all four data inputs with a single clock. Data are shifted in on a low to high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to V_{DD1} , and counterclockwise (CCW) shifting when connected to GND. Operation of the shift register is not affected by the \overline{LE} (latch enable) input. Transfer of data from the shift registers to the latches occurs when the \overline{LE} input is high. Data is stored in the latches when \overline{LE} is low. The current source on the logic inputs provides active pull up when the input pins are open.

Absolute Maximum Ratings

| | | |
|---|-------------------------|----------------|
| Supply voltage ¹ , V_{DD1} | -0.5V to +15V | |
| Supply voltage ¹ , V_{DD2} | -0.5V to +15V | |
| Supply voltage ¹ , V_{PP} | -0.5V to +225V | |
| Logic input levels ¹ | -2.0V to $V_{DD1}+2.0V$ | |
| Continuous total power dissipation ² | Plastic | 1200mW |
| | Ceramic | 1900mW |
| Operating temperature range | Plastic | -40°C to +85°C |
| | Ceramic | -55°C to 125°C |
| Storage temperature range | -65°C to +150°C | |

Notes:

1. All voltages are referenced to GND.
2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 19mW/°C for ceramic.

02/96/022

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics ($V_{DD1} = 5V$, $V_{DD2} = 12V$, $V_{PP} = 200V$ and $T_A = 25^\circ C$)

| Symbol | Parameters | Min | Max | Units | Condition |
|------------|------------------------------------|------|-----|---------|---|
| I_{DD1} | V_{DD1} supply current | | 5 | mA | $f_{CLK} = 10MHz$ |
| I_{DD2} | V_{DD2} supply current | | 20 | mA | $V_{DD2} = V_{DD2} \text{ max}$ $f_{CLK} = 10 \text{ MHz}$ |
| I_{PP} | High voltage supply current | | 2 | mA | All output high or low |
| I_{DD1Q} | Quiescent V_{DD1} supply current | | 100 | μA | All input = V_{DD1} |
| I_{DD2Q} | Quiescent V_{DD2} supply current | | 100 | μA | All input = V_{DD1} |
| V_{OH} | High-level output | 185 | | V | $I_O = -50mA$ |
| V_{OL} | Low-level output | | 20 | V | $I_O = 50mA$ |
| I_{IH} | High-level logic input current | | 1.0 | μA | $V_{IN} = V_{DD1}$ |
| I_{IL} | Low-level logic input current | | -10 | μA | $V_{IN} = 0V$ |
| V_{GG} | HVGND to LVGND voltage difference | -1.0 | 1.0 | V | |

AC Characteristics (Logic signal inputs and data inputs have $t_r, t_f \leq 5ns$. $V_{DD1} = 5V$ or $12V$, $V_{DD2} = 12V$, $V_{PP} = 200V$)

| Symbol | Parameters | Min | Max | Units | Condition |
|--------------------|--|-----------------|-----|-------|---------------------------|
| f_{CLK} | Clock frequency | $V_{DD1} = 5V$ | 10 | MHz | Per register $C_L = 15pF$ |
| | | $V_{DD1} = 12V$ | 5 | MHz | Per register $C_L = 15pF$ |
| t_{WL}, t_{WH} | Clock width high or low | 40 | | ns | |
| t_{SU} | Data set-up time | 20 | | ns | |
| t_H | Data hold time | 20 | | ns | |
| t_{ON}, t_{OFF} | Time from \overline{LE} to HV_{OUT} | | 275 | ns | $C_L = 15pF$ |
| t_{WLE} | Width of \overline{LE} pulse | 25 | | ns | |
| t_{DLE} | Delay time clock to \overline{LE} low to high | 50 | | ns | |
| t_{SLE} | \overline{LE} setup time before clock rises | 20 | | ns | |
| t_{DLF}, t_{DLN} | \overline{BL} or \overline{CS} low to high to HV_{OUT} | | 250 | ns | |
| t_{COF}, t_{CON} | Clock to HV_{OUT} | | 275 | ns | |
| t_{DLH} | Delay time clock to data low to high | | 100 | ns | $C_L = 15pF$ |
| t_{DHL} | Delay time clock to data high to low | | 100 | ns | $C_L = 15pF$ |

Recommended Operating Conditions

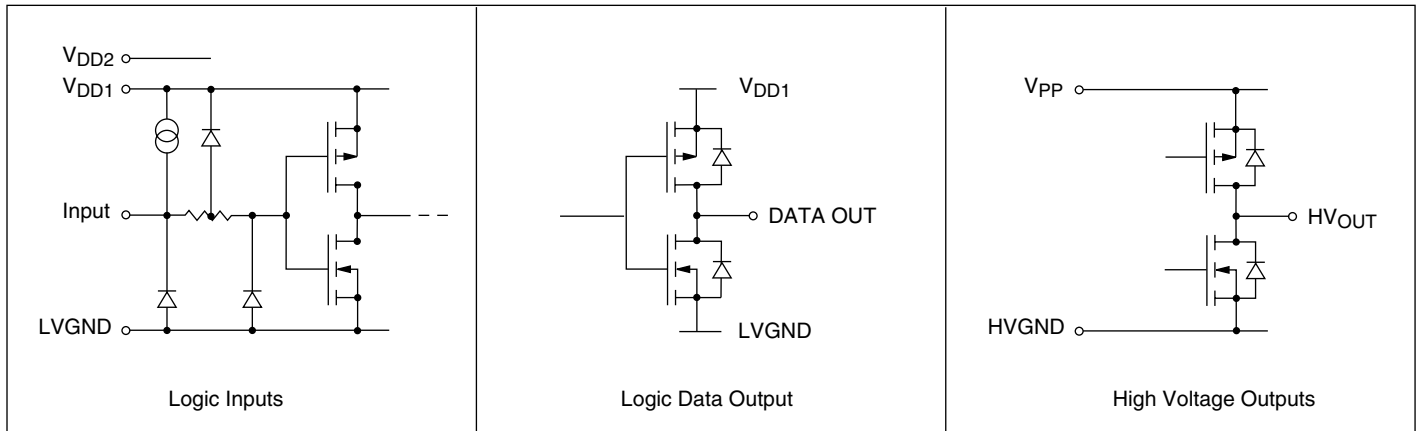
| Symbol | Parameters | Min | Max | Unit | |
|------------------|---|------------------|-----------|------------|------------|
| V_{DD1} | Logic supply voltage | 4.5 | V_{DD2} | V | |
| V_{DD2} | 12V supply voltage | 10.8 | 13.2 | V | |
| V_{PP} | High voltage supply voltage | 50 | 200 | V | |
| V_{IH} | High-level input voltage | $V_{DD1} - 0.5V$ | V_{DD1} | V | |
| V_{IL} | Low-level input voltage | 0 | 0.5 | V | |
| f_{CLK} | Clock frequency | $V_{DD1} = 5V$ | 10 | MHz | |
| | | $V_{DD1} = 12V$ | 5 | MHz | |
| T_A | Operating free-air temperature | Plastic | -40 | +85 | $^\circ C$ |
| | | Ceramic | -55 | +125 | $^\circ C$ |
| I_{OD} | Allowable pulsed current through output diodes ¹ | | 500 | mA | |
| $I_{GND(VPP)}$ | Allowable pulsed V_{PP} or HVGND current ¹ | | 16 | A | |
| $V_{PP(SLEW)}^2$ | Slew rate of V_{PP} | | 340 | V/ μs | |

Notes:

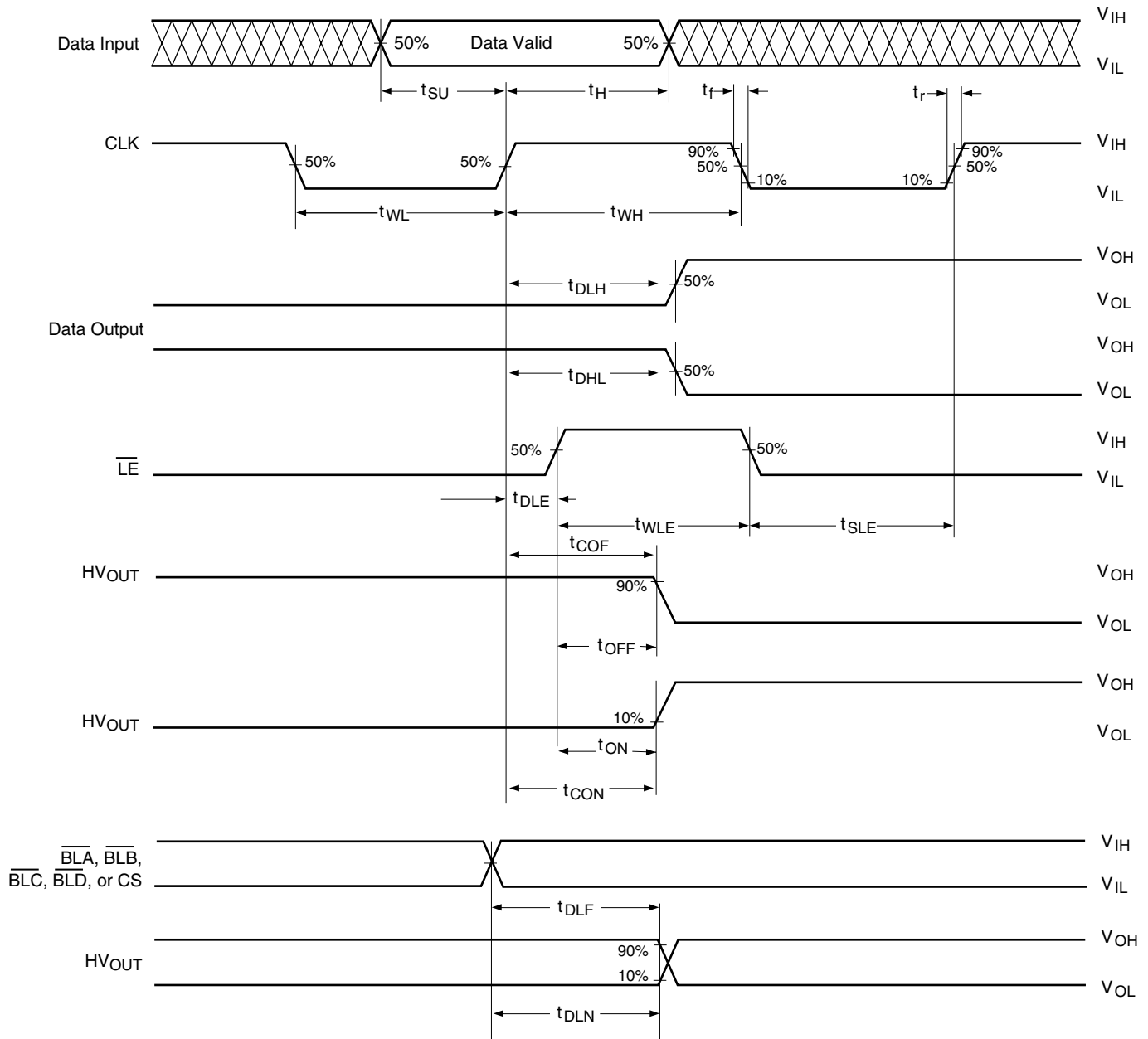
1.The current pulse width = 500ns, duty cycle = 5%.

2.This device cannot be hot-switched for output frequency greater than 500Hz. For output frequency greater than 500Hz, V_{PP} must be ramped.

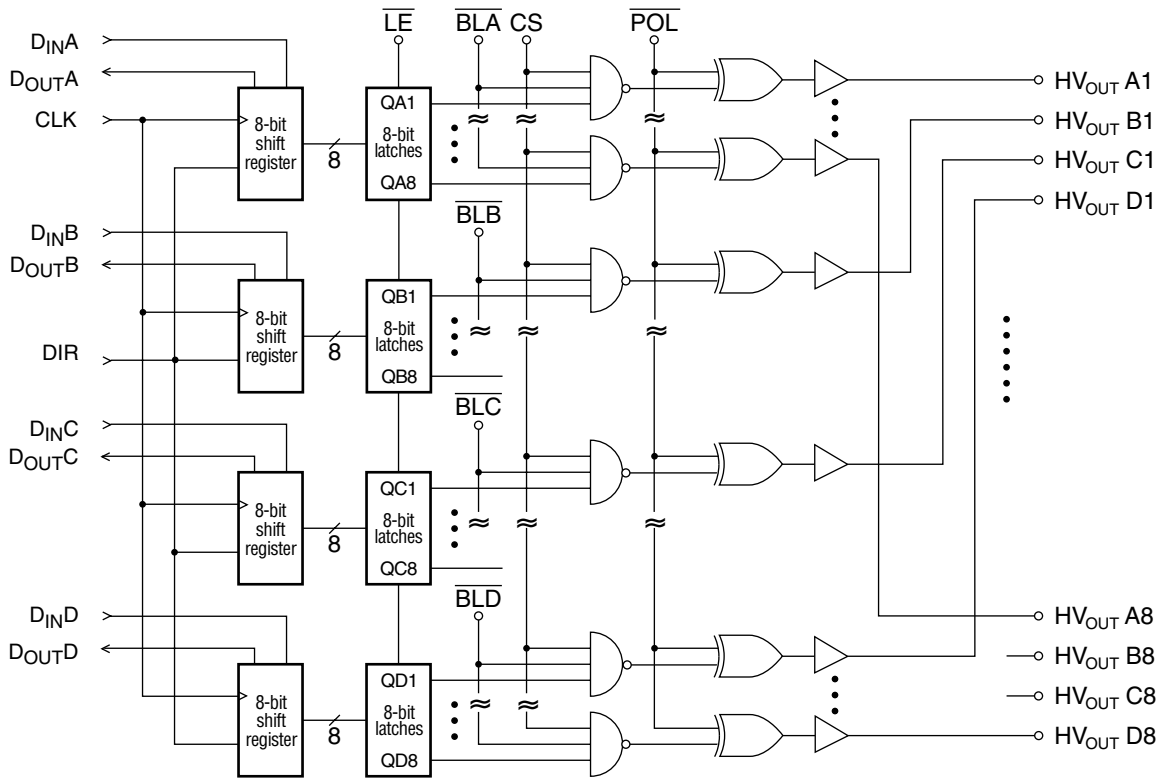
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

| Function | Inputs | | | | | | | | | | | | | HV Outputs | | | | |
|------------------|------------------|------------------|------------------|------------------|-----|----|-----|-----|-----|-----|-----|----|-----|------------------|------------------|------------------|------------------|---|
| | D _{INA} | D _{INB} | D _{INC} | D _{IND} | CLK | LE | DIR | BLA | BLB | BLC | BLD | CS | POL | A | B | C | D | |
| All O/P High | X | X | X | X | X | X | X | X | X | X | X | X | L | L | H | H | H | H |
| All O/P Low | X | X | X | X | X | X | X | X | X | X | X | X | L | H | L | L | L | L |
| “A” Outputs Low | X | X | X | X | X | X | X | L | X | X | X | X | H | L | * | * | * | |
| Normal Polarity | X | X | X | X | X | X | X | H | H | H | H | H | H | No Inversion | | | | |
| Outputs Inverted | X | X | X | X | X | X | X | H | H | H | H | H | L | Inversion | | | | |
| Transparent Mode | H | L | L | L | ↑ | H | X | H | H | H | H | H | H | H | L | L | L | L |
| Data Stored | X | X | X | X | X | L | X | H | H | H | H | H | H | Stored Data | | | | |
| Shift CW | X | X | X | X | ↑ | H | H | H | H | H | H | H | X | A _N | B _N | C _N | D _N | |
| Shift CCW | X | X | X | X | ↑ | H | L | H | H | H | H | H | X | A _{N-1} | B _{N-1} | C _{N-1} | D _{N-1} | |

Notes:

H = High level, L = Low level, X = Irrelevant, ↑ = Low to high transition.
 * = Dependent on previous stage's state before the last CLK ↑ for last LE high.

Power-up sequence:

- GND (HV, LV)
- V_{DD2}
- V_{DD1}
- Logic Input Signals
- V_{PP}

To power down reverse the sequence above.

The V_{PP} should not drop below V_{DD} or float during operation.

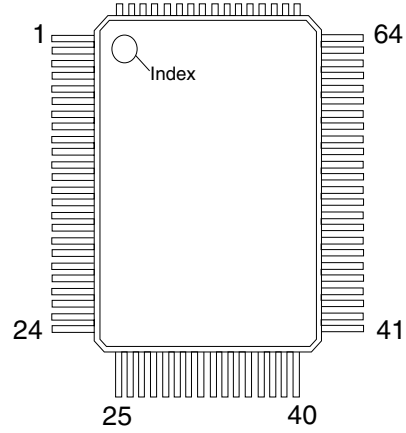
Pin Configurations

Package Outline

HV76

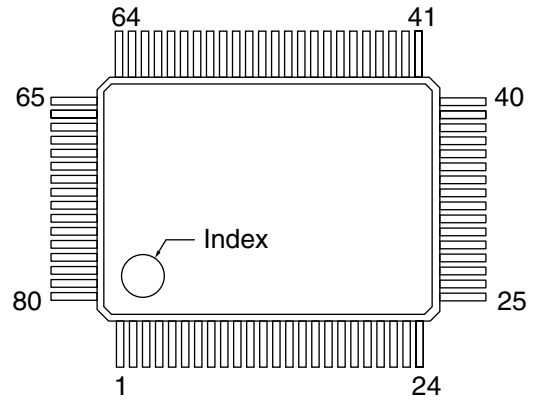
| Pin | Function | Pin | Function |
|-----|----------------------|-----|----------------------|
| 1 | HVGND | 33 | CS |
| 2 | V _{PP} | 34 | D _{OUT} B |
| 3 | HV _{OUT} D8 | 35 | D _{IN} B |
| 4 | HV _{OUT} C8 | 36 | D _{IN} A |
| 5 | HV _{OUT} B8 | 37 | D _{OUT} A |
| 6 | HV _{OUT} A8 | 38 | CLK |
| 7 | HV _{OUT} D7 | 39 | BLA |
| 8 | HV _{OUT} C7 | 40 | BLB |
| 9 | HV _{OUT} B7 | 41 | V _{DD1} |
| 10 | HV _{OUT} A7 | 42 | LVGND |
| 11 | HV _{OUT} D6 | 43 | N/C |
| 12 | HV _{OUT} C6 | 44 | HVGND |
| 13 | HV _{OUT} B6 | 45 | HVGND |
| 14 | HV _{OUT} A6 | 46 | V _{PP} |
| 15 | HV _{OUT} D5 | 47 | HV _{OUT} D4 |
| 16 | HV _{OUT} C5 | 48 | HV _{OUT} C4 |
| 17 | HV _{OUT} B5 | 49 | HV _{OUT} B4 |
| 18 | HV _{OUT} A5 | 50 | HV _{OUT} A4 |
| 19 | V _{PP} | 51 | HV _{OUT} D3 |
| 20 | HVGND | 52 | HV _{OUT} C3 |
| 21 | HVGND | 53 | HV _{OUT} B3 |
| 22 | V _{DD2} | 54 | HV _{OUT} A3 |
| 23 | BLC | 55 | HV _{OUT} D2 |
| 24 | BLD | 56 | HV _{OUT} C2 |
| 25 | LE | 57 | HV _{OUT} B2 |
| 26 | D _{OUT} D | 58 | HV _{OUT} A2 |
| 27 | D _{IN} D | 59 | HV _{OUT} D1 |
| 28 | D _{IN} C | 60 | HV _{OUT} C1 |
| 29 | D _{OUT} C | 61 | HV _{OUT} B1 |
| 30 | POL | 62 | HV _{OUT} A1 |
| 31 | LVGND | 63 | V _{PP} |
| 32 | DIR | 64 | HVGND |

*Pins 65 to 80 are N/C (ceramic only)



top view

3-sided Plastic 64-pin Gullwing Package



top view

80-pin Ceramic Gullwing Package