inmos®

Product data

IMS C011 link adaptor

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The IMS C011 link adaptor is a universal high speed system interconnect, providing full duplex communication according to the INMOS serial link protocol. The link protocol provides synchronised message transmission using handshaken byte streams. Data reception is asynchronous, allowing communication to be independent of clock phase.

The IMS C011 converts the bidirectional serial link data into parallel data streams. It can be used to freely interconnect transputers, INMOS peripheral controllers, I/O subsystems, and microprocessors of different families.

The serial links can be operated at differing speeds; two C011 link adaptors can connect high and low speed links whilst maintaining the synchronised message transmission provided by the link protocol.

This manual details the product specific aspects of the IMS C011 and contains data relevant to the engineering and programming of the device.

Other information relevant to all transputer products is contained in the occam programming manual (supplied with INMOS software products and available as a separate publication), and the transputer development system manual (supplied with the development system).

This edition of the manual is dated October 27, 1986.

The IMS C011 link adaptor allows the user the flexibility of configuring it in one of two modes, and one of two serial link speeds for each mode.

Configuration depends upon the wiring of **SeparateIQ** pin (16) and is as follows:

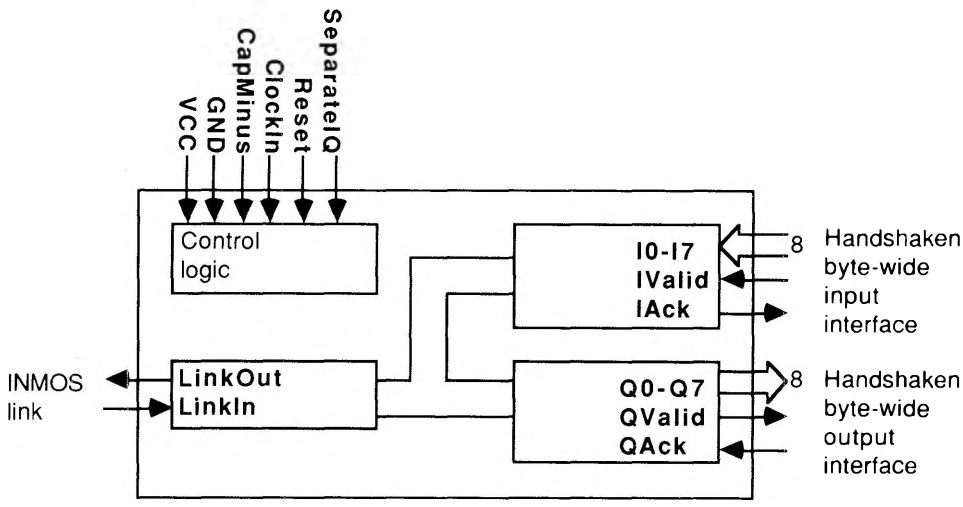
SeparateIQ pin	Mode	Speed of link at Clock=5MHz
Wire to **VCC**	Mode 1	10 Mbits/sec
Wire to **ClockIn**	Mode 1	20 Mbits/sec
Wire to **GND**	Mode 2	10 or 20 Mbits/sec

See Section 8 for pin descriptions and package diagrams.

For compatibility with INMOS products, the clock frequency should be 5MHz.

The following chapters describe the two different modes. Where there is no mention of mode, it may be assumed that the text applies to both modes.

Mode 1 Block Diagram



In mode 1 the link adaptor converts between an INMOS serial link and two independent fully handshaken byte-wide interfaces. One interface is for data coming from the serial link and one for data going to the serial link.

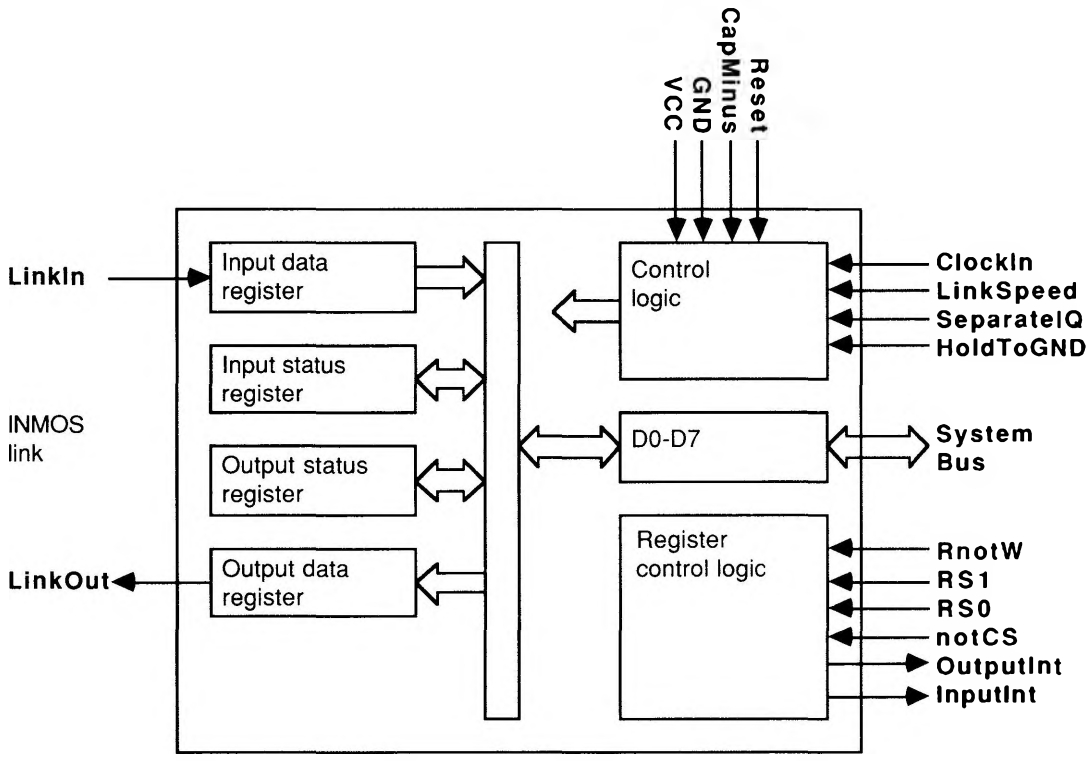
The serial link enables the link adaptor to communicate with another link adaptor, a transputer or an INMOS peripheral processor. Data reception is asynchronous which allows communication to be independent of clock phase. Transfers may proceed in both directions at the same time.

This mode provides programmable I/O pins for a transputer.

The serial links can be operated at differing speeds; when connected by their parallel ports two C011 link adaptors can connect high and low speed links whilst maintaining the synchronised message transmission provided by the link protocol.

The IMS C011 converts the bidirectional serial link data into parallel data streams. It can be used to fully interconnect transputers, INMOS peripheral controllers, I/O subsystems, and microprocessors of different families.

Mode 2 Block Diagram

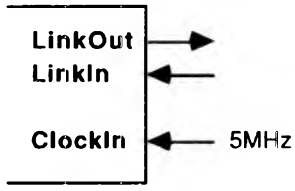


In mode 2 the link adaptor provides an interface between an INMOS serial link and a microprocessor system bus, via an 8-bit bi-directional interface.

This mode has status/control and data registers for both input and output. Any of these can be accessed by the byte wide interface at any time. Two interrupt lines are provided, each gated by an interrupt enable flag. One presents an interrupt on output ready, and the other on data present.

The IMS C011 converts the bidirectional serial link data into parallel data streams. It can be used to fully interconnect transputers, INMOS peripheral controllers, I/O subsystems, and microprocessors of different families.

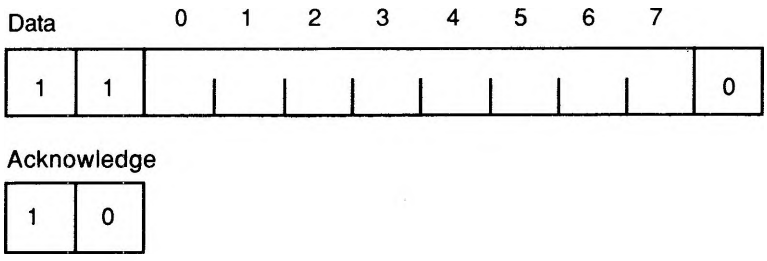
Standard Clock Input



The INMOS serial links are standard across all products in the transputer product range. All transputers will support a standard communications frequency of 10 Mbits/sec, regardless of processor performance. Thus transputers of different performance can be connected directly and future transputer systems will be able to communicate directly with those of today.

Each link consists of a serial input and a serial output, both of which are used to carry data and link control information.

Link protocol

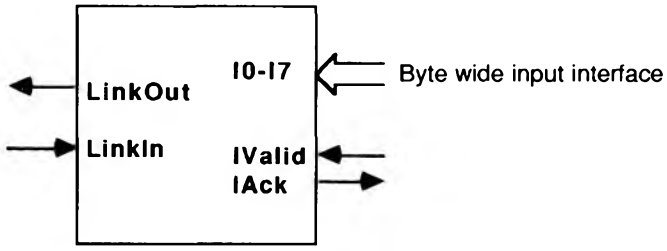


A message is transmitted as a sequence of bytes. After transmitting a data byte, the sender waits until an acknowledge has been received, signifying that the receiver is ready to receive another byte. The receiver can transmit an acknowledge as soon as it starts to receive a data byte, so that transmission can be continuous. This protocol provides handshaken communication of each byte of data, ensuring that slow and fast transputers communicate reliably.

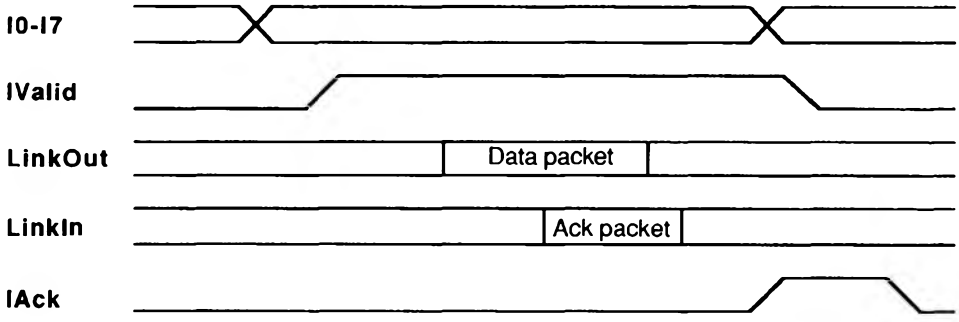
When there is no activity on the links they remain at logic 0, **GND** potential.

A 5 MHz input clock is used, from which internal timings are generated. Link communication is not sensitive to clock phase. Thus, communication can be achieved between independently clocked systems as long as the communications frequency is within the specified tolerance.

Output to link

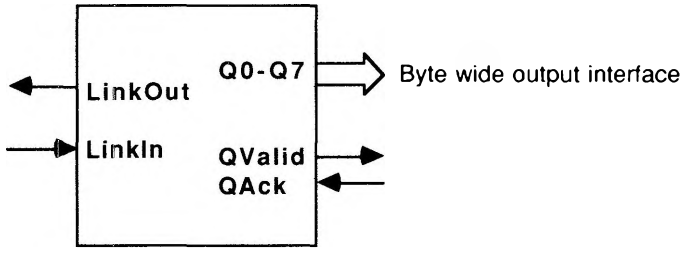


Timing of output to link

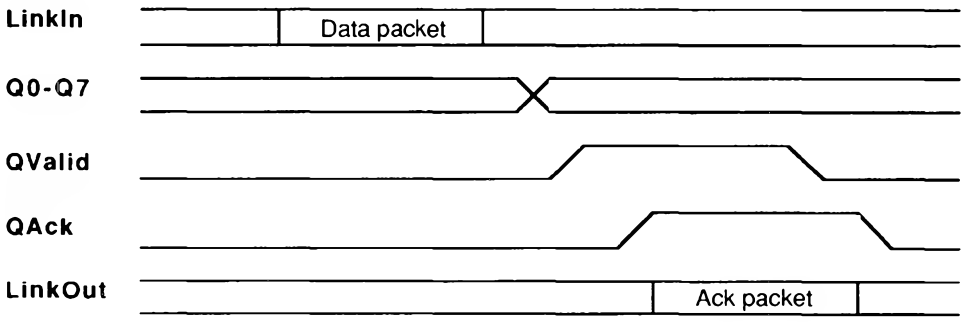


IValid and **IAck** provide a simple two wire handshake. Data is presented to the link adaptor on **I0-I7**, and **IValid** is taken high to commence the handshake. The link adaptor transmits the data through the serial link, and acknowledges receipt of the data on **IAck** when it has received the acknowledgment from the serial link. **IValid** is then taken low, and the link adaptor completes the handshake by taking **IAck** low.

Input from link



Timing of input from link



The link adaptor receives data from the serial link, presents it on **Q0**-**Q7**, and takes **QValid** high to commence the handshake. Receipt of the data is acknowledged on **QAck**, and the link adaptor then transmits an acknowledgement on the serial link. The link adaptor takes **QValid** low and the handshake is completed by taking **QAck** low.

In mode 2 the link adaptor is controlled at the parallel interface by reading and writing status/control registers, and by reading and writing data registers. Two interrupt lines are provided. One indicates that the link adaptor is ready to output a byte to the link, and the other indicates that it is holding a byte which it has read from the link.

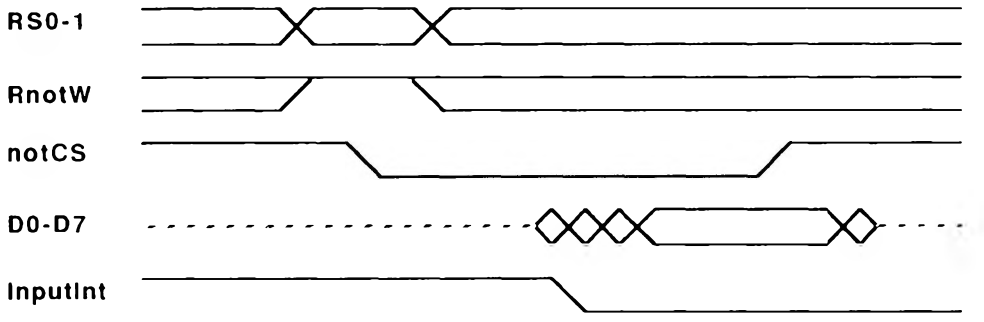
Parallel interface

One of the four registers is selected by **RS0** and **RS1**. If a new value is to be written into the selected registers, it is set up on **D0-D7** and **RnotW** is taken low. **notCS** is then taken low. On read cycles, the current value of the selected register is placed on **D0-D7**.

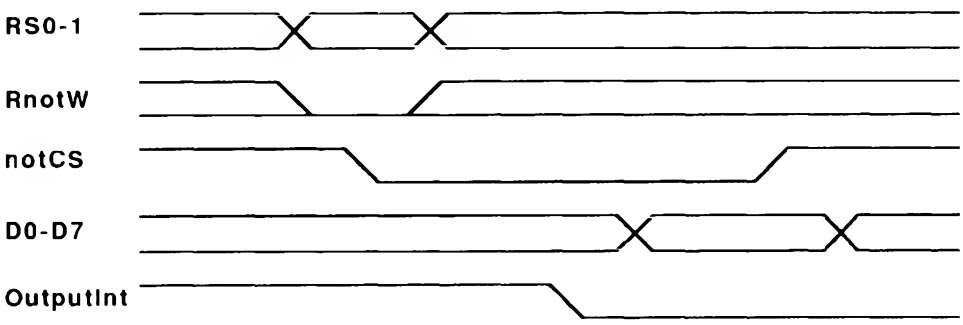
RS1	RS0	RnotW	Function
0	0	1	**D0-D7** := input data register
0	1	0	output data register := **D0-D7**
1	0	1	**D0-D7** := input status register
1	0	0	input status register := **D0-D7**
1	1	1	**D0-D7** := output status register
1	1	0	output status register := **D0-D7**

Note : Writing to the input data register has no effect and reading the output data register will result in undefined data on the data bus. Unused bit positions must be set to zero in both the input status register and the output status register.

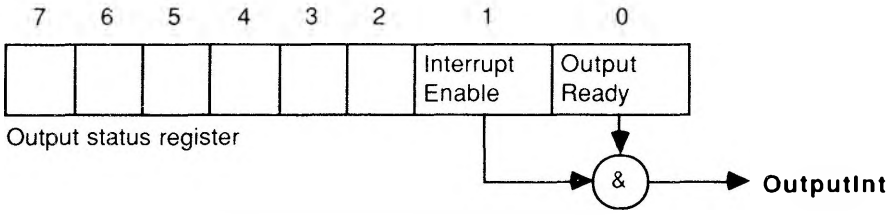
Read register timing diagram



Write register timing diagram

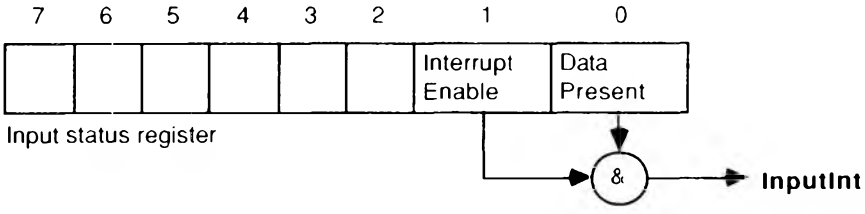


Output to link



The output ready status bit indicates that the serial link is ready to send a byte of data. The bit is set high on reset, and when the link adaptor receives an acknowledgement from the serial link. It is reset low when a data byte is written to the output data register on the parallel interface. **OutputInt** is set high if both output ready and interrupt enable are set high. Output interrupt enable is set low on reset.

Input from link



The data present status bit indicates that the serial link has received a byte of data. The bit is reset low when the data byte is read from the input data register on the parallel interface, this causes an acknowledgement to be transmitted on the serial link. **InputInt** is set high if both data present and interrupt enable are set high. Input interrupt enable and **data present** are both set low on reset.

Note: Parameters given in this section will be revised as a result of further characterization.

7.1 Absolute maximum ratings

Parameter		Min	Max	Unit	Note
VCC	DC supply voltage	0	7.0	V	1, 2, 3
VI,VO	Input or output voltage on any pin	-0.5	**VCC**+0.5	V	1, 2, 3
OSCT	Output short circuit time (one pin)		1	s	1
TS	Storage temperature	-65	150	°C	1
TA	Ambient temperature under bias	-55	125	°C	1
PD	Power dissipation rating		600	mW	

Notes

1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 All voltages are with respect to **GND**.

3 This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however it is advised that normal precautions be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level such as **GND**.

7.2 Recommended operating conditions

Parameter		Min	Max	Unit	Note
VCC	DC supply voltage	4.5	5.5	V	1
VI,VO	Input or output voltage	0	**VCC**	V	1,2
CL	Load capacitance on any pin		50	pF	
TA	Operating temperature range	0	70	°C	

Notes

1 All voltages are with respect to **GND**.

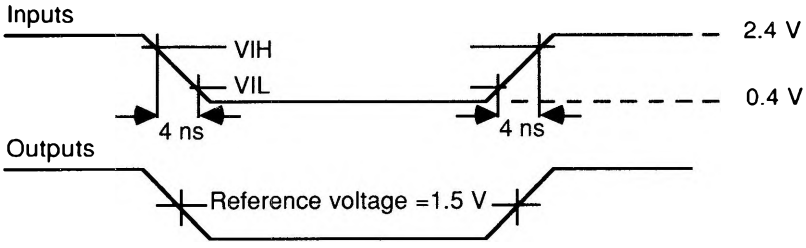
2 Excursions beyond the supplies are permitted but not recommended; see DC characteristics.

7.3 DC characteristics

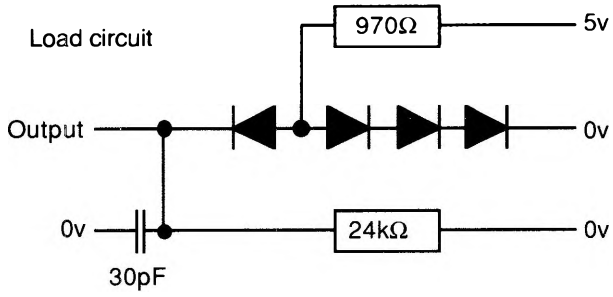
Parameter		Conditions	Min	Max	Unit
VIH	High level input voltage		2.0	**VCC**+0.5	V
VIL	Low level input voltage		-0.5	0.8	V
II	Input current	**GND** < **VI**< **VCC**		±200	μ A
VOH	Output high voltage	**IOH** = -2mA	**VCC**-1		V
VOL	Output low voltage	**IOL** = 4mA		0.4	V
IOS	Output short circuit current	**GND** < **VO** < **VCC**		50	mA
IOZ	Tristate output current	**GND** < **VI** <**VCC**		±200	μ A
PD	Power dissipation			100	mW
CIN	Input capacitance	f = 1 MHz		7	pF
COZ	Output capacitance in tristate	f = 1 MHz		10	pF

Note : 4.5 V < **VCC** < 5.5 V
0 °C < **TA** < 70 °C
Input clock frequency = 5 MHz
All voltages are with respect to **GND**

7.4 Measurement of AC characteristics



Reference points for AC characteristics



Load circuit for AC measurements

The load circuit approximates to two TTL loads, with a total capacitance of 30 pF.

7.5 Connection of INMOS serial links

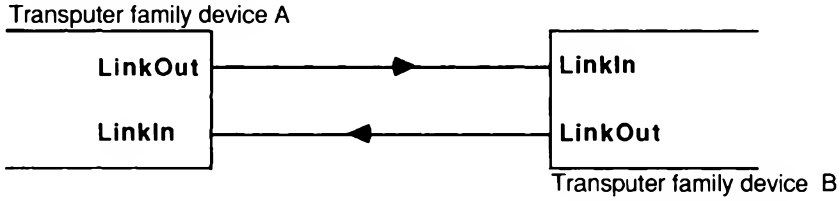
INMOS serial links can be connected in 3 different ways depending on their environment:

1 Directly connected

2 Connected via a series matching resistor

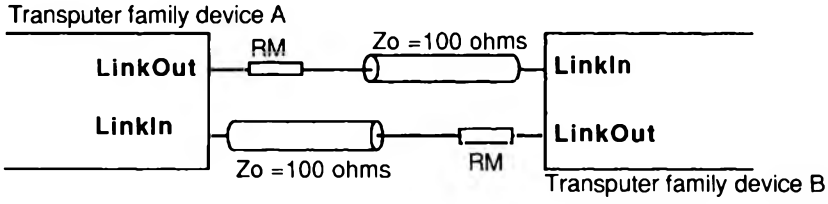
3 Connected via buffers

Direct connection



Direct connection is suitable for short distances on a printed circuit board.

Matched line

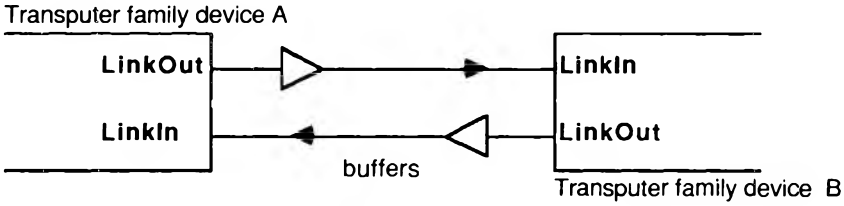


For long wires, approximately >30 cm, then a 100ohm transmission line should be used with series matching resistors.

Parameter		Nom	Max	Unit
RM	Series matching resistor for 100 ohm line.	47		ohm
TD	Delay down line		0.4	bit time

Note that if two connected devices have different values for **TD**, the lower value should be used. With series termination at **LinkOut** the transmission line reflection must return within 1 Bit time. Otherwise line buffers should be used.

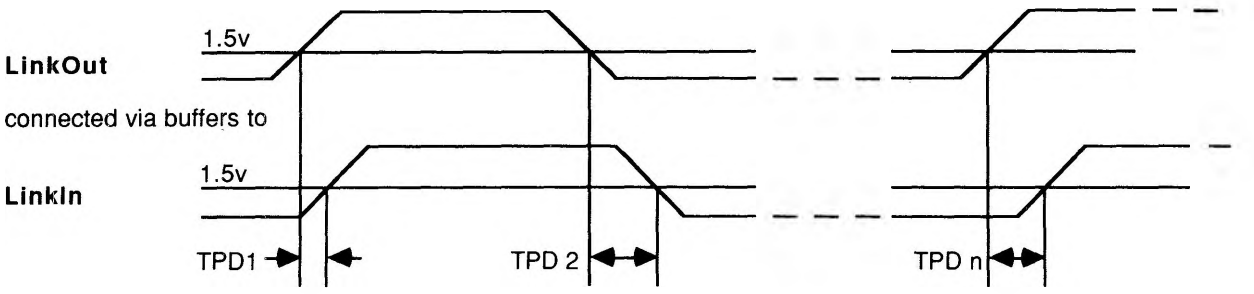
Buffered links



If buffers are used their overall propagation delay, TPD, should be stable within the skew tolerance.

Parameter	Max	Unit
Skew in buffering at 5 Mbits/sec	30	ns
Skew in buffering at 10 Mbits/sec	10	ns
Skew in buffering at 20 Mbits/sec		ns
Rise and fall time of **LinkIn** (10% to 90%)	20	ns

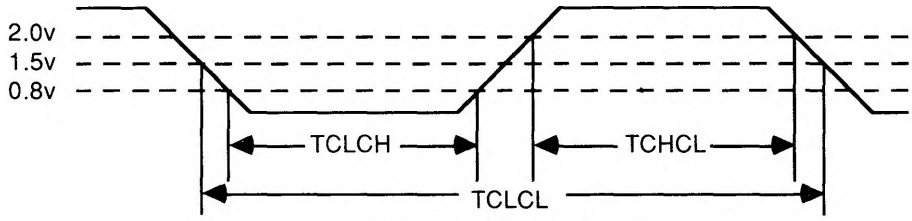
The above figures indicate that buffered links can be realised at 10Mbits/sec. For the case of 20 Mbits/sec, the maximum value can only be specified as a result of further characterisation.



The absolute value of TPD is immaterial because data reception is asynchronous. However, TPD will vary from moment to moment because of ground noise, variation in the power supplies of buffers and the difference in the delay for rising and falling edges. This will vary the length of data bits reaching **LinkIn**. *Skew* is the difference between the maximum and minimum instantaneous values of TPD.

7.6 AC characteristics of system services

ClockIn waveform



ClockIn Waveform diagram

Parameter		Min	Nom	Max	Unit	Note
TCHCL	Clock pulse width high	40			ns	1
TCLCH	Clock pulse width low	40			ns	1
	Rise and fall time of **ClockIn** (10% to 90%)			10	ns	1
TCLCL	Clock period		200	400	ns	2
	Difference in frequencies of **ClockIn** for two devices connected by a link			400	ppm	4
TRHRL	**Reset** pulse width high	8			**ClockIn** periods	3
	Time **VCC** and **ClockIn** valid before reset is taken low		10		ms	3,5

Notes

1 The clock transitions must be monotonic within the range between **VIH** and **VIL**.

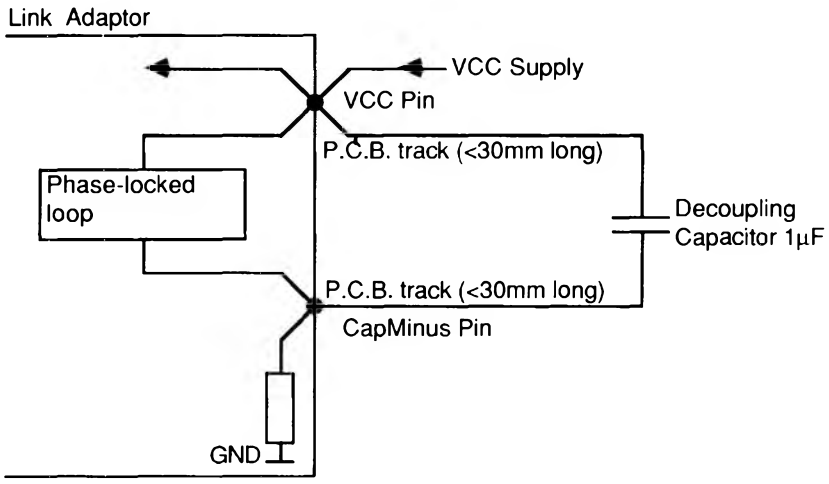
2 The **TCLCL** parameter is measured between corresponding points on consecutive falling edges.

3 During reset, **LinkIn** should be held low. Note that reset forces **LinkOut** to be low.

4 This value allows the use of low cost 200ppm crystal oscillators.

5 When powering up.

Recommended PLL decoupling



Notes

Parameter		Min	Nom	Max	Unit	Note
C	Decoupling capacitor	1			µF	1
	A.C. noise between **VCC** and **GND**			200	mV	2,3
	A.C. noise between **VCC** and ground reference of load capacitance			200	mV	4

1 The decoupling capacitor should be a high-quality tantalum (or other) type, with low series resistance (<1 ohm), and low impedance at high frequency (<10 ohm at 100 MHz). It should be connected between **VCC** and **CapMinus**, with short tracks, and with a star point at the **VCC** pin, as shown.

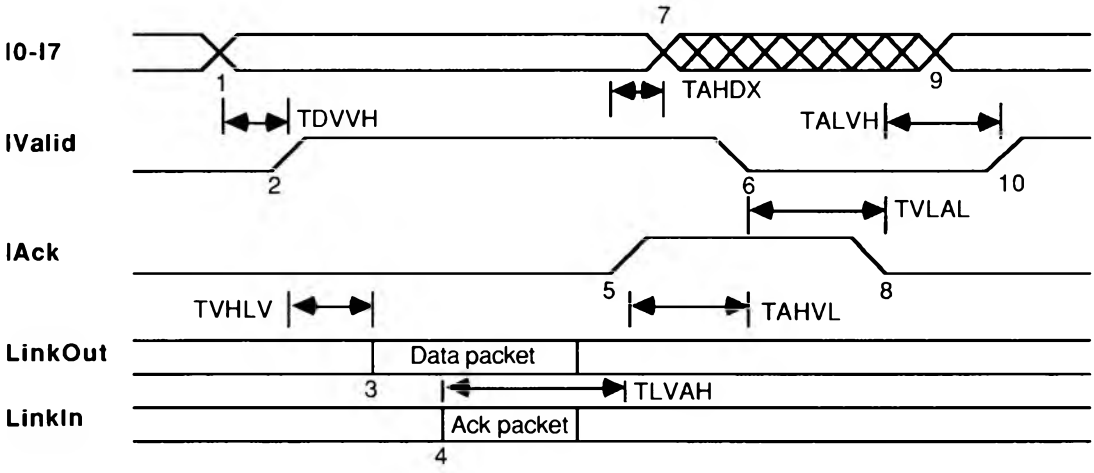
2 Requires a 0.1µF. capacitor between **VCC** and **GND**, close to the chip.

3 Peak to peak at all frequencies above 100 KHz.

4 Peak to peak at all frequencies above 30 MHz.

7.7 AC characteristics of parallel interface

7.7.1 Mode 1 Output to link



Event details

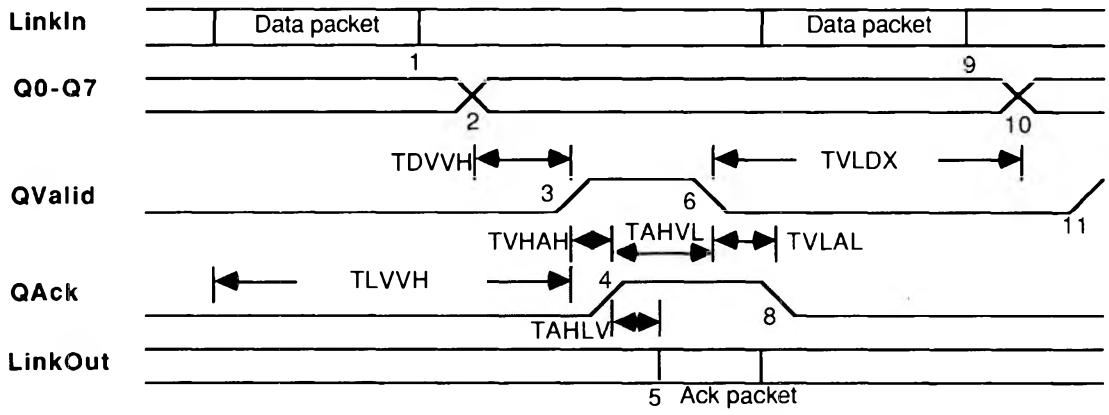
1 Data is presented on **I0-7**
2 The presence of valid data is indicated by raising **IValid**
3 The C011 commences transmitting the data on **LinkOut**
4 The C011 receives an acknowledge packet on **LinkIn**
5 The C011 acknowledges the data by taking **IAck** high
6 **IValid** is taken low
7 Data is removed from **I0-7**
8 The C011 completes the handshake by taking **IAck** low
9 Another data byte is presented on **I0-7**
10 The presence of valid data is indicated by raising **IValid**

Dependencies

Ensure that	1 precedes 2	by **TDVVH**
	5 precedes 6	by **TAHVL**
	5 precedes 7	by **TAHDX**
	8 precedes 10	by **TALVH**
The C011 ensures that	2 precedes 3	by **TVHLV**
	4 precedes 5	by **TLVAH**
	6 precedes 8	by **TVLAL**
The link protocol ensures that	3 precedes 4	

Parameter		Min	Max	Unit
TDVVH	Data setup before **IValid** high	5		ns
TVHLV	**IValid** high to byte on link			
	(no ack on link)	0.8	1.8	bit time
	(ack on link)	0.8	3.8	bit time
TLVAH	ack to **IAck** high		3	bit time
TAHVL	**IAck** high to **IValid** low	0		ns
TVLAL	**IValid** low to **IAck** low	1	4	bit time
TALVH	**IAck** low to **IValid** high	0		ns
TAHDX	Data hold from **IAck** high	0		ns

7.7.2 Mode 1 input from link



Event details

1 The C011 receives on **LinkIn** the data packet to be output
2 The C011 places the data on **Q0-7**
3 The C011 indicates the presence of valid data by raising **QValid**
4 The data is acknowledged by taking **QAck** high
5 The C011 transmits an acknowledge packet on **LinkOut**
6 The C011 takes **QValid** low
7 The C011 no longer holds the data outputs **Q0-7** valid
8 The handshake is completed by taking **QAck** low
9 The C011 receives on **LinkIn** another data packet
10 The C011 places the data on **Q0-7**
11 The C011 indicates the presence of valid data by raising **QValid**

Dependencies

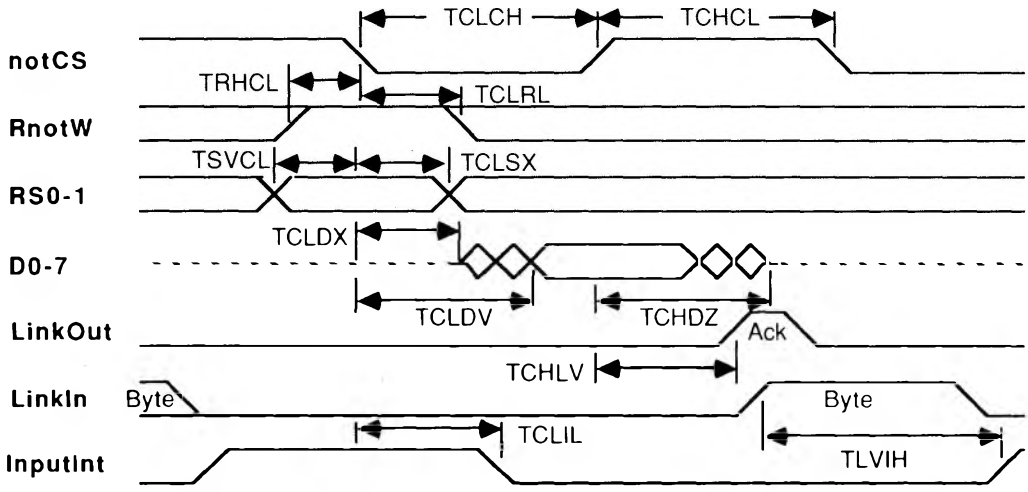
Ensure that	3 precedes 4	by **TVHAH**
	6 precedes 8	by **TVLAL**
The C011 ensures that	1 precedes 2	
	2 precedes 3	by **TDVVH**
	4 precedes 5	by **TAHLV**
	4 precedes 6	by **TAHVL**
	6 precedes 10	by **TVLDX**
	8 precedes 11	

Parameter		Min	Max	Unit
TDVVH	Data setup before **QValid** high	15		ns
TVLDX	Data hold after **QValid** low	11		bit time
TLVVH	Byte to **QValid** high	12		bit time
TVHAH	**QAck** setup time	0		ns
TVLAL	**QAck** hold time	0		ns
TAHLV	**QAck** high to Ack on link			
	(no byte on link)	0.8	1.8	bit time
	(byte on link)	0.8	12.8	bit time
TAHVL	**QAck** high to **QValid** low	1.8		bit time

7.7.3 Mode 2

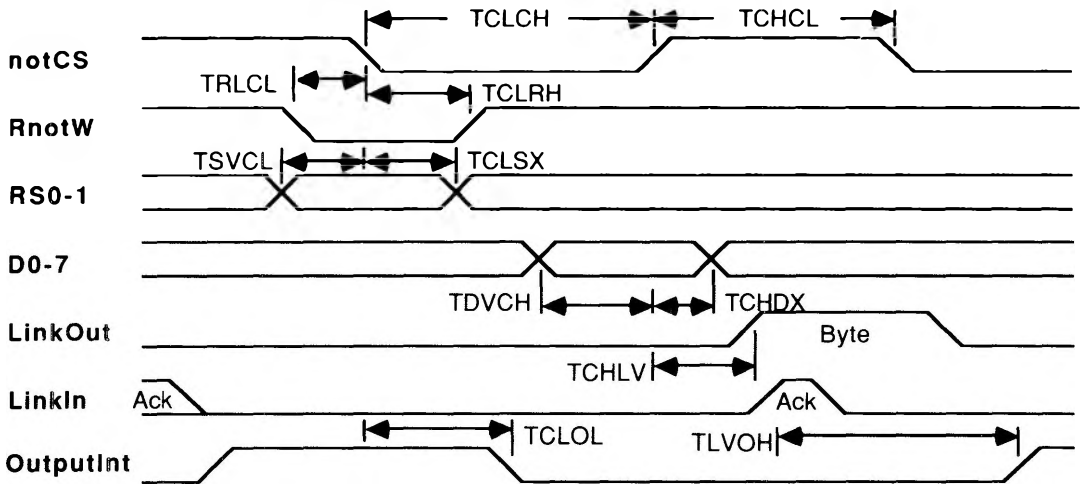
AC characteristics of parallel interface

Read cycle



Parameter		Min	Max	Unit
TCLCH	**notCS** low time	50		ns
TCHCL	time between cycles	50		ns
TRHCL	**RnotW** setup	5		ns
TCLRL	**RnotW** hold	5		ns
TSVCL	Register select setup	5		ns
TCLSX	Register select hold	5		ns
TCLDX	**notCS** to output active	5		ns
TCLDV	**notCS** to output valid		40	ns
TCLDZ	**notCS** high to output invalid	0	25	ns
TCHLV	**notCS** high to Ack on link			
	(no byte on link)	0.8	1.8	bit time
	(byte on link)	0.8	12.8	bit time
TCLIL	**notCS** low to **InputInt** low		25	ns
TLVIL	Byte to **InputInt** high		12	bit time

Write cycle



Parameter		Min	Max	Unit
TCLCH	**notCS** low time	50		ns
TCHCL	time between cycles	50		ns
TRLCL	**RnotW** setup	5		ns
TCLRH	**RnotW** hold	5		ns
TSVCL	Register select setup	5		ns
TCLSX	Register select hold	5		ns
TDVCH	Data setup	15		ns
TCHDX	Data hold	5		ns
TCHLV	**notCS** high to byte on link			
	(no Ack on link)	0.8	1.8	bit time
	(Ack on link)	0.8	3.8	bit time
TCLOL	**notCS** low to **OutputInt** low		25	ns
TLVOH	Ack to **OutputInt** high		3	bit time

8.1 Mode 1

CapMinus Negative end of decoupling capacitor.

ClockIn 5MHz input clock.
Input

GND Ground.

I0-I7 Byte-wide input data.
Input

IAck Link adaptor acknowledges that input data has been received.
Output

IValid Input data on **I0-I7** is valid.
Input

LinkIn INMOS serial link input.
Input

LinkOut INMOS serial link output.
Output

Q0-Q7 Byte-wide output data.
Output

QAck Acknowledge to link adaptor that data output from the link adaptor has been received.
Input

QValid Output data on **Q0-Q7** is valid.
Output

Reset Reset link adaptor.
Input

SeparateIQ This pin selects operating modes 1 or 2. In addition to this, it controls the link speed in mode 1 operation. If wired to **VCC**, mode 1 is selected with a link speed of 10 Mbits/sec. If wired to **ClockIn**, mode 1 is selected but with a link speed of 20 Mbits/sec. Wiring to **GND** selects mode 2.
Input

VCC Star point for +5 volt supply input and positive end of decoupling capacitor.

8.2 Mode 2

CapMinus Negative end of decoupling capacitor.

ClockIn 5MHz input clock.
Input

D0-D7 Bi-directional databus.
Input/Output

DoNotWire Signal reserved for INMOS use. Must be left unconnected.

GND Ground.

HoldToGND Signal reserved for INMOS use. Must be held to **GND**. Failure to do so may cause damage to the device.
Input

InputInt Input interrupt.
Output

LinkIn INMOS serial link input.
Input

LinkOut INMOS serial link output.
Output

LinkSpeed Determines the speed of the links. If wired to **GND** link speed is 10 Mbits/sec, if wired to **VCC** speed is 20 Mbits/sec.
Input

notCS Chip select input.
Input

OutputIn Output interrupt.
Output

Reset Reset link adaptor.
Input

RnotW Read or write register.
Input

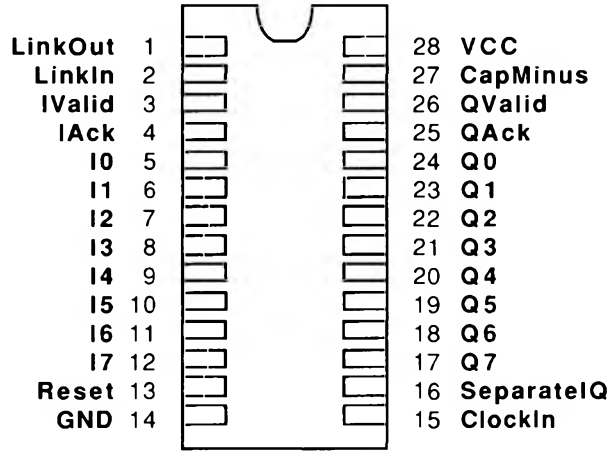
RS0-RS1 Register select lines; used in conjunction with **notCS** and **RnotW** to control the selection of the internal register to be read or written.
Input

SeparateIQ This must be wired to **GND** to select mode 2.
Input

VCC Star point for +5 volt supply input and positive end of decoupling capacitor.

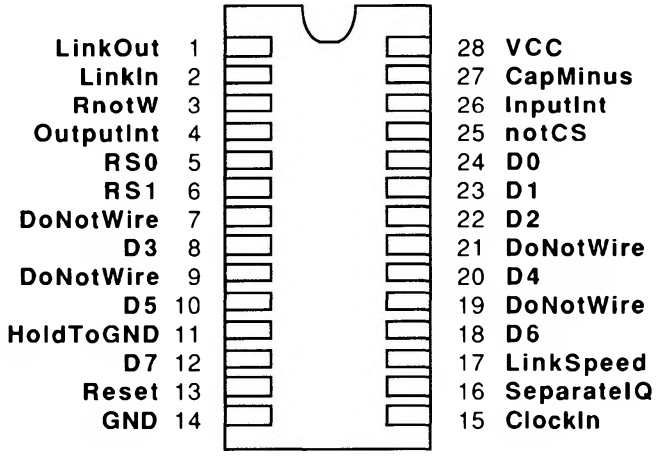
The C011 is available in a 28 pin plastic package.

Package mode 1



C011 Mode 1 pin out

Package mode 2



C011 Mode 2 pin out