Data Sheet For 80188EB Core

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
0.1	29th Oct 2007	Initial Draft Version	FA, MJ
0.2	29th Nov 2007	Logic symbol and Resource utilization included, IOPU added in Block diagram	FA
0.3	14th Dec 2007	Timing Diagram and Instruction set included.	AS
0.4	29th Dec 2007	I/O Signals Updated.	AS
REL 1.0	19th Nov'11	Updated as per the latest formatting	Arun
REL 1.1	16th Aug'12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

The iW-80188EB is a powerful 16-bit microprocessor core, executes instruction list compatible with 80188EB microprocessor. The design along with multiple peripherals can be fit into single FPGA.

1.2 Features

The following are the main features of the 80188EB Core:

- iW-80188EB CPU Core
  - Multiplexed 20-bit address and 8-bit data bus
  - 1M-byte memory space divided into 4 segments
  - 64K-byte IO space
  - Non Maskable Interrupt support
  - Arithmetic-Logic Unit
    - 8,16,32-bit arithmetic operations
    - 8,16-bit logical operations
    - Boolean manipulations
    - 16 x 16 bit multiplication (signed or unsigned)
    - 32/16-bit division (signed or unsigned)
- CPU On-Chip Peripherals
  - Programmable Timer / Counter Unit
    - Three programmable independent 16-bit timers
    - TOUT0 to TOUT1 pin outputs
    - TIN0 & TIN1 used either as clock or control signals
    - Timer-2 can be used to clock other two timers
    - Internal / external input clock selectable
  - Serial Communications Unit
    - RS-232-C protocol support (on-chip CTS_N, SINT_N pins)
    - Both synchronous and asynchronous modes are supported
    - Two independent identical channels
    - Full duplex operation in asynchronous mode
    - Half-duplex operation in synchronous mode

- Programmable seven, eight or nine data bits in asynchronous mode
- Independent baud rate generator
- Double-buffered transmit and receive
- Clear-to-Send feature for transmission
- Break character transmission and detection
- Programmable even, odd or no parity
- Detects both framing and overrun errors
- Supports interrupt on transmit and receive

- Interrupt Controller Unit
  - Edge trigger / level trigger selectable
  - Individually maskable interrupt requests
  - Programmable interrupt request priority orders
  - Supports Cascading (Only INTP0 and INTP1) and polling mode
  - 5 external interrupt request inputs (INTP0 to INTP4)
  - 2 internal interrupt input pins (SCU and TCU)
- Chip Select Unit
  - Ten programmable chip-select outputs
  - Programmable start and stop addresses
  - Memory or I/O bus cycle decoder
  - Programmable wait-state generator
  - Provision to disable a chip-select
  - Provision to override bus ready
- Clock Generator
- Two 8-bit multiplexed Input/output Ports

1.3 Features Not Supported

- Oscillators internal to the FPGA, so crystals cannot be directly connected to the FPGA
- ONCE mode
- Power down modes
- Refresh Control Unit
- WAIT instruction is not supported

1.4 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
CPU	Central Processing Unit
I/O	Input/ Output

2 80188EB Core

2.1 Block Diagram

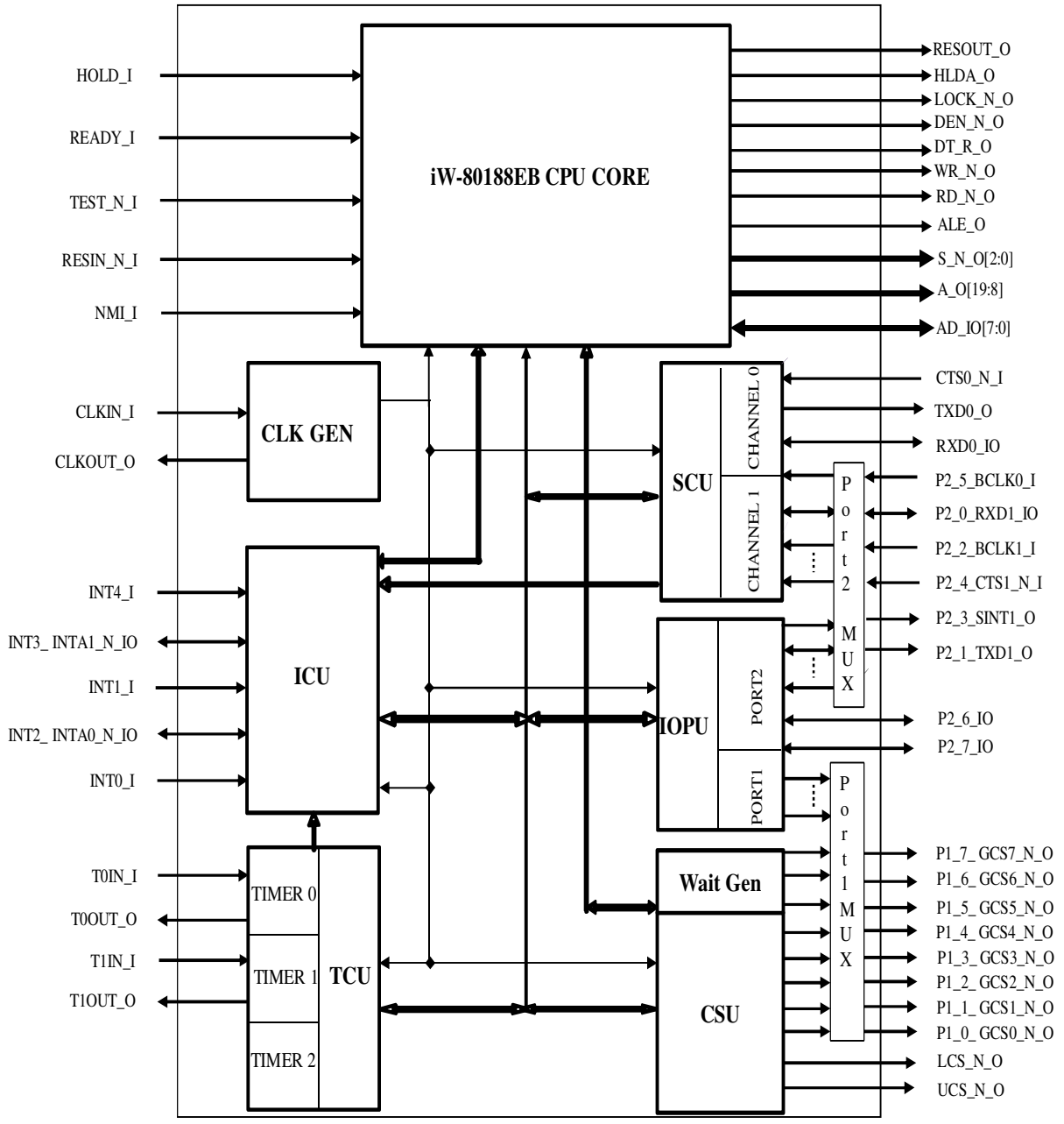

Figure 1: 80188EB Core Block Diagram

2.2 Description

The main blocks in 80188EB Core:

- **Central Processing Unit (CPU)**: This module executes instructions, which include fetching, decoding instructions and generating appropriate requests to the Bus Interface Unit.
- **Timer / Counter Unit (TCU):** This module provides three programmable 16-bit timer/counters. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally.
- **Serial Communications Unit (SCU):** This module supports both synchronous and asynchronous communications modes and contains two independent channels. Each channel has its own baud rate generator that is independent of the TCU, and can be internally or externally clocked at up to one half of the operating frequency.
- **Interrupt Control Unit (ICU):** This module serves to merge two internal and five external interrupt requests on a priority basis, for individual service by the CPU. The Interrupt Control Unit can independently mask each interrupt source or the CPU can globally mask all interrupts.
- **Chip-Select Unit (CSU):** This module integrates logic, which provides up to ten programmable chip selects to access both memories and peripherals. Besides selecting a specific device, each chip-select can be used to control the number of wait states inserted into the bus cycle
- **I/O Port Unit (IOPU):** This module supports two 8-bit channels of input, output, or input/output operation
- **Clock Generator:** This module generates both internal and external clock

2.3 I/O Signal Description

Table 2: 80188EB Core IO Signals

Signal	I/O	Width	Description
RESIN_N_I	I	1	An active low signal causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active.
RESOUT_O	O	1	Indicates the processor is currently in the reset state. RESOUT will remain active as long as RESIN_N remains active.
CLKIN_I	I	1	External clock input operating at two times the processor operating frequency.
CLKOUT_O	O	1	Processor Clcok output. It is half of Clock input (CLKIN_I).
AD_IO[7:0]	IO	8	Provide a multiplexed address and Data bus. During the address phase of the bus cycle, address bits AD [7:0] are presented on the bus and can be latched using ALE. 8-bit data information is transferred during the data phase of the bus cycle.
A_O[19:8]	O	12	Provide multiplexed address during the address phase of the bus cycle. A [19:16] are presented on these pins and can be latched using ALE. These pins are driven to logic 0 during the data phase of the bus cycle. A [15:8] provides valid address information for the entire bus cycle.
ALE_O	O	1	Address Latch Enable, an active high signal used to strobe address information into a transparent type latch during the address phase of the bus cycle.

<table>
<tr><th>Signal</th><th>I/O</th><th>Width</th><th>Description</th></tr>
<tr><td>S_N_O[2:0]</td><td>O</td><td>3</td><td>Bus cycle Status are encoded on these pins to provide bus transaction information. S[2:0] are
<table>
<tr><th>S2</th><th>S1</th><th>S0</th><th>BUS CYCLE</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Processor HALT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Queue Instruction Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive(no bus activity)</td></tr>
</table></td></tr>
<tr><td>READY_I</td><td>I</td><td>1</td><td>Active high Ready input to signal the completion of a bus cycle. It must be active to terminate any bus cycle, unless it is ignored by correctly programming the Chip-Select Unit.</td></tr>
<tr><td>RD_N_O</td><td>O</td><td>1</td><td>Active low Read output signals that the accessed memory or I/O device must drive data information onto the data bus.</td></tr>
<tr><td>WR_N_O</td><td>O</td><td>1</td><td>Active low Write output signals that data available on the data bus are to be written into the accessed memory or I/O device.</td></tr>
<tr><td>DEN_N_O</td><td>O</td><td>1</td><td>Active low Data enable output to control the enable of bi-directional transceivers in a buffered system. DEN is active only when data is to be transferred on the bus.</td></tr>
<tr><td>DT_R_O</td><td>O</td><td>O</td><td>Data Transmit/Receive output controls the direction of a bi-directional buffer in a buffered system.</td></tr>
<tr><td>HOLD_I</td><td>I</td><td>1</td><td>HOLD request input to signal that an external bus master wishes to gain control of the local bus.</td></tr>
</table>

Signal	I/O	Width	Description
HLDA_O	O	1	The processor generates HLDA in response to a HOLD indicating that bus is granted. It indicates that the processor has relinquished control of the local bus.
LOCK_N_O	O	1	The processor will not service other bus requests (such as HOLD) while LOCK is active.
NMI_I	I	1	Non-Maskable Interrupt input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally.
P2_7_IO, P2_6_IO	IO	1	Bi-directional pins.
CTS0_N_I, P2_4_CTS1_N_I	I	1	Active low Clear-To-Send input is used to prevent the transmission of serial data on their respective TXD signal pin. CTS is multiplexed with an input only port function.
TXD0_O, P2_1_TXD1_O	O	1	Transmit Data output provides serial data information. TXD1 is multiplexed with an output only Port function.
RXD0_IO , P2_0_RXD1_IO	IO	1	Receive Data input accepts serial data information. RXD1 is multiplexed with an input only Port function. During synchronous serial communications, RXD is bi-directional and will become an output for transmission or data
P2_5_BCLK0_I, P2_2_BCLK1_I	I	1	Baud Clock input can be used as an alternate clock source for each of the integrated serial channels. BCLKx is multiplexed with an input only Port function, and cannot exceed a clock rate greater than one-half the operating frequency of the processor.
P2_3_SINT1_O	O	1	Serial interrupt output will go active to indicate serial channel 1 requires service. SINT1 is multiplexed with an output only Port function.
INT0_I, INT1_I, INT4_I	I	1	Maskable interrupt input will cause a vector to a specific type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with INTA0 and INTA1 to interface with an external slave controller.

Signal	I/O	Width	Description
INT2_INTA0_N_IO, INT3_INTA1_N_IO	IO	1	These pins provide a multiplexed function. As inputs, they provide a maskable interrupt that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an Interrupt acknowledge handshake signal to allow interrupt expansion.
T0OUT0_O, T1OUT1_O	O	1	Timer output pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN0_I,T1IN1_I	I	1	Timer input is used either as clock or control signals, depending on the timer mode selected.
UCS_N_O	O	1	Upper Chip Select will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user.
LCS_N_O	O	1	Lower Chip Select will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user.
P1_0_GCS0_N_O to P1_7_GCS7_N_O	O	1	These pins provide a multiplexed function. If enabled, each pin can provide a Generic Chip Select output, which will go active whenever, the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general-purpose output Port. As an output port pin, the value of the pin can be read internally.

3 Timing Waveforms

3.1 CPU Write Cycle

3.1.1 CPU Write Cycle (RDY = 0 and Without wait state)

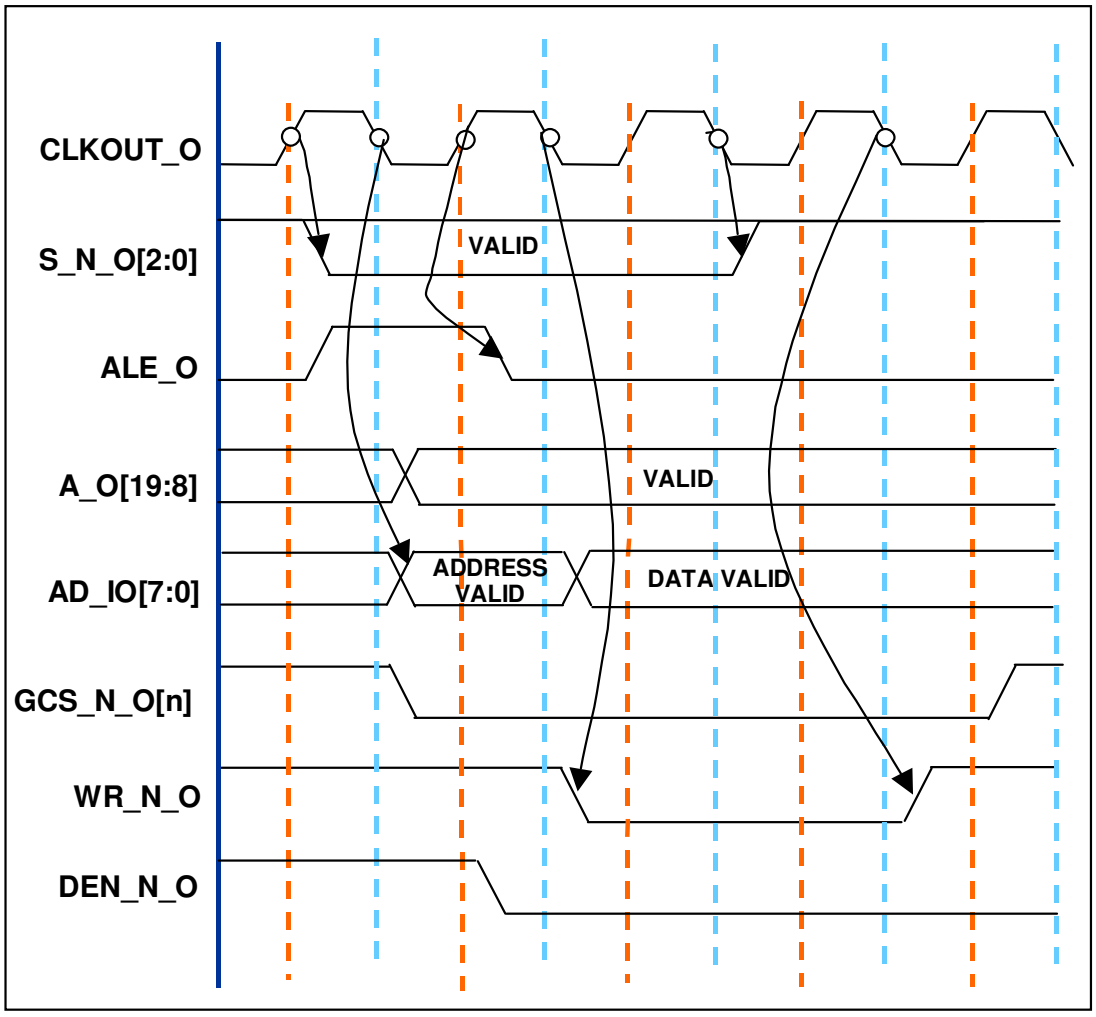

Figure 2: CPU Write Cycle (RDY = 0 and Without wait state)

3.1.2 CPU Write Cycle (RDY = 0 and With wait state)

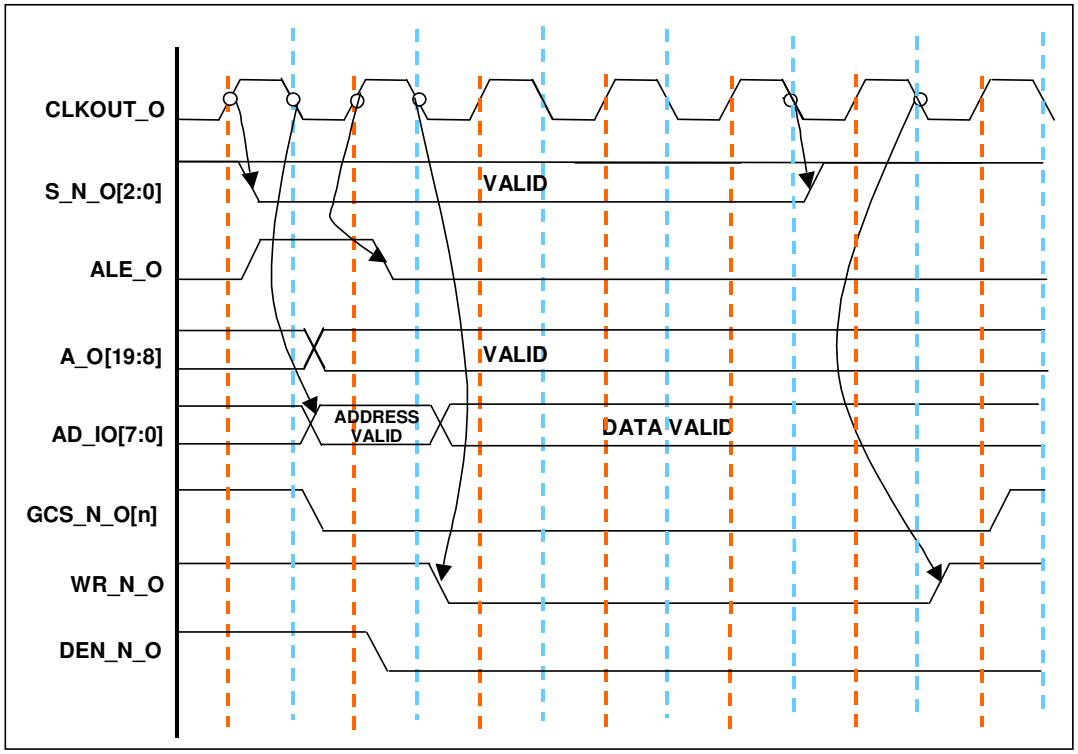

Figure 3: CPU Write Cycle (RDY = 0 and With wait state)

3.1.3 CPU Write Cycle (RDY = 1)

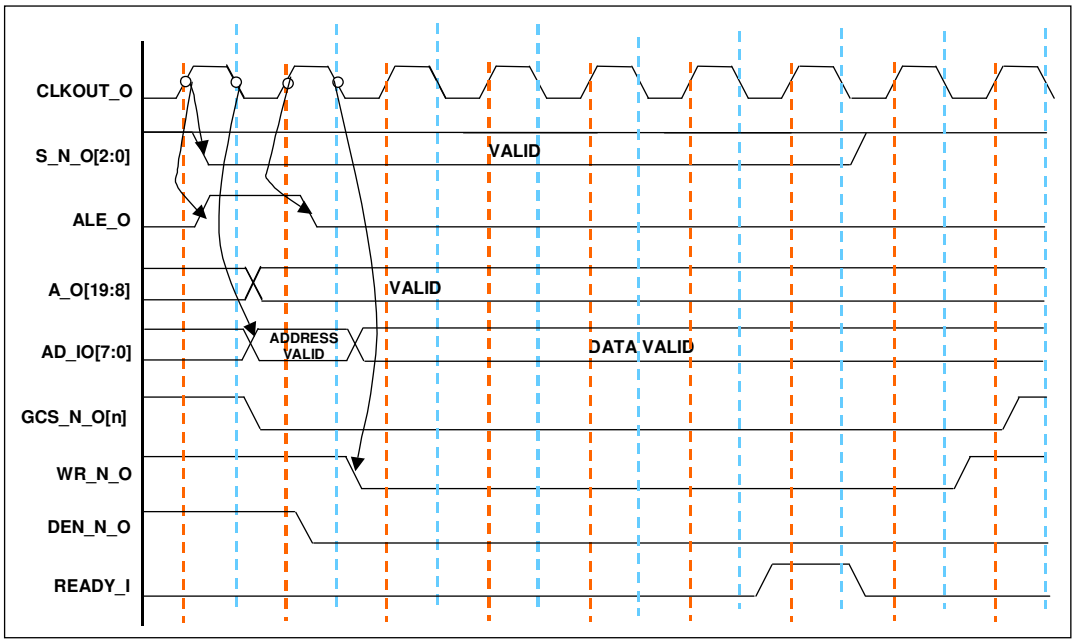

Figure 4: CPU Write Cycle (RDY = 1)

3.2 CPU Read Cycle

3.2.1 CPU Read Cycle

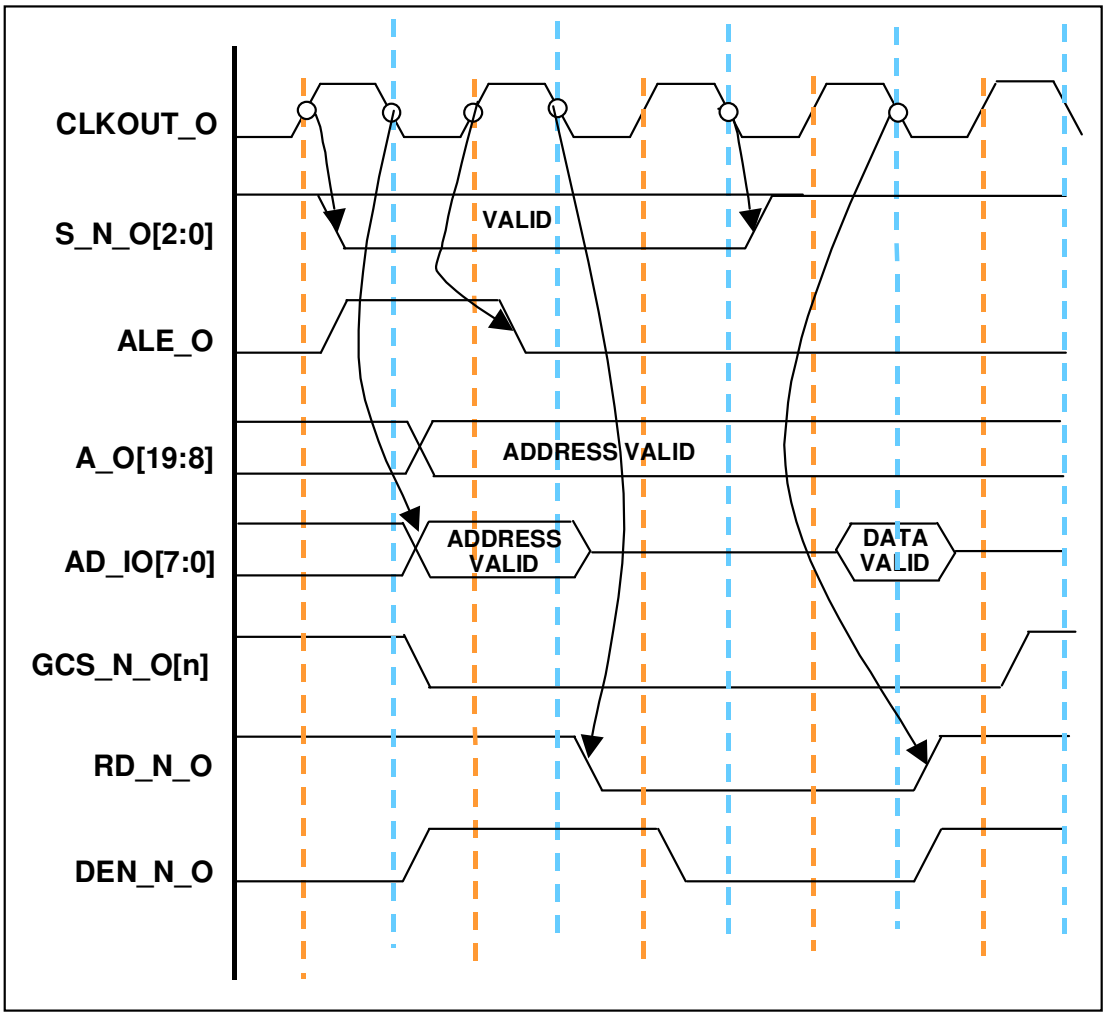

Figure 5: CPU Read Cycle

3.3 Interrupt Acknowledge Cycle

3.3.1 Interrupt Acknowledge Cycle

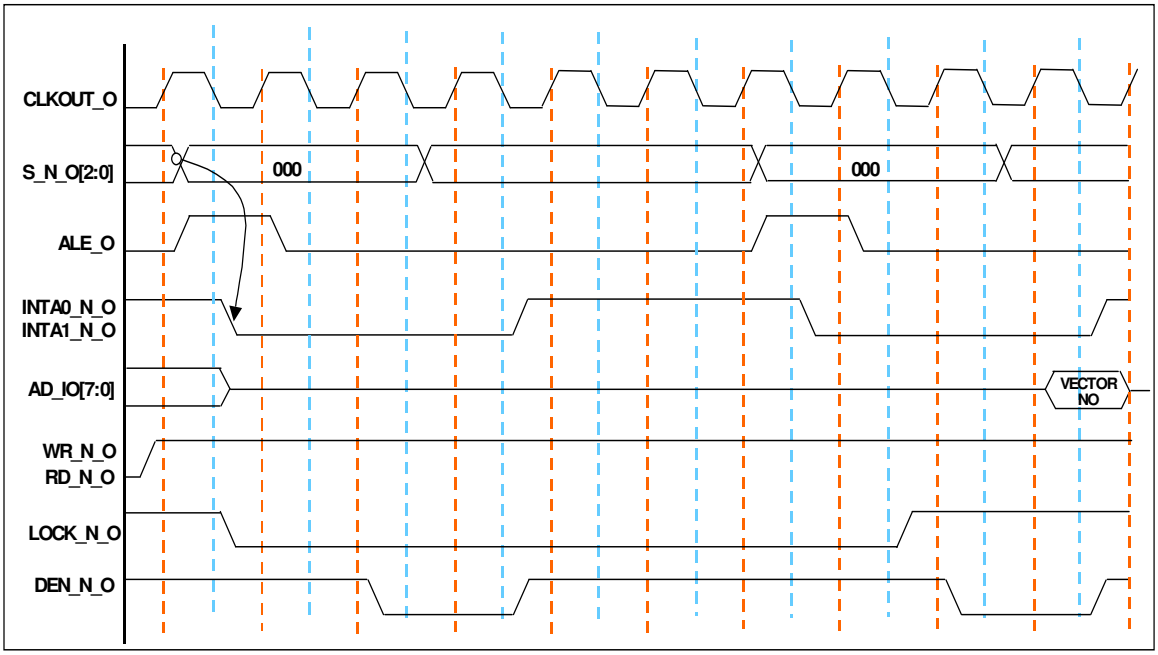

Figure 6: Interrupt Acknowledge Cycle

3.4 HOLD/HACK Cycle

3.4.1 HOLD/HACK Cycle

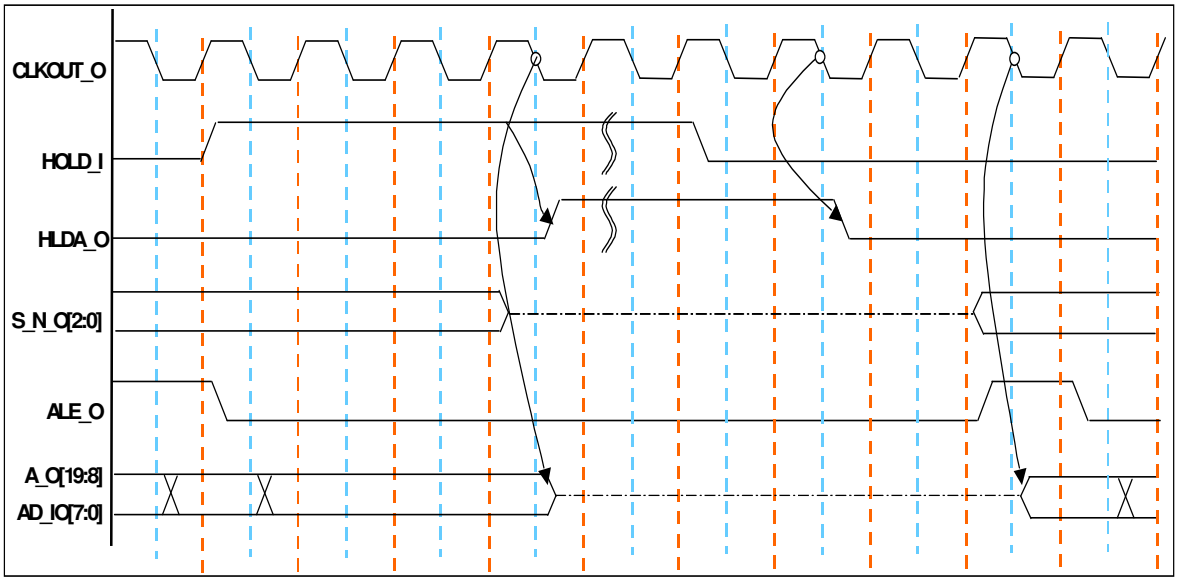

Figure 7: HOLD/HACK Cycle

3.5 HALT Cycle

3.5.1 HALT Cycle

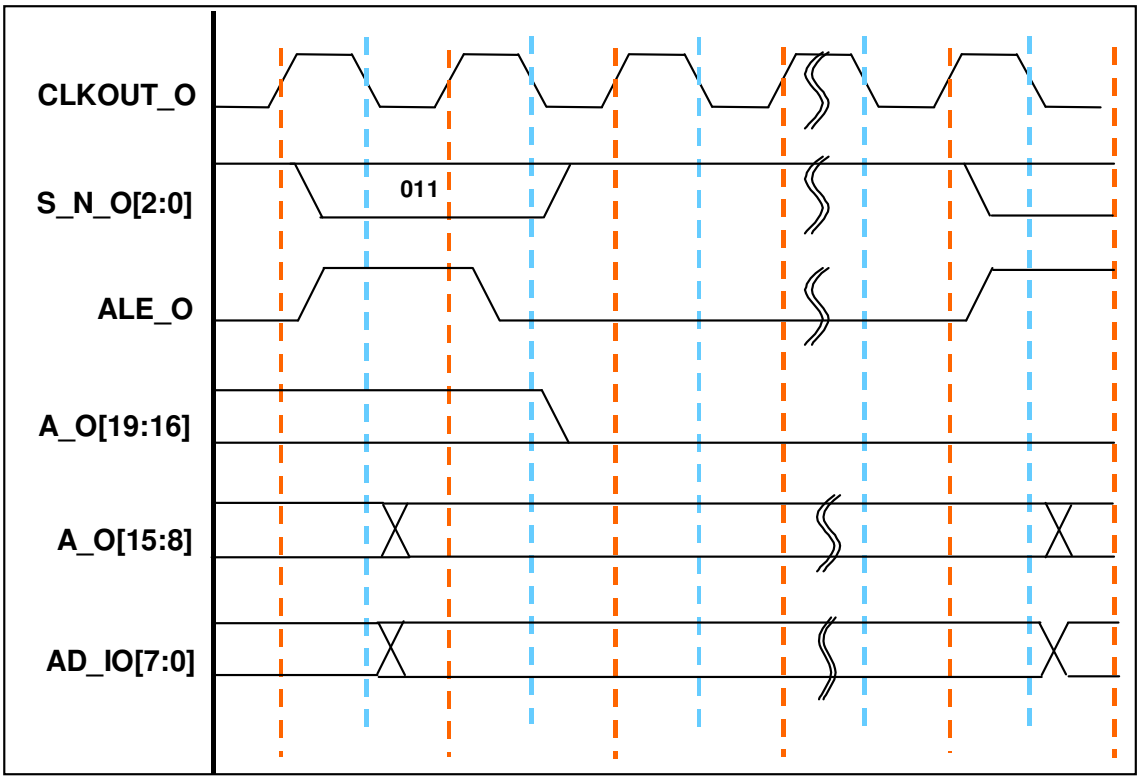

Figure 8: HALT Cycle