2-PHASE DRUM MOTOR DRIVER

The KA3084D is a monolithic integrated circuit, and it is suitable for drum motor driver of VCR system.

FEATURES

- •Drives the BLDC motor using 2 hall sensors.
- •2-phase, full-wave drive method
- •Built-in thermal shutdown (TSD) circuit
- •Controls the motor speed through voltage
- •Built-in bandgap circuit
- •Built-in Frequency Generator (FG) & Phase Generator (PG) Amplifier & Comparator.

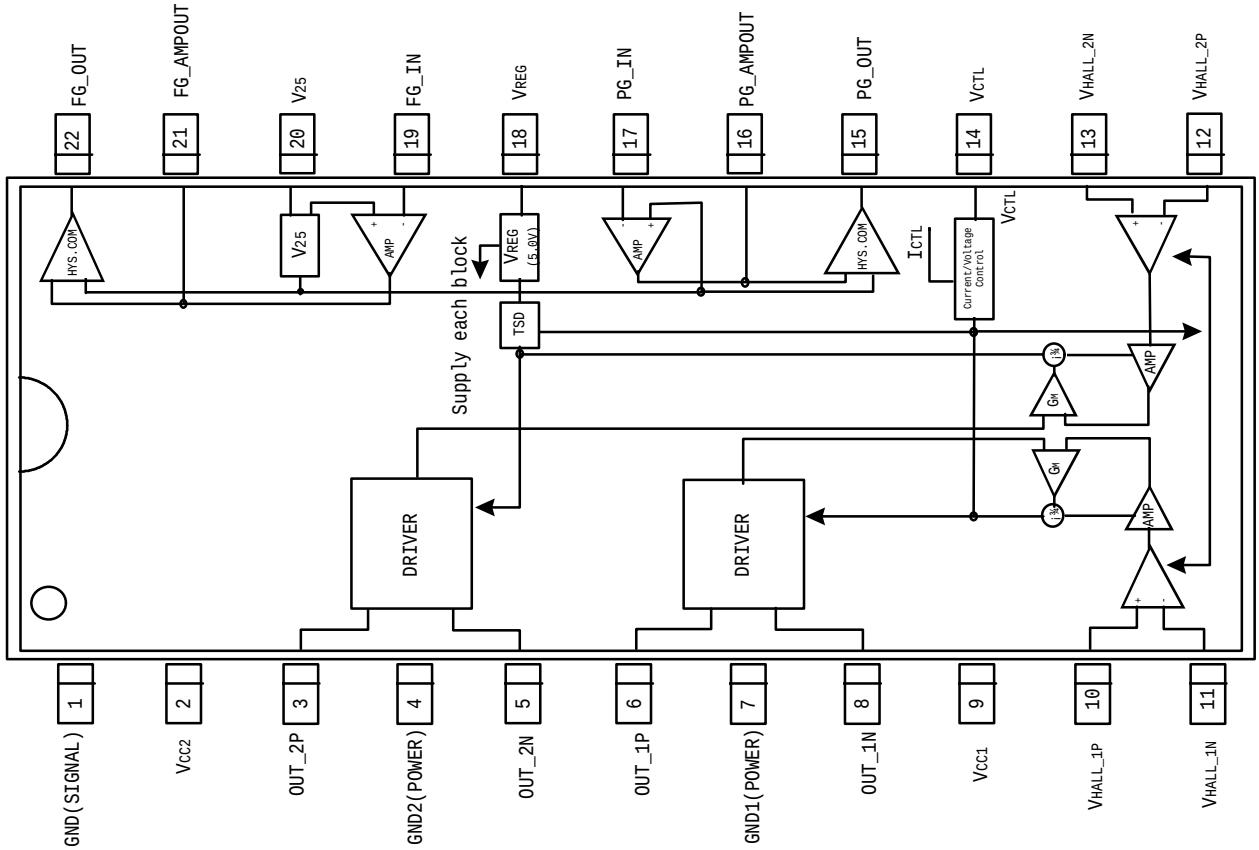
ORDERING INFORMATION

Device	Package	Operating Temperature
KA3084D	22-SOP-300	- 25 ¡ -+ 75¡ É

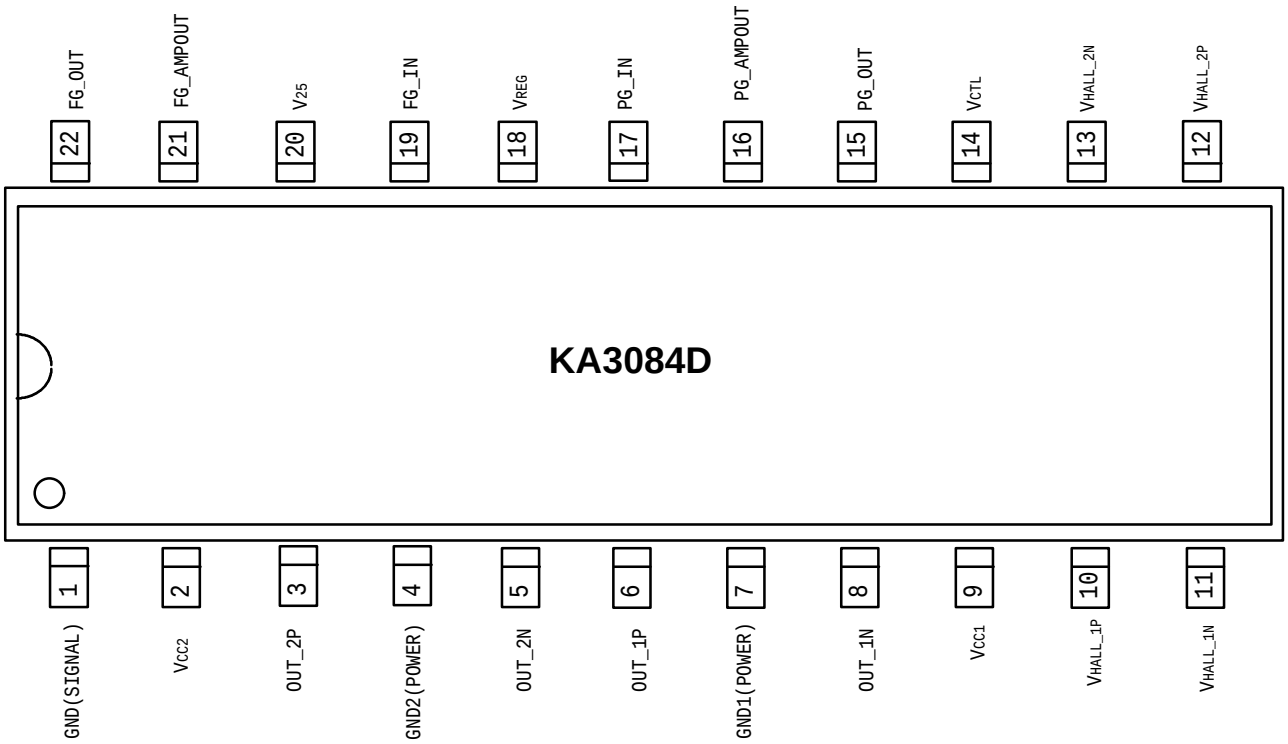
TARGET APPLICATIONS

•VCR drum motors

BLOCK DIAGRAM



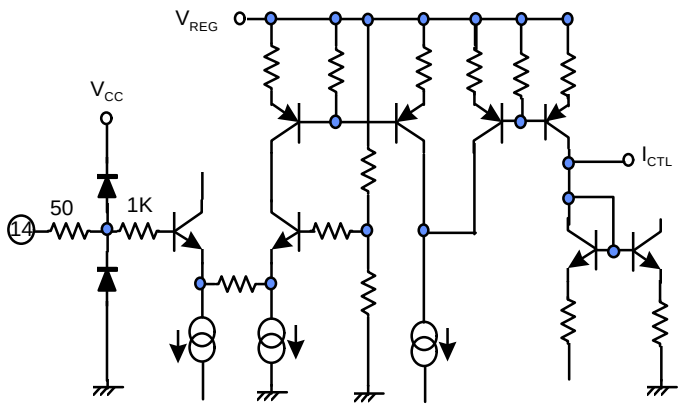
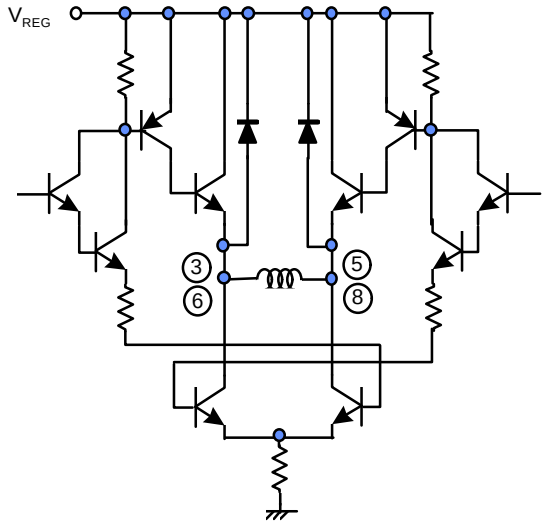
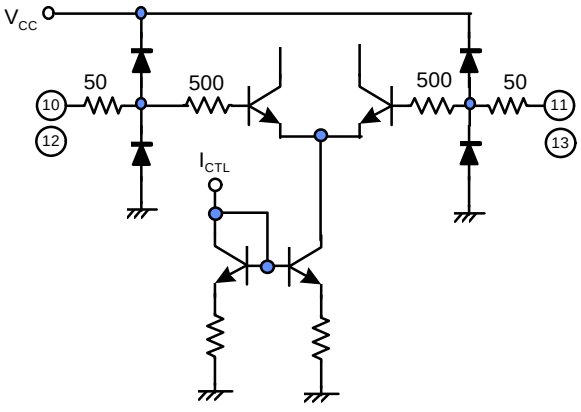
PIN CONFIGURATION

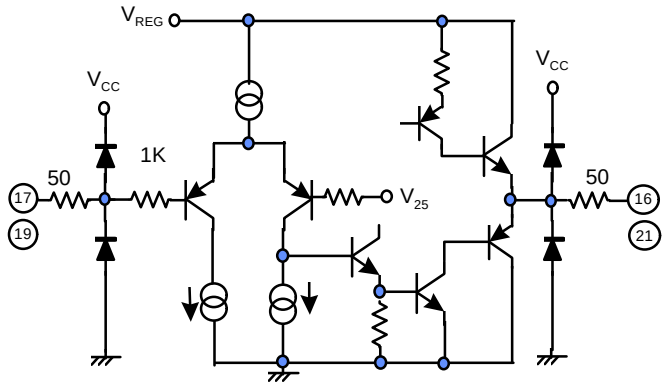
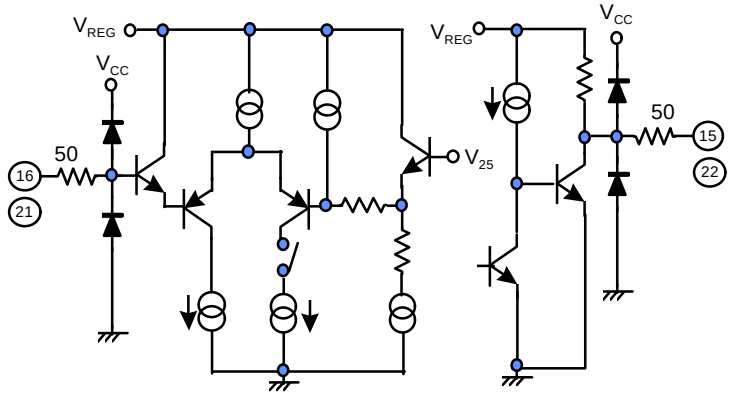


PIN DESCRIPTION

Pin no.	Symbol	I/O	Description
1	GND(Signal)	--	Ground(Signal)
2	V_{CC2}	--	Power Supply 2
3	OUT_2P	O	Output Drive2(P)
4	GND2(Power)	--	Power Ground 2
5	OUT_2N	O	Output Drive 2(N)
6	OUT_1P	O	Output Drive 1(P)
7	GND1(Power)	--	Power Ground 1
8	OUT_1N	O	Output Drive 1(N)
9	V_{CC1}	--	Power Supply 1
10	V_{HALL_1P}	I	HALL Signal Input 1P
11	V_{HALL_1N}	I	HALL Signal Input 1N
12	V_{HALL_2P}	I	HALL Signal Input 2P
13	V_{HALL_2N}	I	HALL Signal Input 2N
14	V_{CTL}	I	Voltage Ccontrol(Motor Speed Control)
15	PG_OUT	O	Phase Generator Output
16	PG_AMPOUT	O	Phase Generator Amp. Output
17	PG_IN	I	Phase Generator Input
18	V_{REG}	O	Regurated Voltage
19	FG_IN	I	Frequency Generator Input
20	V_{25}	I/O	Reference Voltage
21	FG_AMPOUT	O	Frequency Generator Amp. Output
22	FG_OUT	O	Frequency Generator Output

INTERNAL CIRCUIT

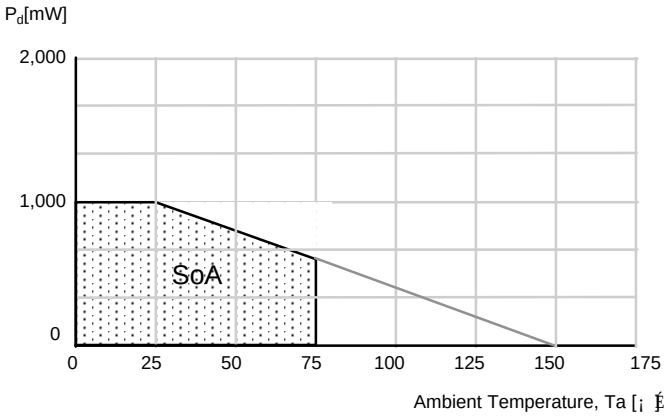
DESCRIPTION	PIN NO.	INTERNAL CIRCUIT
VCTL	14	
Motor Output	3,5,6,8	
HALL Input	10,11,12,13	

DESCRIPTION	PIN NO.	INTERNAL CIRCUIT
PG,FG Amplifier	16,17, 19,21	
PG,FG hysteresis Amplifier	15,16, 21,22	

ABSOLUTE MAXIMUM RATINGS (Ta = 25¡ É)

Characteristics	Symbol	Value	Unit	Remark
Supply Voltage	V_{CCmax}	18	V	--
Output Current	I_{Omax}	*1 1.0	A	--
V_{REG} Output Current	I_{REGmax}	30	mA	--
Power Dissipation	P_d	*2 1	W	No Heat Sink
Operating Temperature	T_{OPR}	-25 ~ +75	¡ É	--
Storage Temperature	T_{STG}	-45 ~ +125	¡ É	--

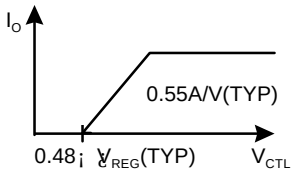
*1 Duty 1/100, pulse width 500§ Á
*2 1)When mounted on glass epoxy PCB (76.2¡ ¿114¡ ¿1.57mm)
2)Power dissipation reduces 8.0mW/¡ Éfor using above Ta=25¡ É(wihout heat-sink)
3)Do not exceed Pd and SOA



RECOMMENED OPERATING CONDITIONS

Characteristics	Symbol	Value			Unit
		Min.	Typ.	Max.	
Operating Supply Voltage	V_{CC}	8	12	16	V

ELECTRICAL CHARACTERISTICS
(Ta=25¡ ÉV$_{CC}$=12V , unless otherwise specified,)

Characteristics	Symbol	Test Condition	Spec			Unit
			Min.	Typ.	Max.	
FULL CIRCUIT						
Quiescent Current	I_Q	V_{CC}=12V	--	8.5	13	mA
VOLTAGE REGULATOR						
Regulated Voltage	V_{REG}	V_{CC}=12V	4.6	5.0	5.4	V
Regulated Voltage	V_{REG}	V_{CC}=12V, I_{REG}=-20mA	--	8.5	13	mA
HALL INPUT						
*Hall Minium Input Level	V_{INH}	--	50	--	--	mV_{P-P}
Hall Bias Current	I_{BH}	V_{CTL}=2.0V, HALL=2.5V	--	0.25	2.0	uA
OUTPUT DRIVE						
Output Saturation Voltage(Upper)	V_{S_U}	V_{CTL}=4.5V	--	1.3	2.0	V
Output Saturation Voltage(Lower)	V_{S_L}	V_{CTL}=4.5V	--	2.0	2.0	V
Output Current A	$I_{OUT\ A}$	V_{HALL_1P}=2.6V, V_{HALL_1N}=2.4V, V_{CTL} =3.5V	500	700	900	mA
Output Current B	$I_{OUT\ B}$	V_{HALL_2P}=2.6V, V_{HALL_2N}=2.4V, V_{CTL} =2.5V	500	700	900	mA
VOLTAGE CONTROL						
* V_{CTL} Reference Voltage	V_{25}	0.48 ¡ ¿V_{REG}	2.1	2.3	2.5	V
* V_{CTL} Input Range	V_{CTL}	--	0	--	V_{REG}	V
V_{CTL} Offset Range	V_{OFF}	V_{CTL} = 0 ~ V_{CTL}	-150	0	+150	mV
V_{CTL} Input Bias Current	I_{VCTL}	V_{CTL} = 2.5V	--	1.0	6.0	uA
Voltage Control Gain	GM	VCTL = 2.8V, 3.3V ¥ ÄO/¥ ÄVCTL V_{HALL_1P}=2.6V,V_{HALL_1N}=2.4V  	0.38	0.55	0.64	A/V

Characteristics	Symbol	Condition	Spec			Unit
			Min.	Typ.	Max.	
FULL CIRCUIT						
*Shutdown Temperature	TSD	--	130	160	--	¡ É
*Temperature Hysteresis	T_{HYS}	--	--	30	--	¡ É
FG/PG AMP						
Input Offset Voltage	V_{OFS}	--	--	0	¡ 8	mV
Input Current	I_{AMP_IN}	V_{IN}=2.5V	--	0.2	2.0	uA
*Open Loop Gain	G_A	V_{CC}=12V, Signal=500Hz	65	70	--	dB
Output High Volatge	V_{OHA}	V_{IN}=2.0V	V_{REG} -1.48	V_{REG} -0.74	--	V
Output Low Volatge	V_{OLA}	V_{IN}=2.7V	--	0.85	1.45	V
COMPARATOR (Hysteresis)						
Hysteresis Level	V_{HYS}	--	¡ 130	¡ 165	¡ 200	mV
Output Low Volatge	V_{OLHYS}	V_{IN}=2.0V	--	0.12	0.32	V
Output Pull-up Resistance	V_{BHYS}	--	7.0	10	13	§ Ú

NOTE: The mark (*) in the chart means items calculated and approved in design not the items proven by actual test result.

APPLICATION INFORMATION

1. A DIAGRAM SUMMARIZING THE ENTIRE SYSTEM

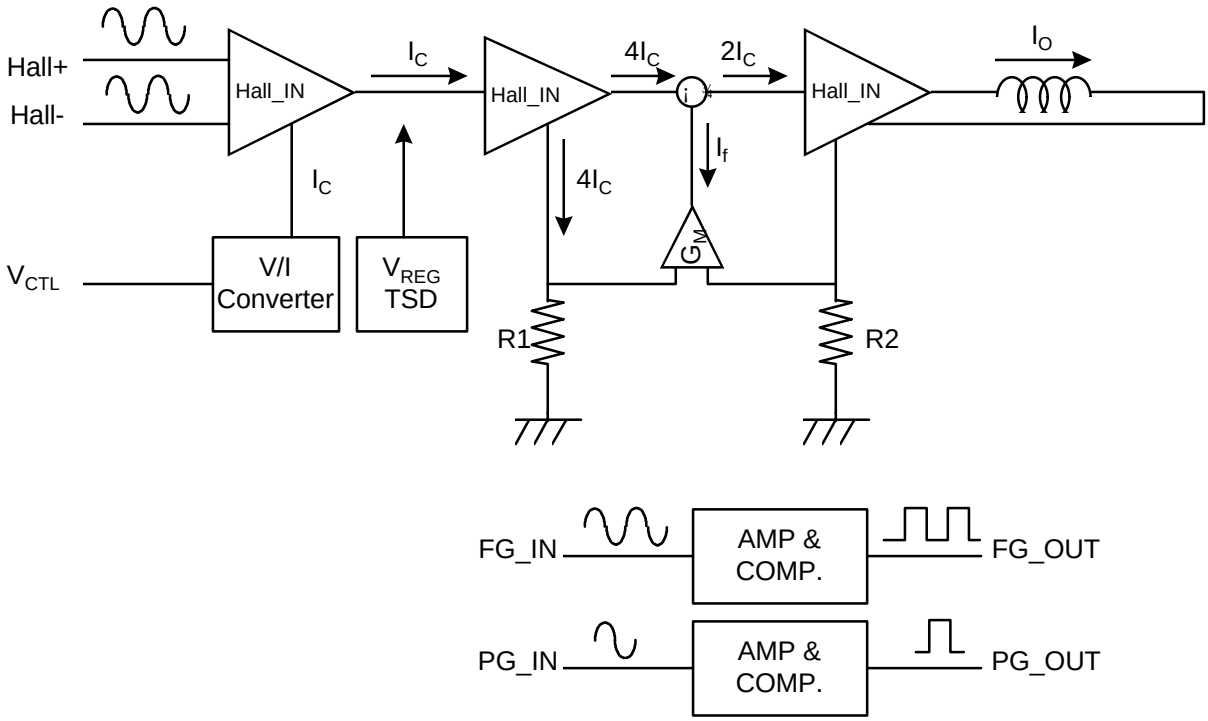


Figure 1.

Figure 1 is a diagram of the KA3084D concept. Essentially, it shows that it turns on or off depending on the signal of the hall sensor used for sensing the rotor position of motor.

The AMP, G_M (Feedback) and Output blocks are circuits used to determine current gain of KA3084D.

Furthermore, Hall_IN represents the hall signal switch.

It supplies stable bias to each V_{REG} block. The TSD block is a thermal shutdown circuit that protects the IC during an high temperature inside the IC.

Moreover, FG. and PG. blocks output individual signals generated in the motor using the amplifier and comparator.

These signals transmit motor speed and position data to controller of external servo etc. for their control.

2. CURRENT CONTROL

Figure 2 simplifies Figure 1 even more.

The supplied Io current drives the motor and the Ic current controls the motor speed.

At this time, I_{CTL} controls the magnitude of Io. Moreover, A_T is the system's entire current gain.

Figure 3 is a graph of I_{CTL} vs. Io.

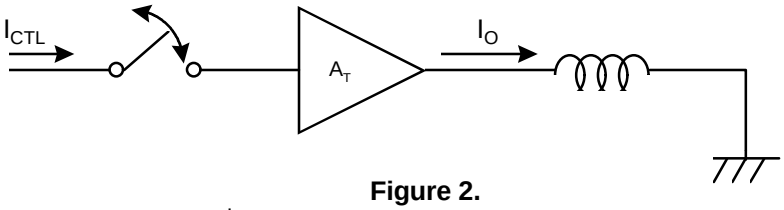


Figure 2.

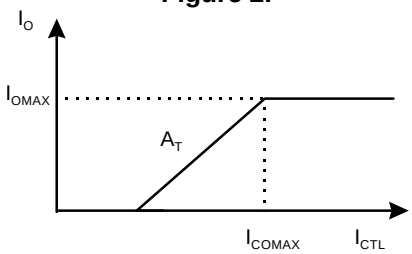


Figure 3.

3. VOLTAGE CONTROL

Even though KA3084D command uses Ic to control the magnitude of Io, it can also use voltage. KA3084D mainly uses voltage control and optionally uses current control.

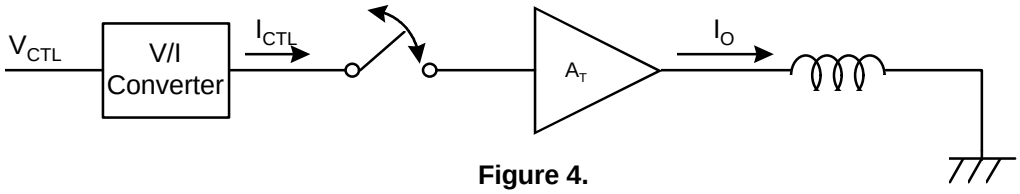


Figure 4.

Figure 4 shows the principle of the voltage control.
The V_{CTL} is the motor speed control voltage, and the I_{CTL} is V_{CTL} that was converted to current through the V/I Converter.
Figure 5 shows the graph of V_{CTL} vs. Io.

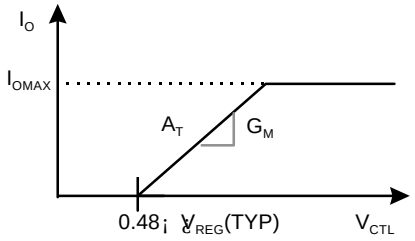
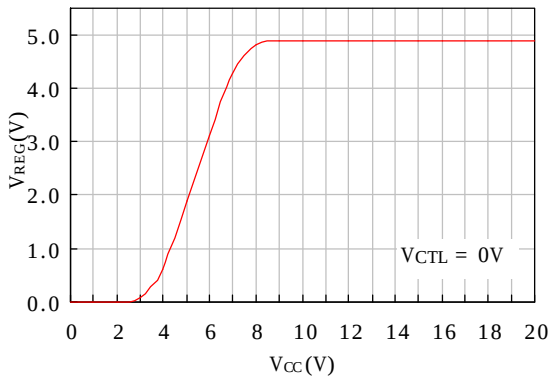


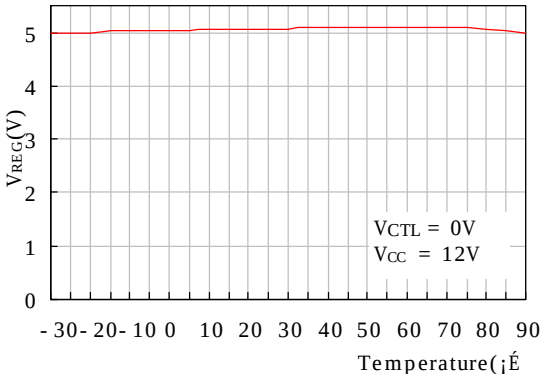
Figure 5.

CHARACTERISTIC GRAPHS

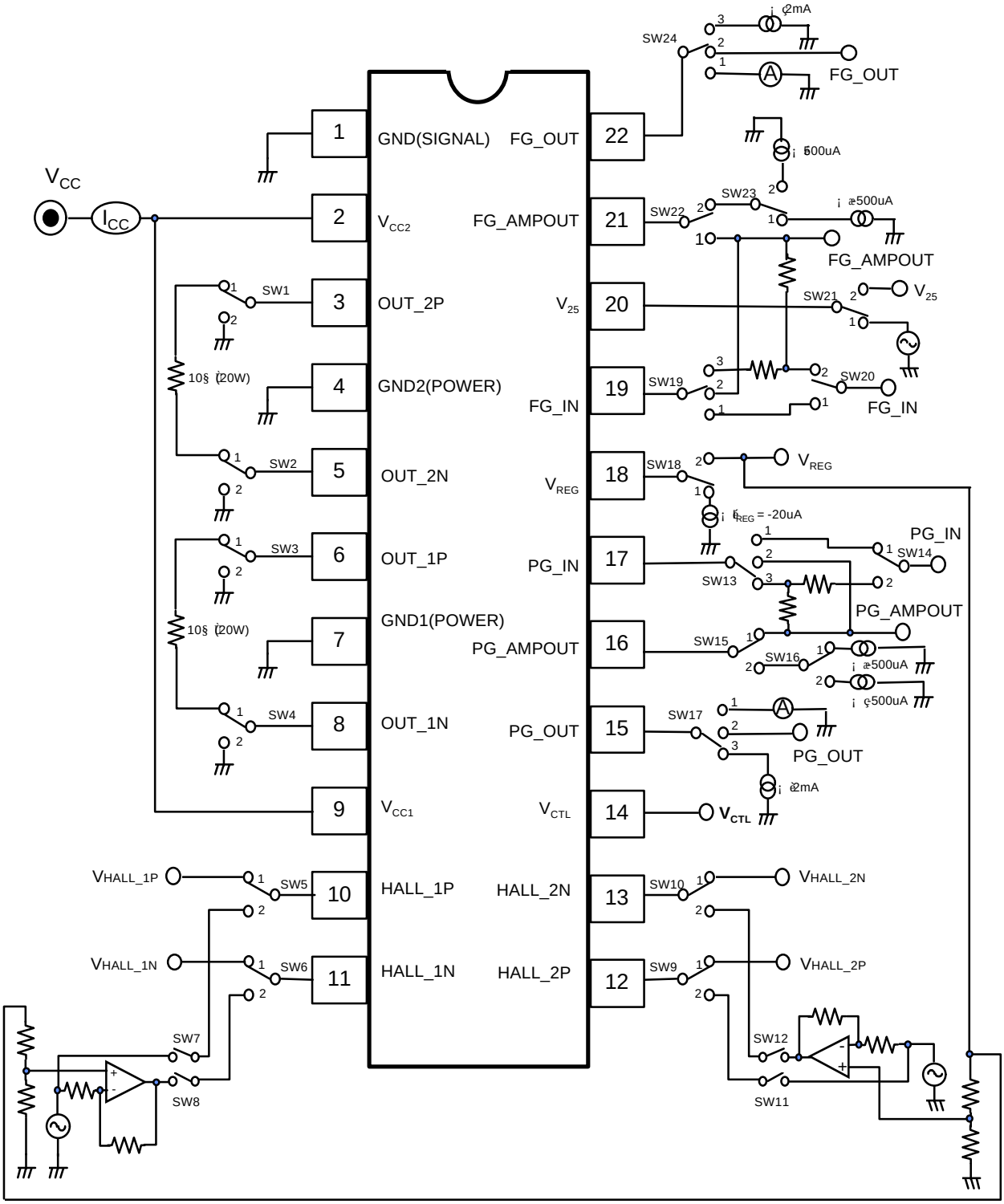
1. V_{CC} vs V_{REG}



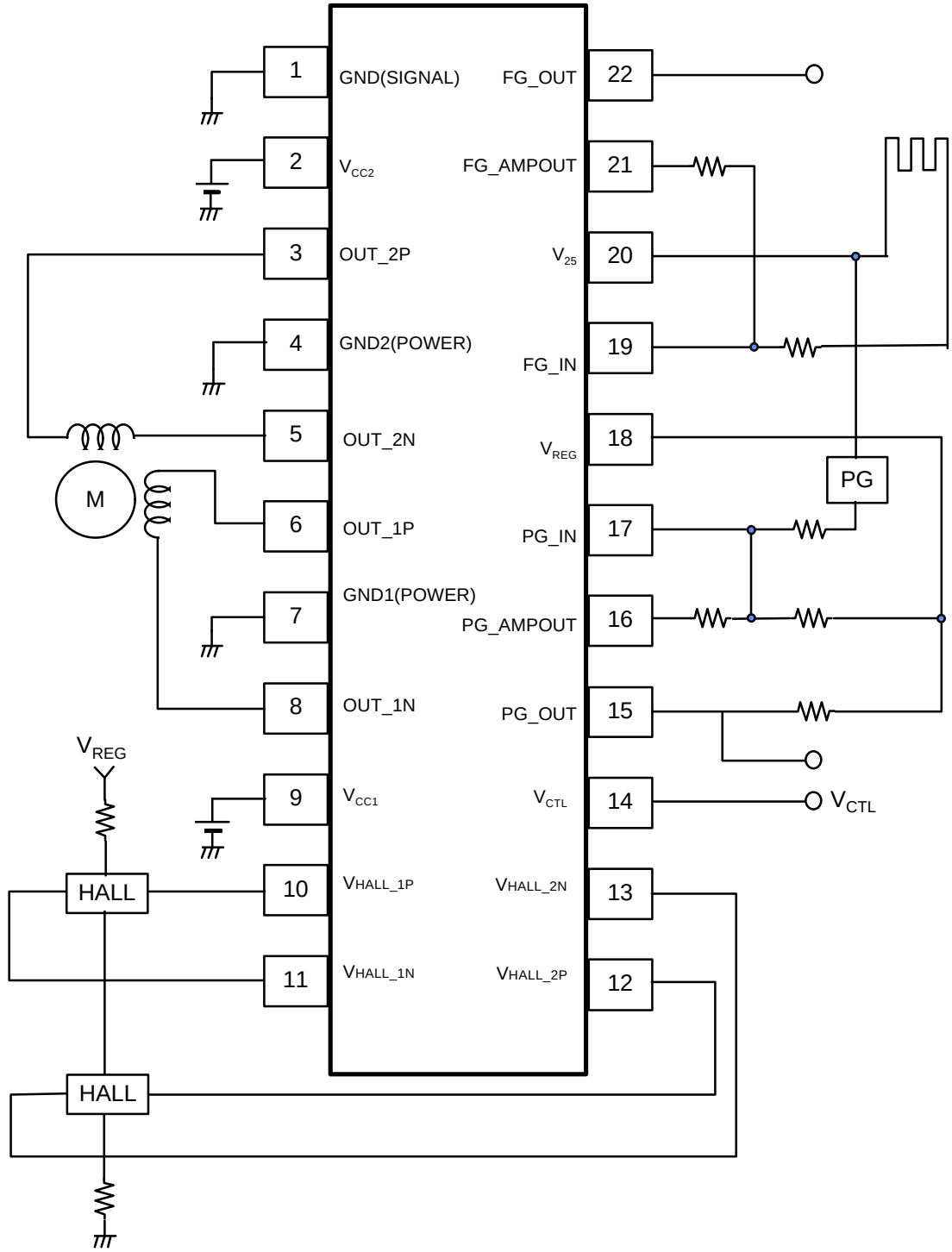
2. Temp. vs V_{REG}



TEST CIRCUIT



APPLICATION CIRCUIT



PACKAGE DIMENSIONS

22-SOP-300