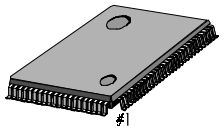
INTRODUCTION

The KS0104B is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology.
This device consists of 80 bit bi-directional shift register, 80 bit data latch and 80 bit driver.

100QFP-1420C



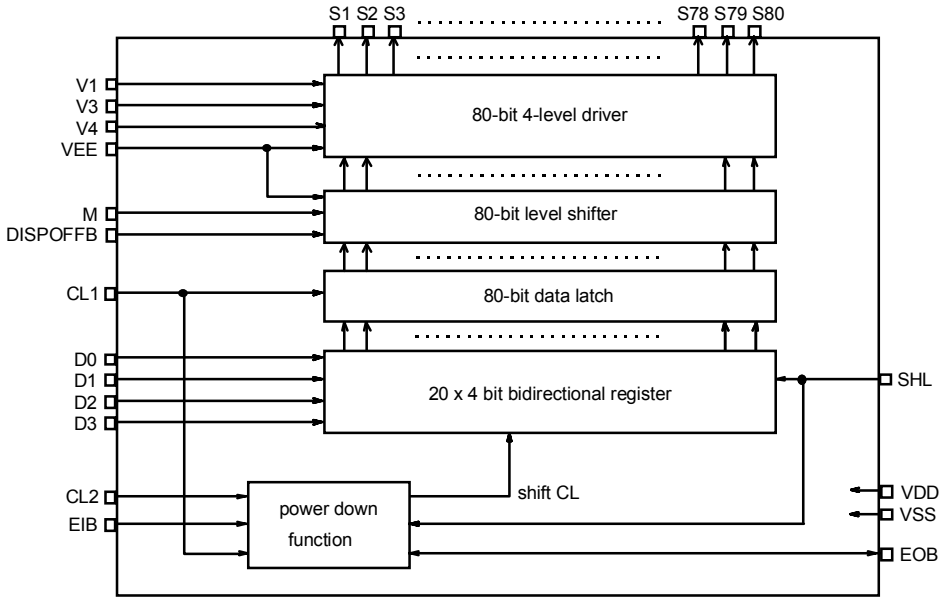
FEATURES

- Power supply voltage : +5V± 10%, +3V± 10%
- Supply voltage for display : 6 to 28V (VDD-VEE)
- Parallel data processing (4 bit)
- Applicable LCD duty : 1/64 to 1/256
- Interface

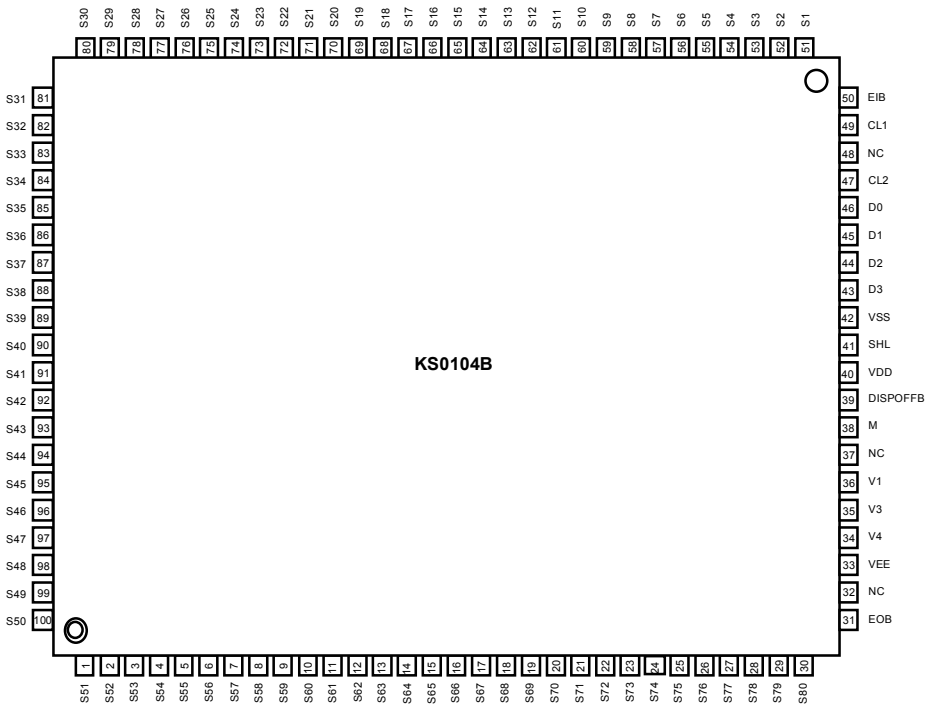
Driver	
COM	SEG (cascade)
KS0086	Other KS0104B

- High voltage CMOS process
- 100 QFP and bare chip available.

BLOCK DIAGRAM



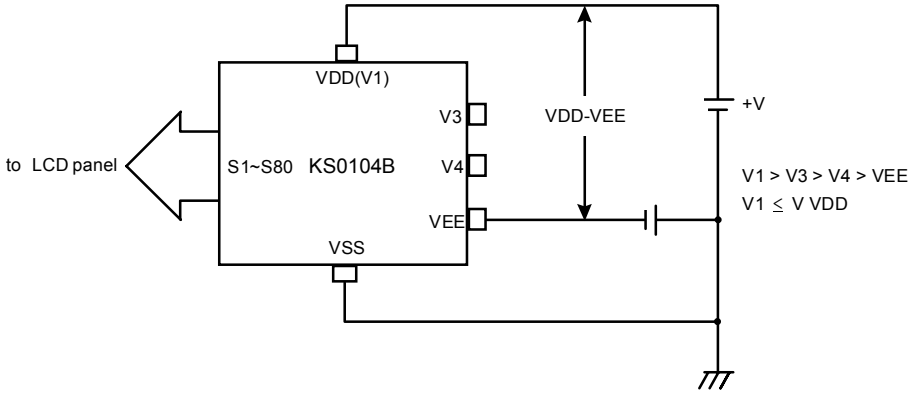
PIN CONFIGURATION



MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Operating Voltage	VDD	-0.3 ~ 6.0	V
Driver Supply Voltage	V_{LCD}	0 ~ 30	
Input Voltage	V_{IN}	-0.3 ~ VDD +0.3	
Operating Temperature	T_{OPR}	-30 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	

Voltage greater than above may result in damage to the circuit.



ELECTRICAL CHARACTERISTICS

DC Characteristics

(VDD = 2.7 to 5.5 V, VSS=0V, Ta=-30 to +85 °C, C_L = 15pF)

Characteristics	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage	VDD	-		2.7	-	5.5	V
Driver Supply Voltage	V_{LCD}	V_{LCD}=VDD - VEE		6	-	28	
Input Voltage (*1)	V_{IH}	-		0.8VDD	-	-	
	V_{IL}	-		0	-	0.2 VDD	
Output Voltage (*2)	V_{OH}	I_{OH} = -0.4 mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4 mA		-	-	0.4	
Input Leakage Current 1(*1)	I_{IL1}	V_{IN}=VDD to VSS		-1	-	1	μA
Input Leakage Current 2(*3)	I_{IL2}	V_{IN} = VDD to VEE		-25	-	25	
On Resistance (*4)	R_{ON}	I_{ON} = 100 μA		-	2	4	kΩ
Supply Current	I_{STB}	f_{CL2} = 1 MHz, f_{CL2} = 19.2 kHz, f_M = 40 Hz, V_{LCD} = 26 V, No load	VDD = 5.5 V (*5)	-	-	200	μA
	I_{DD}		VDD = 5.5 V (*6)	-	-	3	mA
			VDD = 2.7 V (*6)	-	-	1	mA
	I_{EE}		VDD = 5.5 V (*7)	-	150	500	μA

NOTES

(*1) Applied to CL1, CL2, EIB, EOB, D0 to D3, SHL, DISPOFFB, M pin.

(*2) EIB, EOB pin

(*3) V1, V3, V4 pin

(*4) VDD-VEE=26V (VDD=3V), VEE=28V(VDD=5V), V1=VDD, V3=VDD-2/10(VDD-VEE), V4=VEE+2/10(VDD-VEE), S1 to S80 pin

(*5) Display data pattern : 0000, Current from VDD to VSS when the display data is not processing (SHL=VSS, D0 to D3=VSS, DISPOFFB=VDD, M=VSS)

(*6) Display data pattern: 1010, Current from VDD to VSS when the display data is processing

(*7) Display data pattern: 1010, Current on VEE pin

AC Characteristics

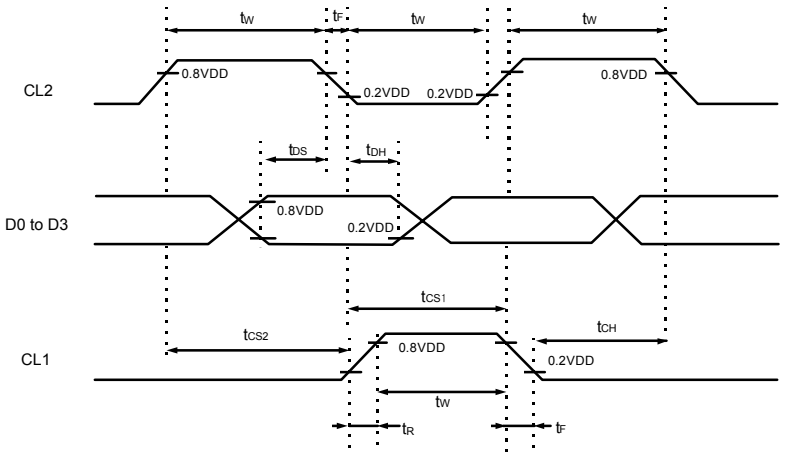
(VDD=+5V± 10%, VSS=0V, Ta=-30 to +85 °C, C_L=15pF)

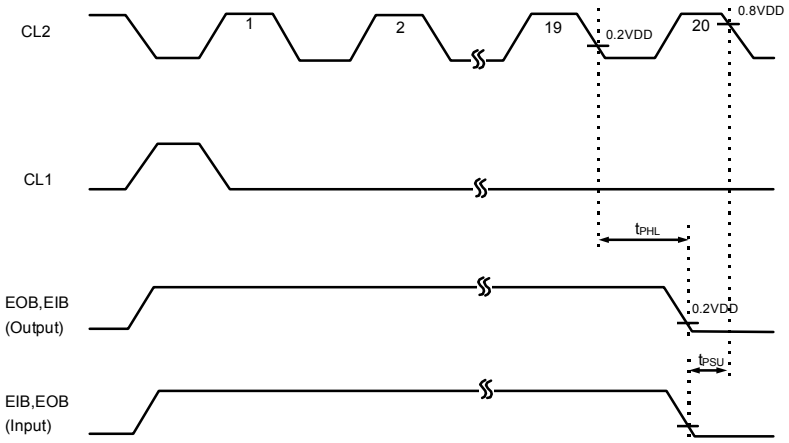
Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock Cycle Time	t_{CYC}	Duty=50%	125	-	-	ns
Clock Pulse Width	t_W	-	45	-	-	
Clock Rise/Fall Time	t_R/t_F	-	-	-	30	
Data Set-Up Time	t_{DS}	-	30	-	-	
Data Hold Time	t_{DH}	-	30	-	-	
Clock Set-Up Time1	T_{CS1}	-	80	-	-	
Clock Set-Up Time2	T_{CS2}	-	10	-	-	
Clock Hold Time	t_{CH}	-	80	-	-	
Propagation Delay Time	t_{PHL}	EOB Output	-	-	80	
		EIB Output			80	
EIB, EOB Set-Up Time	t_{PSU}	EOB Input	30	-	-	
		EIB Input	30			

(VDD=+3V± 10%, VSS=0V, Ta=-30 to +85 °C, C_L=15pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock Cycle Time	t_{CYC}	Duty=50%	250	-	-	ns
Clock Pulse Width	t_W	-	95	-	-	
Clock Rise/Fall Time	t_R/t_F	-	-	-	30	
Data Set-Up Time	t_{DS}	-	50	-	-	
Data Hold Time	t_{DH}	-	50	-	-	
Clock Set-Up Time1	T_{CS1}	-	80			
Clock Set-Up Time2	t_{CS2}	-	15	-	-	
Clock Hold Time	t_{CH}	-	120	-	-	
Propagation Delay Time	t_{PHL}	EOB Output	-	-	155	
		EIB Output			155	
EIB, EOB Set-Up Time	t_{PSU}	EOB Input	65	-	-	
		EIB Input	65			

Timing Characteristics



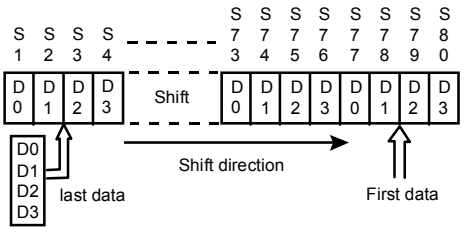
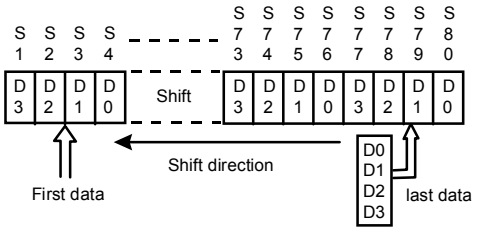


PIN DESCRIPTION

PIN (NO)	INPUT OUTPUT	NAME	FUNCTION	INTERFACE
VDD (40)	Power	Operating Voltage	For logical circuit (+5V± 10%, +3V± 10%)	Power Supply
VSS(42)			0V (GND)	
VEE(33)		Negative Supply Voltage	For LCD drive circuit	
V1, V3, V4 (34-36)	Input	LCD driver output voltage level	Bias supply voltage terminals to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. (refer to note 1)	Power
S1 ~ S80 (1-30, 51-100)	Output	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V1, V3, V4 and VEE is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to note 2)	LCD
CL2 (47)	Input	Data shift clock	Clock pulse input for the 4 bit parallel shift register. The data is shifted to 80 bit shift register at the falling edge of the clock pulse. The clock pulse, which was input when the enable bit (EIB/EOB) is not active condition, is invalid.	Controller
M (38)	Input	Alternate signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input	Controller
CL1 (49)	Input	Data latch clock	The signal for latching the shift register contents is input to this terminal. CL1 pulse "H" level initializes power-down function block.	Controller
DISPOFFB (39)	Input	Output level control (Display off)	Control input pin for display data output level (S1～S80). V1 level is output from S1～S80 terminal during "L" level input. LCD becomes non-selected by V1 level output from every output of segment drivers and every output of common drivers.	Controller
SHL (41)	Input	Data shift control	EOB and EIB can be used as either input terminal or output terminal according to the condition of SHL. The shifting direction of each data, D0～D3, the I/O condition of EOB and EIB, and the condition of SHL are described in the table below. (refer to note 3).	VDD/VSS

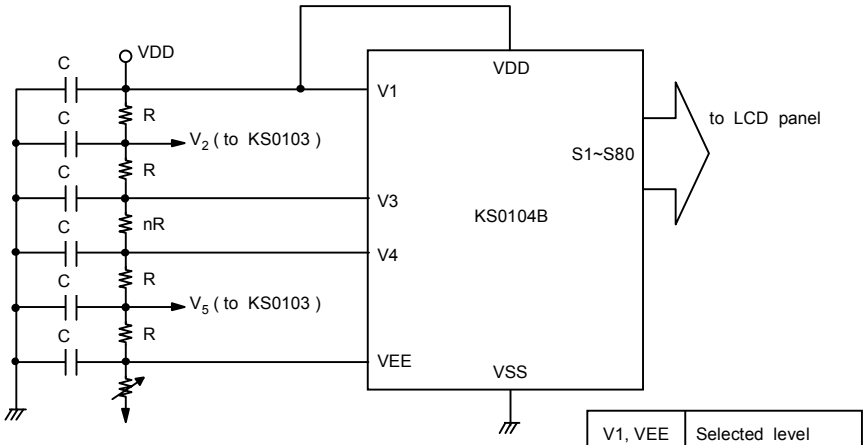
EOB, EIB (31,50)	Input Output	Pin	I/O	SHL	Display data shift direction	Description
		EOB	Input	L	D0 ; S1→ S5··· → S77 D1 ; S2→ S6··· → S78	Enable input terminal of KS0104B.
		EIB	Output		D2 ; S3→ S7··· → S79 D3 ; S4→ S8··· → S80	Enable output terminal of KS0104B. EIB is connected to next KS0104B's EOB when the KS0104B's are connected in series (cascade connection).
		EIB	Input	H	D0 ; S80→ S76··· → S4 D1 ; S79→ S75··· → S3	Enable input terminal of KS0104B.
		EOB	Output		D2 ; S78→ S74··· → S2 D3 ; S77→ S73··· → S1	Enable output terminal of KS0104B. EOB is connected to next KS0104B's EIB when the KS0104B's are connected in series (cascade connection)

PIN DESCRIPTION (continued)

<table>
<tr><th>PIN (NO)</th><th>INPUT
OUTPUT</th><th colspan="2">NAME</th><th colspan="2">FUNCTION</th><th>INTERFACE</th></tr>
<tr><td rowspan="5">D0 ~ D3
(43 ~ 46)</td><td rowspan="5">Input</td><td>Pin</td><td>I/O</td><td>SHL</td><td colspan="2">Data direction</td><td rowspan="5"></td></tr>
<tr><td>EOB</td><td>Input</td><td rowspan="2">L</td><td colspan="2" rowspan="2"> 
</td></tr>
<tr><td>EIB</td><td>Output</td></tr>
<tr><td>EIB</td><td>Input</td><td rowspan="2">H</td><td colspan="2" rowspan="2"> 
</td></tr>
<tr><td>EOB</td><td>Output</td></tr>
<tr><td>Display data input</td><td colspan="2">Display data input pins for 4 bit parallel shift register and it is input synchronized with the clock pulse.
The combination of D0-D3 level, M signal, display data output level and the display on the LCD panel is described on the table below.
(DISPOFFB = H)

<table><tr><th>D0 ~ D3</th><th>M</th><th>Display data output level</th><th>Display on the LCD</th></tr><tr><td>L</td><td>L</td><td>V3</td><td>OFF</td></tr><tr><td>H</td><td>L</td><td>V1</td><td>ON</td></tr><tr><td>L</td><td>H</td><td>V4</td><td>OFF</td></tr><tr><td>H</td><td>H</td><td>VEE</td><td>ON</td></tr></table></td><td>Controller</td></tr>
</table>

NOTE 1.



V1, VEE	Selected level
V3, V4	Nonselected level

* n=5(1/64 duty) to 13 (1/256 duty)

NOTE 2.

M	Latched data	DISPOFFB	Output level (S1 ~ S80)
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	VEE
X	X	L	V1

*NOTE 3

. EOB and EIB pins works as input terminals.
ENABLE F/F stops Display data at "H" level input. ENABLE F/F starts Display data at "L" level input.

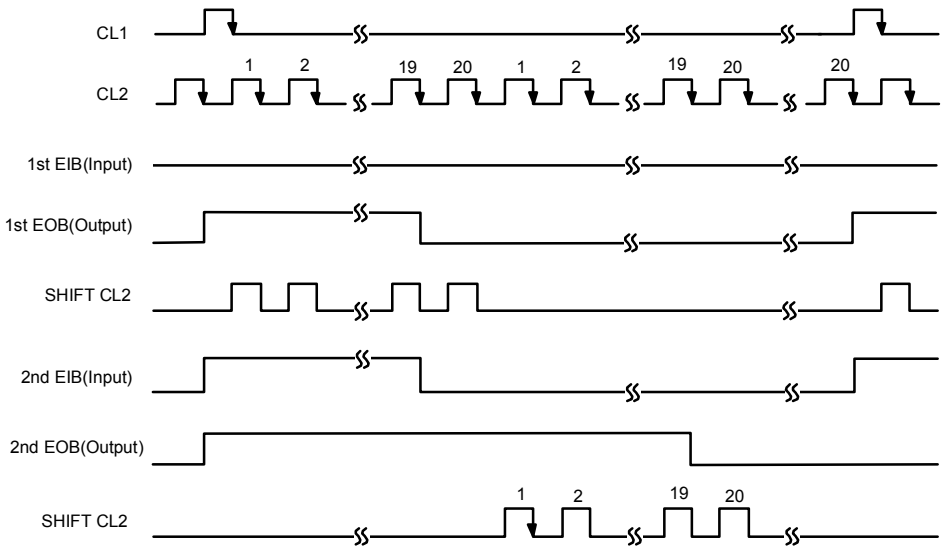
. EOB and EIB pins work as output terminals.
These terminals are set to the "H" level immediately after ENABLE F/F is initialized by the load pulse. Upon completion of 80-bit serial/parallel conversion using the shift clock input from the CL2 terminal, these terminals are then set to the "L" level.

. The operation of ENABLE F/F is terminated and held unchanged until the next load pulse is detected. (For cascade connection, refer to the application circuit drawing)

POWER DOWN FUNCTION

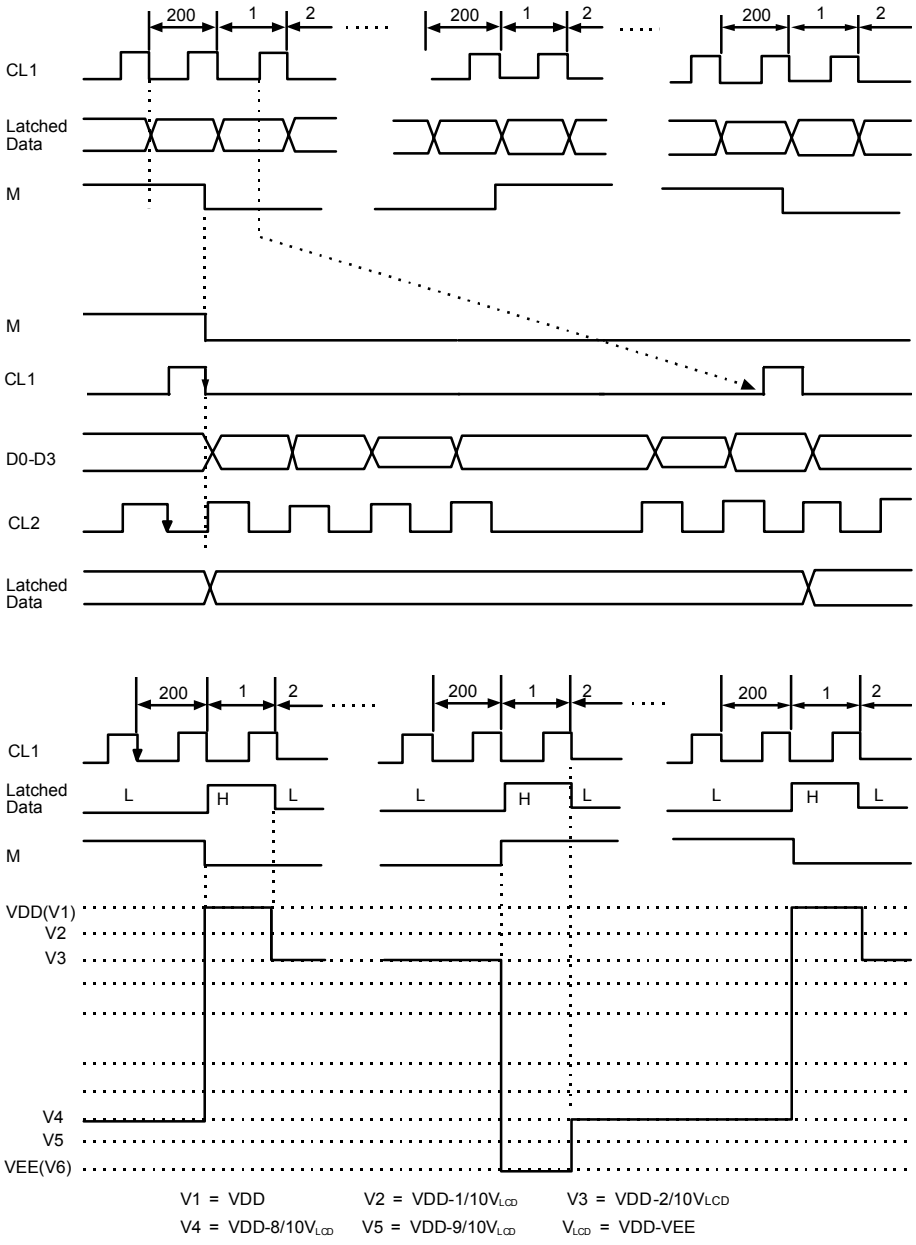
In order to reduce the power consumption, in case of cascade connection, KS0104B has a "power down function".

EIB	Enable input	Enable	L
		Disable	H
EOB	Enable output	EOB of Nth driver is connected to EIB of (N+1)th driver KS0104B	



SHL = “H” (EIB = Input, EOB = Output)
First KS0104B’s EOB should be connected to second KS0104B’s EIB.

Timing Chart - 1/200 Duty, 1/15 Bias

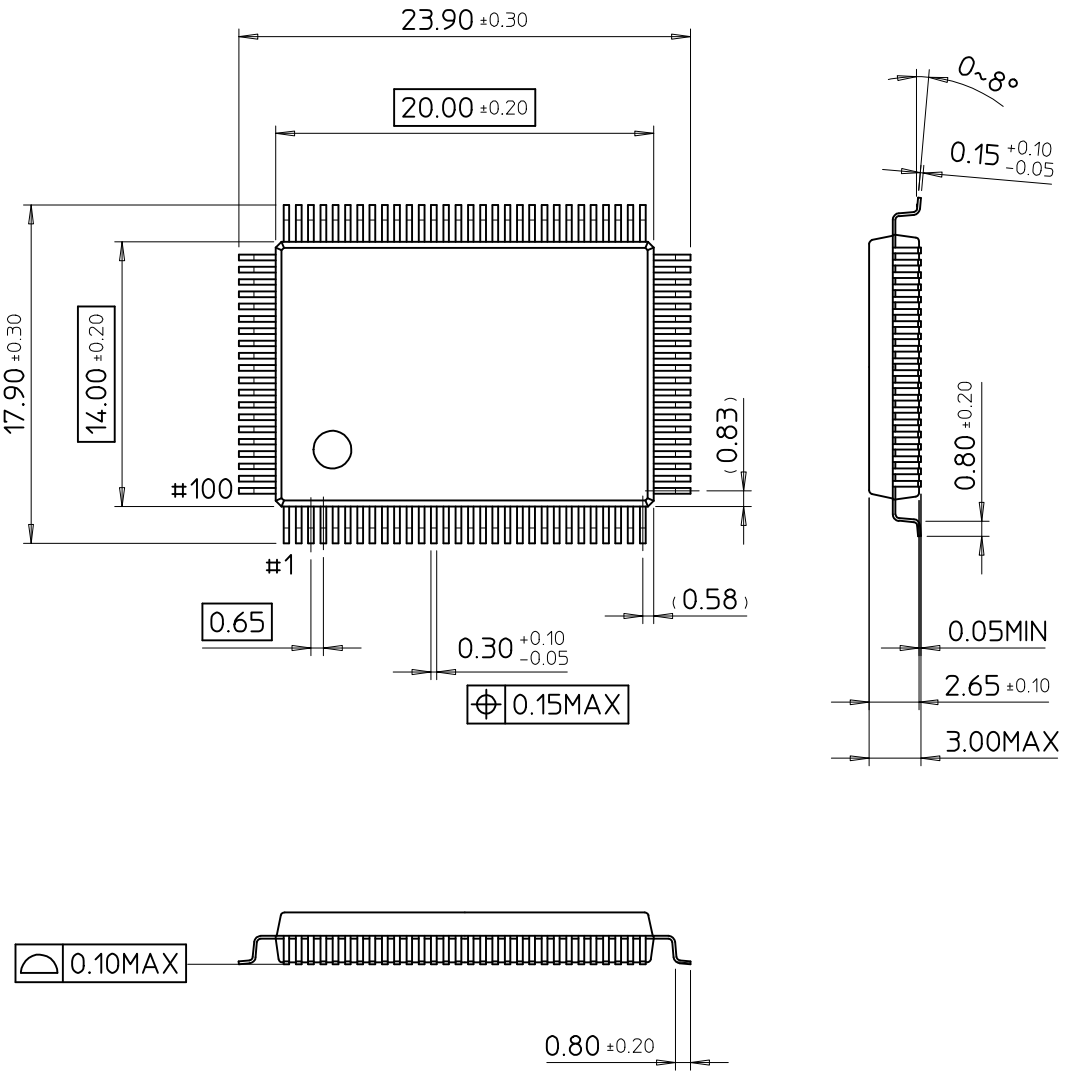


V1 = VDD V2 = VDD-1/10V_{LCD} V3 = VDD-2/10V_{LCD}

V4 = VDD-8/10V_{LCD} V5 = VDD-9/10V_{LCD} V_{LCD} = VDD-VEE

100-QFP-1420C

Dimensions in Milimeters



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