INTRODUCTION

The KS0715 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It contains 33 common and 100 segment driver circuits. This chip is connected directly to a microprocessor, accepts 8-bit serial or parallel display data and stores in an on-chip display data RAM of 65 × 132 bits. It provides a highly-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read / write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

FEATURES

- **Driver outputs**
  - — Common outputs: 33 common
  - — Segment outputs: 100 segment
- **On-chip display data RAM**
  - — Capacity: 65 × 132 = 8,580 bits
  - — Bit data “1”: a dot of display is illuminated
  - — Bit data “0”: a dot of display is not illuminated
- **Multi-chip operation (master, slave) available**
- **Applicable duty-ratio**

Duty Ratio	Applicable LCD Bias	Maximum Display Area
1/33	1/6 or 1/5	33×100

- **Microprocessor interface**
  - — 8-bit parallel bidirectional interface with 6800-series or 8080-series
  - — Serial interface (only write operation) available
- **Various instruction setting**
- **On-chip oscillator circuit**
- **On-chip low power supply for LCD driving voltage generation**
  - — Voltage converter (×2 / × 3 / × 4)
  - — Voltage regulator (temperature coefficient: – 0.05% / °C, – 0.2% / °C)
  - — Voltage follower (LCD Bias: 1/5 or 1/6)
- **On-chip electronic contrast control functions (32 steps)**
- **Operating voltage range**
  - — Supply voltage (V_{DD}): 2.4V to 5.5 V
  - — LCD driving voltage (V_{LCD} = V0 – V_{SS}): 4.0V to 15.0V

- **Low power consumption**
  - 100μA Max. (V_{DD} = 3V, × 4 boosting, V0 = 8V, Internal power supply on)
  - 10μA Max. (standby mode)
- **Wide operating temperature range**
  - Ta = – 40°C to 85°C
- **CMOS process**
- **Package type**
  - Slim chip for COG, and TCP available

BLOCK DIAGRAM

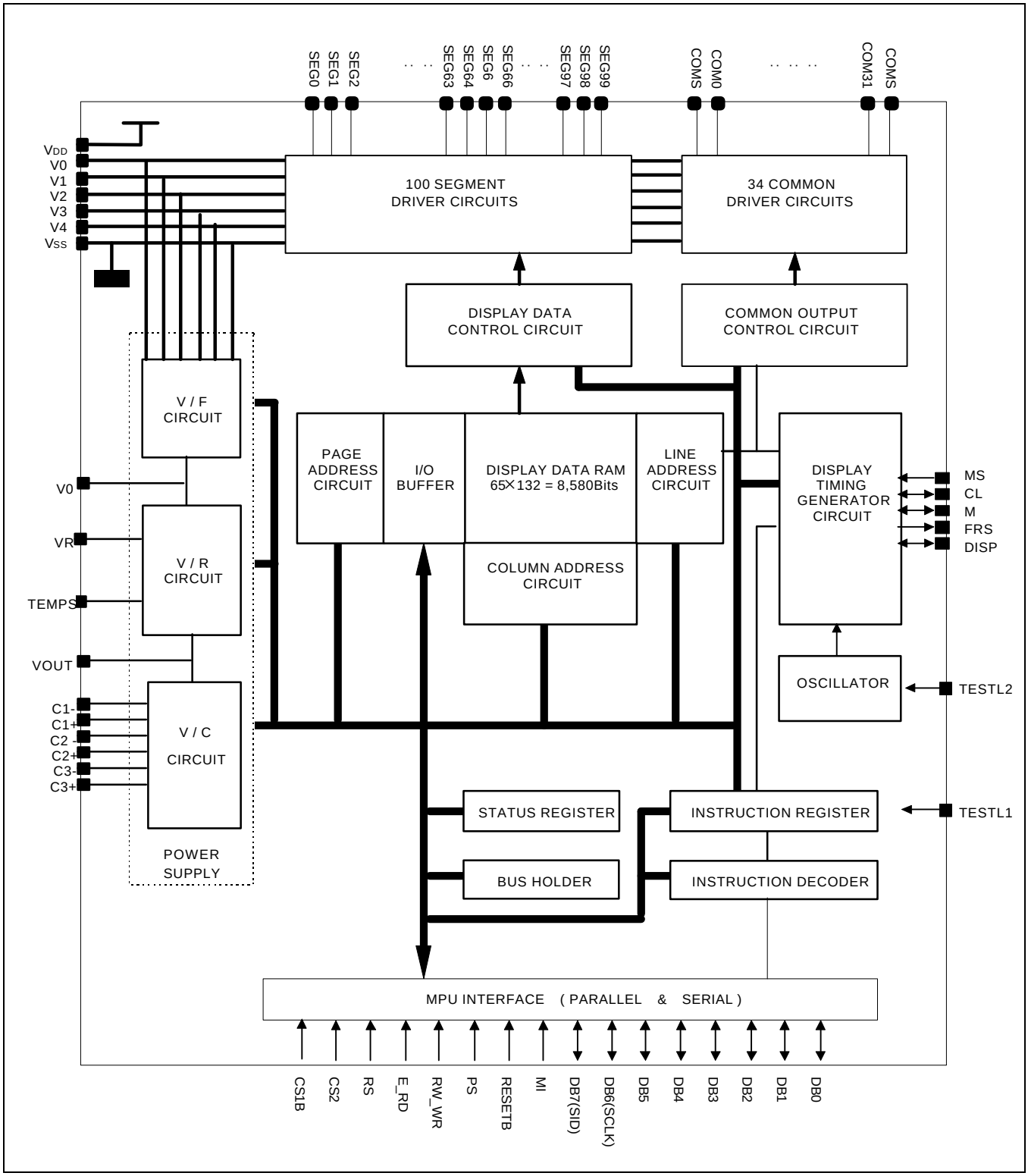


Figure 1. Block Diagram

PAD CONFIGURATION

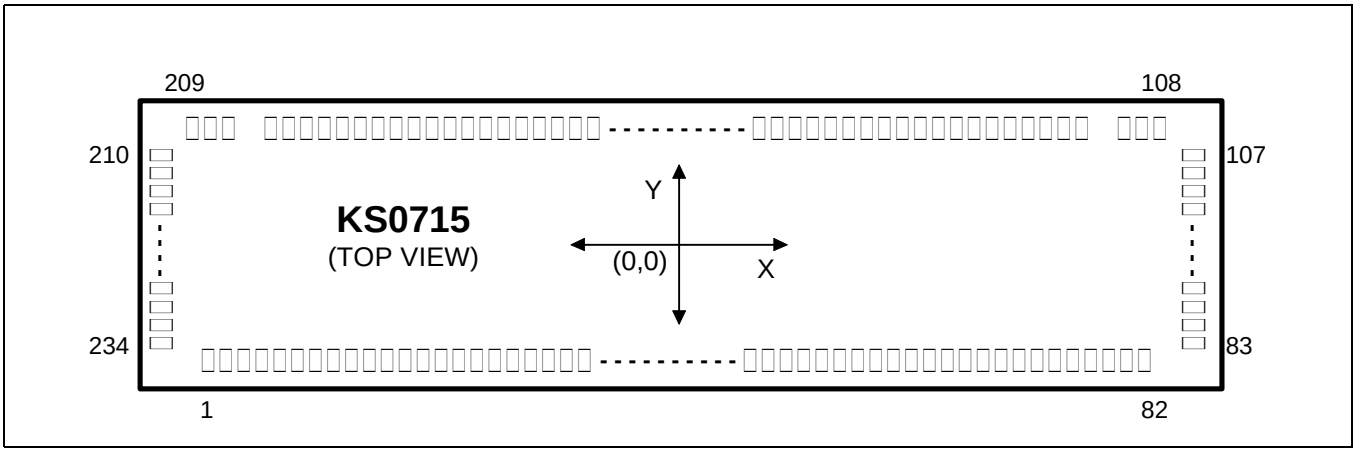


Figure 2. Pad Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	–	7980	2700	µm
Pad pitch	1 to 82	90		
	83 to 234	70		
Bumped pad size	1 to 82	56	114	
	83 to 107	108	50	
	108 to 209	50	108	
	210 to 234	108	50	
Bumped pad height	All pad	17 (Typ.)		

PAD LOCATION

Table 1. Pad Location

[unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	DUMMY	-3645	-1226	46	VOUT	405	-1226	91	COM11	3830	-280
2	TESTL1	-3555	-1226	47	C3+	495	-1226	92	COM10	3830	-210
3	VDD	-3465	-1226	48	C3+	585	-1226	93	COM9	3830	-140
4	FRS	-3375	-1226	49	C3-	675	-1226	94	COM8	3830	-70
5	M	-3285	-1226	50	C3-	765	-1226	95	COM7	3830	0
6	CL	-3195	-1226	51	C1+	855	-1226	96	COM6	3830	70
7	DISP	-3105	-1226	52	C1+	945	-1226	97	COM5	3830	140
8	VDD	-3015	-1226	53	C1-	1035	-1226	98	COM4	3830	210
9	MS	-2925	-1226	54	C1-	1125	-1226	99	COM3	3830	280
10	VSS	-2835	-1226	55	C2+	1215	-1226	100	COM2	3830	350
11	RESETB	-2745	-1226	56	C2+	1305	-1226	101	COM1	3830	420
12	VDD	-2655	-1226	57	C2-	1395	-1226	102	COM0	3830	490
13	PS	-2565	-1226	58	C2-	1485	-1226	103	COMS	3830	560
14	VSS	-2475	-1226	59	VSS	1575	-1226	104	DUMMY	3830	630
15	CS1B	-2385	-1226	60	VSS	1665	-1226	105	DUMMY	3830	700
16	CS2	-2295	-1226	61	VR	1755	-1226	106	DUMMY	3830	770
17	VDD	-2205	-1226	62	VR	1845	-1226	107	DUMMY	3830	840
18	MI	-2115	-1226	63	V0	1935	-1226	108	DUMMY	3535	1190
19	VSS	-2025	-1226	64	V0	2025	-1226	109	SEG0	3465	1190
20	VDD	-1935	-1226	65	V0	2115	-1226	110	SEG1	3395	1190
21	RS	-1845	-1226	66	V0	2205	-1226	111	SEG2	3325	1190
22	VSS	-1755	-1226	67	V0	2295	-1226	112	SEG3	3255	1190
23	RW_WR	-1665	-1226	68	V0	2385	-1226	113	SEG4	3185	1190
24	E_RD	-1575	-1226	69	V1	2475	-1226	114	SEG5	3115	1190
25	VDD	-1485	-1226	70	V1	2565	-1226	115	SEG6	3045	1190
26	VDD	-1395	-1226	71	V2	2655	-1226	116	SEG7	2975	1190
27	VDD	-1305	-1226	72	V2	2745	-1226	117	SEG8	2905	1190
28	VDD	-1215	-1226	73	V3	2835	-1226	118	SEG9	2835	1190
29	VDD	-1125	-1226	74	V3	2925	-1226	119	SEG10	2765	1190
30	VDD	-1035	-1226	75	V4	3015	-1226	120	SEG11	2695	1190
31	DB0	-945	-1226	76	V4	3105	-1226	121	SEG12	2625	1190
32	DB1	-855	-1226	77	VSS	3195	-1226	122	SEG13	2555	1190
33	DB2	-765	-1226	78	VSS	3285	-1226	123	SEG14	2485	1190
34	DB3	-675	-1226	79	TEMPS	3375	-1226	124	SEG15	2415	1190
35	DB4	-585	-1226	80	VDD	3465	-1226	125	SEG16	2345	1190
36	DB5	-495	-1226	81	TESTL2	3555	-1226	126	SEG17	2275	1190
37	DB6	-405	-1226	82	DUMMY	3645	-1226	127	SEG18	2205	1190
38	DB7	-315	-1226	83	DUMMY	3830	-840	128	SEG19	2135	1190
39	VSS	-225	-1226	84	DUMMY	3830	-770	129	SEG20	2065	1190
40	VSS	-135	-1226	85	DUMMY	3830	-700	130	SEG21	1995	1190
41	VSS	-45	-1226	86	DUMMY	3830	-630	131	SEG22	1925	1190
42	VSS	45	-1226	87	COM15	3830	-560	132	SEG23	1855	1190
43	VSS	135	-1226	88	COM14	3830	-490	133	SEG24	1785	1190
44	VSS	225	-1226	89	COM13	3830	-420	134	SEG25	1715	1190
45	VOUT	315	-1226	90	COM12	3380	-350	135	SEG26	1645	1190

Table 1. Pad Location (Continued)

[unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
136	SEG27	1575	1190	169	SEG60	-735	1190	202	SEG93	-3045	1190
137	SEG28	1505	1190	170	SEG61	-805	1190	203	SEG94	-3115	1190
138	SEG29	1435	1190	171	SEG62	-875	1190	204	SEG95	-3185	1190
139	SEG30	1365	1190	172	SEG63	-945	1190	205	SEG96	-3255	1190
140	SEG31	1295	1190	173	SEG64	-1015	1190	206	SEG97	-3325	1190
141	SEG32	1225	1190	174	SEG65	-1085	1190	207	SEG98	-3395	1190
142	SEG33	1155	1190	175	SEG66	-1155	1190	208	SEG99	-3465	1190
143	SEG34	1085	1190	176	SEG67	-1225	1190	209	DUMMY	-3535	1190
144	SEG35	1015	1190	177	SEG68	-1295	1190	210	DUMMY	-3830	840
145	SEG36	945	1190	178	SEG69	-1365	1190	211	DUMMY	-3830	770
146	SEG37	875	1190	179	SEG70	-1435	1190	212	DUMMY	-3830	700
147	SEG38	805	1190	180	SEG71	-1505	1190	213	DUMMY	-3830	630
148	SEG39	735	1190	181	SEG72	-1575	1190	214	DUMMY	-3830	560
149	SEG40	665	1190	182	SEG73	-1645	1190	215	COM17	-3830	490
150	SEG41	595	1190	183	SEG74	-1715	1190	216	COM18	-3830	420
151	SEG42	525	1190	184	SEG75	-1785	1190	217	COM19	-3830	350
152	SEG43	455	1190	185	SEG76	-1855	1190	218	COM20	-3830	280
153	SEG44	385	1190	186	SEG77	-1925	1190	219	COM21	-3830	210
154	SEG45	315	1190	187	SEG78	-1995	1190	220	COM22	-3830	140
155	SEG46	245	1190	188	SEG79	-2065	1190	221	COM23	-3830	70
156	SEG47	175	1190	189	SEG80	-2135	1190	222	COM24	-3830	0
157	SEG48	105	1190	190	SEG81	-2205	1190	223	COM25	-3830	-70
158	SEG49	35	1190	191	SEG82	-2275	1190	224	COM26	-3830	-140
159	SEG50	-35	1190	192	SEG83	-2345	1190	225	COM27	-3830	-210
160	SEG51	-105	1190	193	SEG84	-2415	1190	226	COM28	-3830	-280
161	SEG52	-175	1190	194	SEG85	-2485	1190	227	COM29	-3830	-350
162	SEG53	-245	1190	195	SEG86	-2555	1190	228	COM30	-3830	-420
163	SEG54	-315	1190	196	SEG87	-2625	1190	229	COM31	-3830	-490
164	SEG55	-385	1190	197	SEG88	-2695	1190	230	COMS	-3830	-560
165	SEG56	-455	1190	198	SEG89	-2765	1190	231	DUMMY	-3830	-630
166	SEG57	-525	1190	199	SEG90	-2835	1190	232	DUMMY	-3830	-700
167	SEG58	-595	1190	200	SEG91	-2905	1190	233	DUMMY	-3830	-770
168	SEG59	-665	1190	201	SEG92	-2975	1190	234	DYMMY	-3830	-840

PIN DESCRIPTIONS

Table 2. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages. The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship:

V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS

When the internal power circuit is active, these voltages are generated as the following table according to the state of LCD Bias.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/6 Bias</td><td>(5/6) V0</td><td>(4/6) V0</td><td>(2/6) V0</td><td>(1/6) V0</td></tr>
<tr><td>1/5 Bias</td><td>(4/5) V0</td><td>(3/5) V0</td><td>(2/5) V0</td><td>(1/5) V0</td></tr>
</table>
</td></tr>
<tr><td colspan="3">LCD Driver Supply</td></tr>
<tr><td>C1–</td><td>I</td><td>Capacitor 1– negative connection pin for voltage converter</td></tr>
<tr><td>C1+</td><td>I</td><td>Capacitor 1+ positive connection pin for voltage converter</td></tr>
<tr><td>C2–</td><td>I</td><td>Capacitor 2– negative connection pin for voltage converter</td></tr>
<tr><td>C2+</td><td>I</td><td>Capacitor 2+ positive connection pin for voltage converter</td></tr>
<tr><td>C3–</td><td>I</td><td>Capacitor 3– negative connection pin for voltage converter</td></tr>
<tr><td>C3+</td><td>I</td><td>Capacitor 3+ positive connection pin for voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage converter output</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjust pin</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">System Control</td></tr>
<tr><td>MS</td><td>I</td><td>Master / slave mode select input. Master makes some signals for display, and slave gets them. This is for display synchronization.
MS = “H”: Master mode
MS = “L”: Slave mode
<table>
<tr><th>MS</th><th>OSC circuit</th><th>Power supply cicuit</th><th>CL</th><th>M</th><th>FRS</th><th>DISP</th></tr>
<tr><td>H</td><td>Enable</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output. When KS0715 is used in master/slave mode (multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input/input. When KS0715 is used in master/slave mode (multi-chip), the M pins must be connected each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver output. This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I</td><td>LCD display blanking control input/output. When KS0715 is used in master/slave mode (multi-chip), the DISP pins must be connected each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>TEMPS</td><td>I</td><td>Selects temperature coefficient of the reference voltage
TEMPS = “L”: – 0.05% / °C
TEMPS = “H”: – 0.2% / °C</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Microprocessor Interface</td></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin. When RESETB is low, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>PS</th><th>Operating Mode</th><th>Chip Select</th><th>Data/ Instruction</th><th>Data Input/Output</th><th>Read/ Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB7 to DB0</td><td>E_RD, RW_WR</td><td>–</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>DB7 (SID)</td><td>Write Only</td><td>DB6 (SCLK)</td></tr>
</table>
NOTE: In serial mode, it is impossible to read data from the on-chip RAM. DB0 to DB5 is high impedance and E_RD and RW_WR must be fixed on high or low.</td></tr>
<tr><td>MI</td><td>I</td><td>Microprocessor interface select input in parallel mode.
MI = “H”: 6800-series MPU interface
MI = “L”: 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select inputs.

Data input / output is enabled only when CS1B is low and CS2 is high. When chip select is non-active, DB7 to DB0 will be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input.
RS = “H”: Then data on DB7 to DB0 is display data
RS = “L”: Then data on DB7 to DB0 is control data</td></tr>
<tr><td>RW_WR</td><td>I</td><td>When interfacing to a 6800-series MPU, Read/Write is enable.
RW_WR = “H”: Read
RW_WR = “L”: Write

When interfacing to a 8080-series MPU, RW_WR is enable at low.</td></tr>
<tr><td>E_RD</td><td>I</td><td>When interfacing to a 6800-series MPU: Active High.
This is used as an enable clock input pin of the 6800-series MPU.

When interfacing to an 8080-series MPU: Active Low.
This input connects the RD signal of the 8080-series MPU. While this signal is low, KS0715 data bus output is enabled.</td></tr>
<tr><td>DB0 to DB7</td><td>I/O</td><td>8-bit bidirectional data bus. It is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”):
DB7: Serial input data (SID)
DB6: Serial input clock (SCLK)
DB5 to DB0: High impedance.

When chip select is not active, DB7 to DB0 will be high impedance.</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">LCD Driver Outputs</td></tr>
<tr><td>SEG0 to SEG99</td><td>O</td><td>LCD driver output for segment. The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">M</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td></tr>
<tr><td>COM0 to COM31</td><td>O</td><td>LCD driver output for segment. The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th>Display Data</th><th>M</th><th>COMs Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons. The output signals of two pins are same. When not used, these pins should be left open. In multi-chip(master/slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
<tr><td colspan="3">Test Pin</td></tr>
<tr><td>TESTL1
TESTL2</td><td>I</td><td>IC test pins with pull-up.
These pins must be open.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

CHIP SELECT INPUT

There are CS1B and CS2 pins for chip selection. The KS0715 can interface with a microprocessor only when CS1B is low and CS2 is high. When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB7 to DB0 are to be high impedance. For the serial interface, the internal shift register and the counter are reset.

PARALLEL / SERIAL INTERFACE

The KS0715 has three types of interface with MPU: one serial and two parallel interface. This parallel or serial interface is determined by PS pin as shown in Table 3.

Table 3. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	MI	Interface Mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	X	Serial-mode

NOTE: "x" = Don't care

Parallel Interface (PS = "H")

The 8-bit bidirectional data bus is used in parallel interface and the type of MPU is selected by MI as shown in Table 4. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in Table 5.

Table 4. Microprocessor Selection for Parallel Interface

MI	CS1B	CS2	RS	E_RD	RW_WR	DB7 to DB0	MPU Bus
H	CS1B	CS2	RS	E	RW	DB7 to DB0	6800-series
L	CS1B	CS2	RS	RD	WR	DB7 to DB0	8080-series

Table 5. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (RD)	RW_WR (WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (Instruction)

Serial Interface (PS = “L”)

When the KS0715 is active (CS1B = L & CS2 = H), serial data (DB7) and serial clock (DB6) inputs are enabled. And when the KS0715 is not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock (DB6) and converted into 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

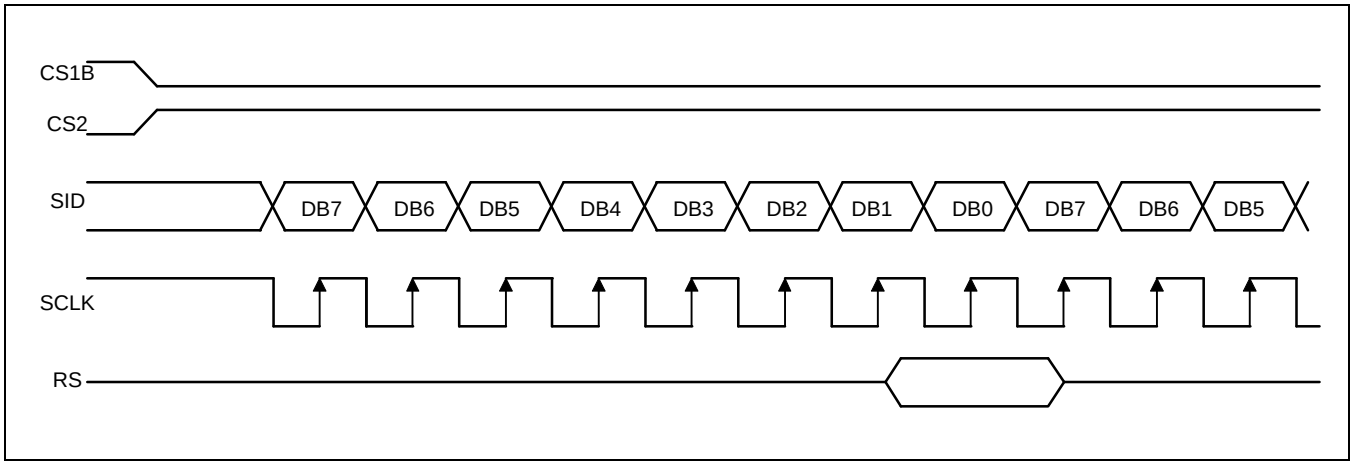


Figure 3. Serial Interface Timing

BUSY FLAG

The busy flag indicates whether the KS0715 is operating or not. When DB7 is high in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor does not need to check this flag before each instruction, which improves the microprocessor performance.

DATA TRANSFER

The KS0715 uses a bus holder and an internal data bus for data transfer with MPU. When writing data from the MPU to the on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure4. When reading data from the on-chip RAM to MPU, the data for the initial read cycle is stored in the bus holder (dummy read). Consequently, MPU reads this stored data from the bus holder for the next data read cycle, as shown in Figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed, so that the data of the specified address can be output with the read display data instruction at the second read of data rather than right after the address sets.

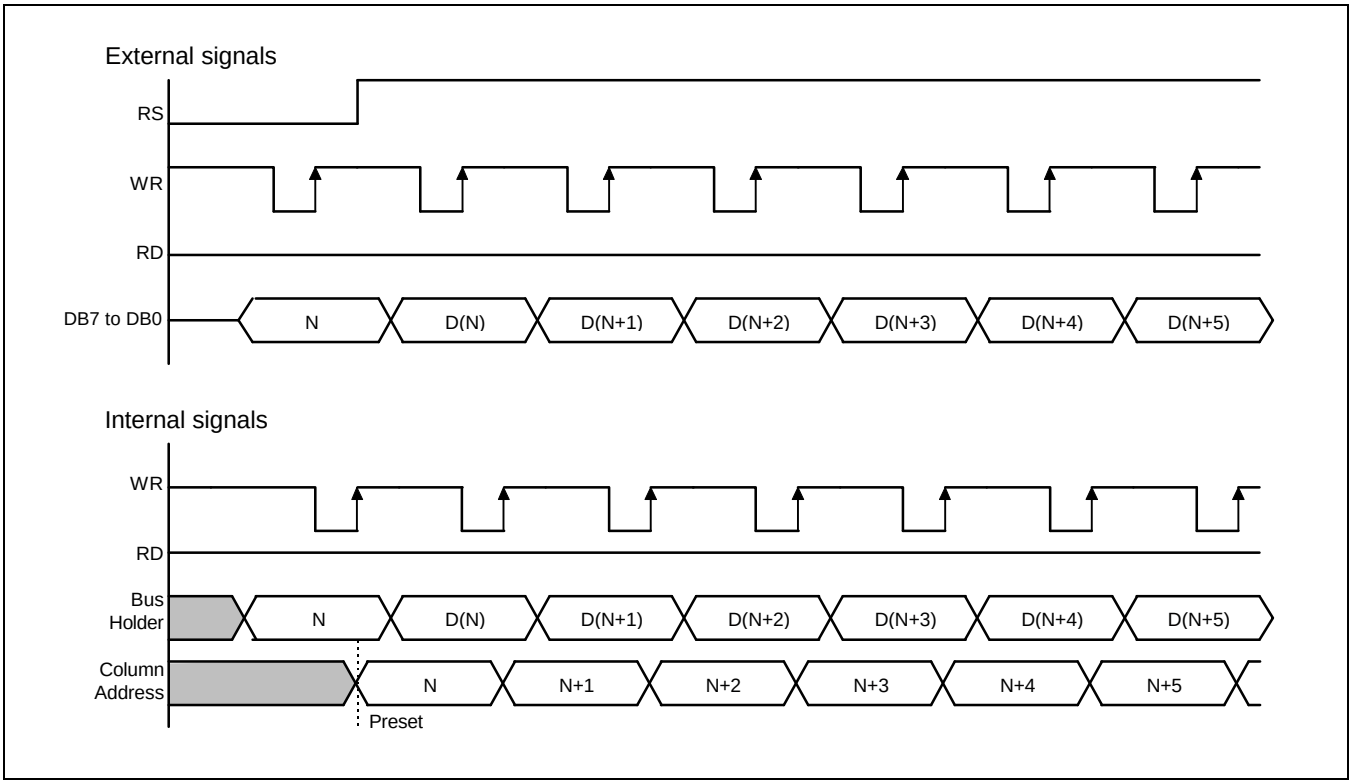


Figure 4. Write Timing

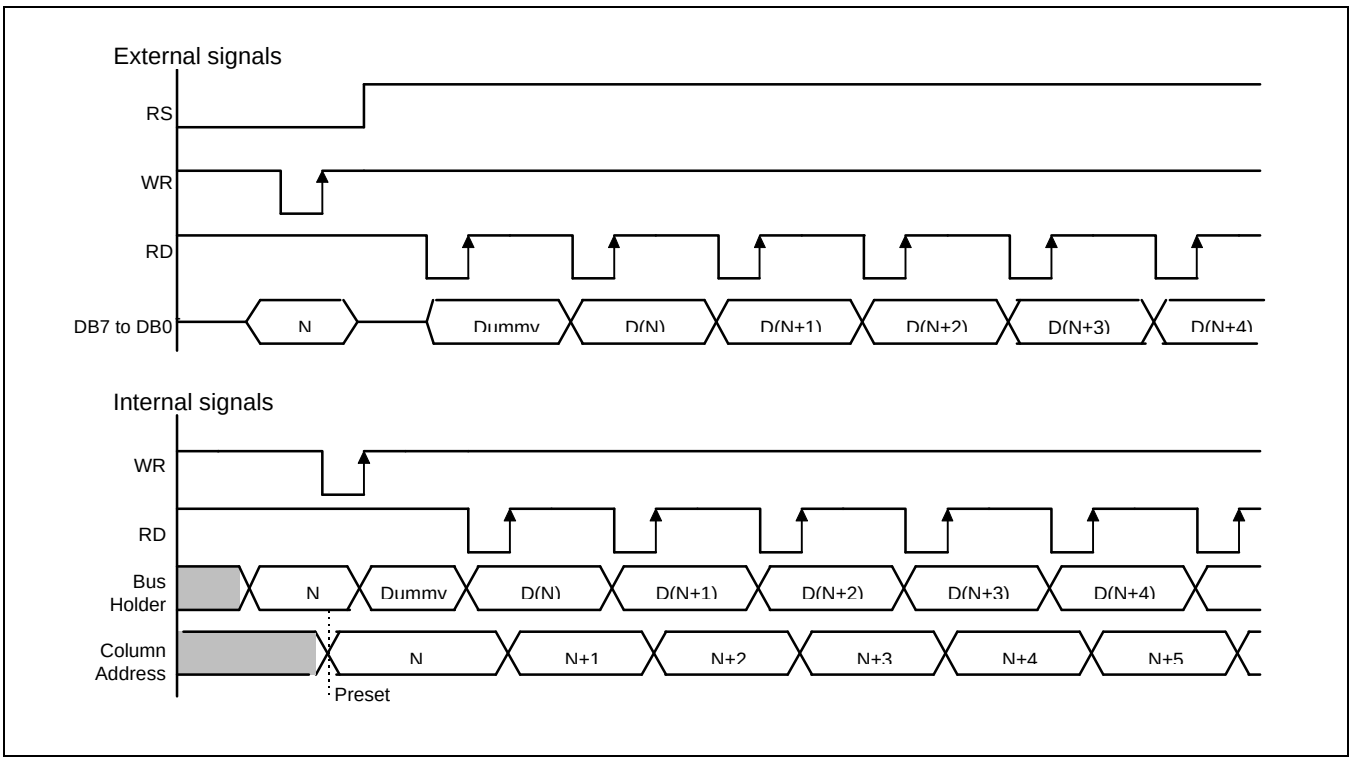


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The display data RAM stores pixel data for the LCD. It is a 65-row ((8 page by 8 bits) + 1) by 132-column addressable array. Each pixel can be selected when the page and column address is specified. The 65 rows are divided into 8 pages with 8 lines each, and a ninth page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 6.

The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as when data is being displayed without causing the LCD to flicker.

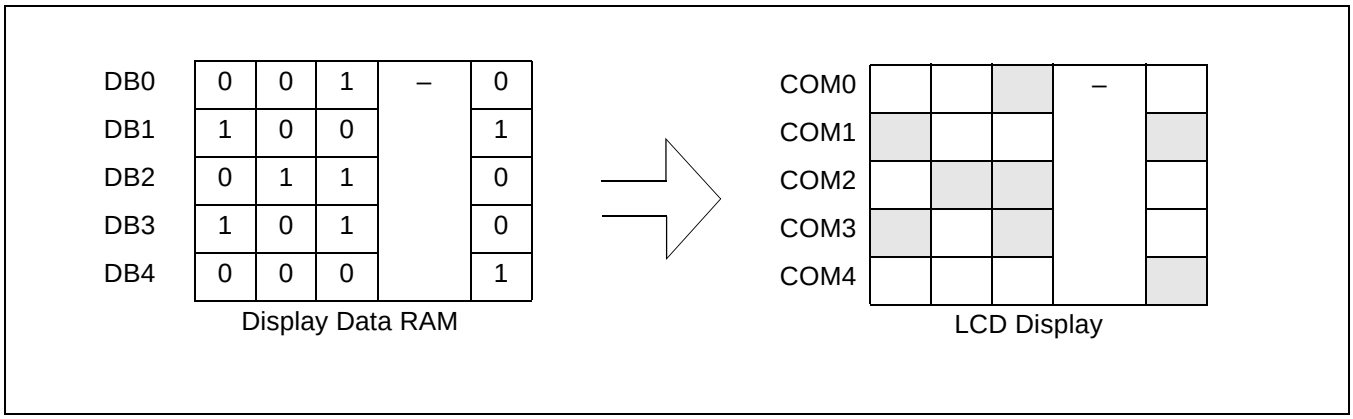


Figure 6. RAM-to-LCD Data Transfer

PAGE ADDRESS CIRCUIT

The function of this circuit is to provide a page address to the display data RAM shown in Table 7. It incorporates a 4-bit page address register changed only by the set page instruction. Page address 8 (DB3 is high, but DB2, DB1 and DB0 are low) is a special RAM area for icons, and only display data DB0 is valid. When page address is above 8, it is impossible to access the on-chip RAM.

LINE ADDRESS CIRCUIT

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display. Therefore, by setting the line address repeatedly, it is possible to scroll the screen and switch the page without changing the contents of the on-chip RAM (refer to Table 7). It incorporates a 6-bit Line Address register which can only be changed by the Initial display line instruction and a 6-bit counter circuit. At the beginning of each LCD frame, the contents of a register are copied to the line counter which is increased by the CL signal, and generates the line address for transferring the 132-bit RAM data to the 100 display data latch circuit. However, display data of icons are not scrolled because the microprocessor cannot access the line address of icons.

COLUMN ADDRESS CIRCUIT

The column address circuit has an 8-bit preset counter that provides the column address to the display data RAM (Shown in Table 7). When set column address MSB / LSB instruction is issued, 7 bits [Y7:Y0] are updated. Since this address is increased by 1 at every read or write data instruction, the microprocessor can access the display data continuously. However, the counter is not increased and locked for a non-existing address above 84H.

It is unlocked if a column address is set again by the set column address MSB / LSB instruction. The column address counter is independent of the page address register. ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. Refer to Table 6.

Table 6. Segment Output Direction According to ADC

SEG Output	**-**	**SEG0**	**SEG1**	**SEG2**	**.....**	**SEG97**	**SEG98**	**SEG99**	**-**
Column address [Y7:Y0]	00H to 0FH	10H	11H	12H	.....	71H	72H	73H	74H to 83H
Display data	X	1	0	0		0	1	1	X
LCD panel display (ADC = 0)	Not outputted								Not outputted
LCD panel display (ADC = 1)	Not outputted				.....				Not outputted

Table 7. Display Data RAM Addressing

Page Address P3, P2, P1, P0				Data	Column Address													Line Address (HEX)	Common Output
0	0	0	0	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page0							00 01 02 03 04 05 06 07	– – – – – – – –
0	0	0	1	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page1							08 09 0A 0B 0C 0D 0E 0F	– – – – – – – –
0	0	1	0	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page2							10 11 12 13 14 15 16 17	– – – – – – – –
0	0	1	1	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page3							18 19 1A 1B 1C 1D 1E 1F	– – – – COM0 COM1 COM2 COM3
0	1	0	0	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page4							20 21 22 23 24 25 26 27	COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11
0	1	0	1	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page5							28 29 2A 2B 2C 2D 2E 2F	COM12 COM13 COM14 COM15 COM16 COM17 COM18 COM19

Table 7. Display Data RAM Addressing

Page Address P3, P2, P1, P0				Data	Column Address													Line Address (HEX)	Common Output
0	1	1	0	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page6							30 31 32 33 34 35 36 37	COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27
0	1	1	1	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page7							38 39 3A 3B 3C 3D 3E 3F	COM28 COM29 COM30 COM31 – – – –
1	0	0	0	DB0							Page8								COMS
Column Address [HEX]				ADC = 0	00	~	0F	10	11	12	.....	71	72	73	74	~	83		
				ADC = 1	83	~	74	73	72	71	.....	12	11	10	0F	~	00		
LCD OUTPUT					–	~	–	SEG0	SEG1	SEG2	.....	SEG97	SEG98	SEG99	–		–		

NOTE: When the initial display line address is 1CH.

LCD DRIVING CIRCUIT

OSCILLATOR

This is a completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

DISPLAY TIMING GENERATOR CIRCUIT

This circuit generates some signals to be used in the LCD. The display clock (CL) generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CL). While the 100-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Two-frame AC driver waveforms and the internal timing signal are shown in Figure 7.
When KS0715 is used in multi-chip mode, the slave chip must receive the M, CL, DISP signals from the master. Table 8. shows the M, CL, and DISP status.

Table 8. Master and Slave Timing Signal Status

Operation Mode	Oscillator ON / OFF	M	CL	DISP
Master	ON	Output	Output	Output
Slave	OFF	Input	Input	Input

DISPLAY DATA LATCH CIRCUIT

This latch circuit temporarily stores the output display data from the display data RAM to the LCD driver in each instruction period. This latch circuit is controlled by the display ON / OFF, Reverse display ON / OFF, and entire display ON / OFF instructions. The data in the display data RAM remains unchanged.

Duty Ratio: 1/33

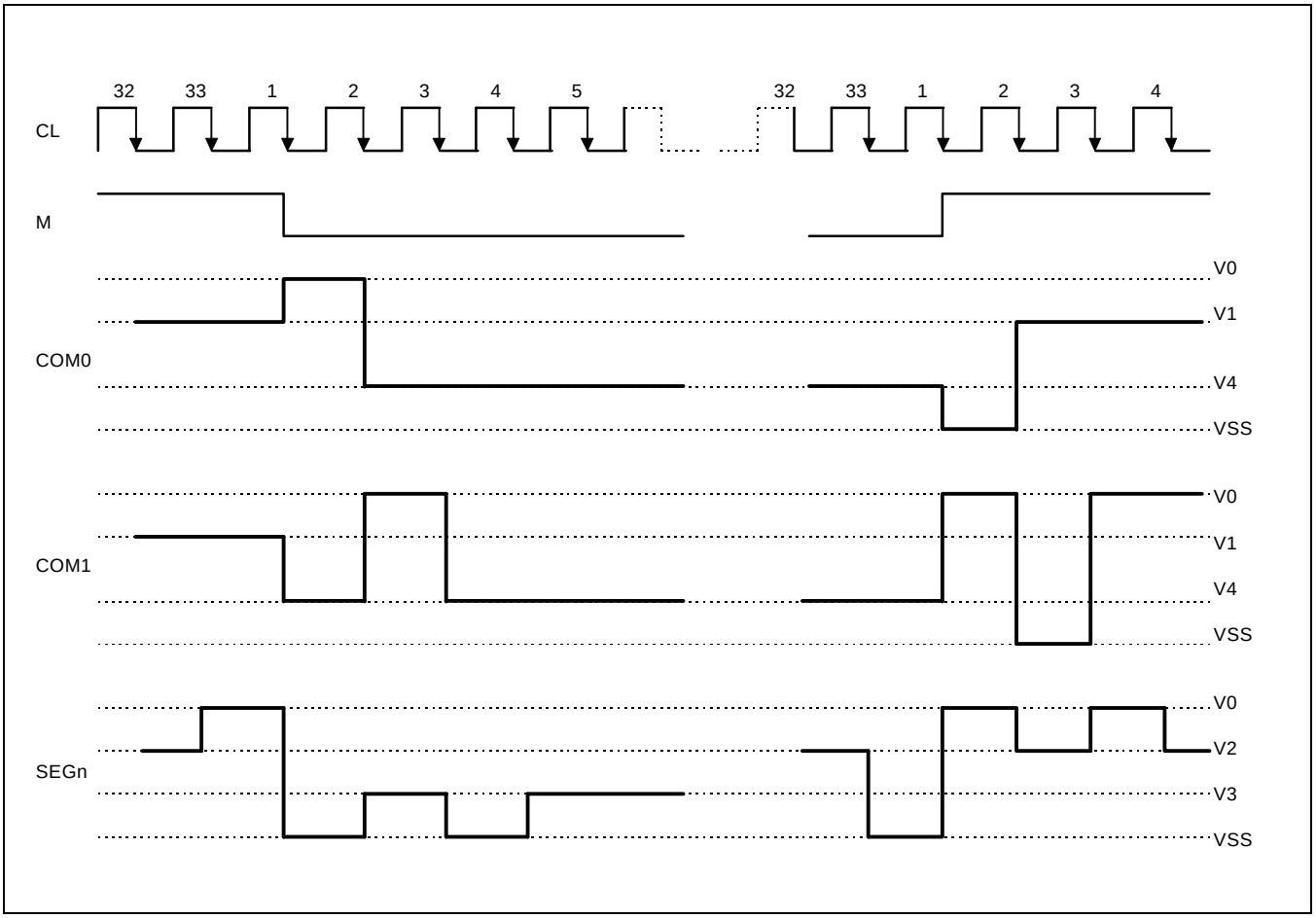


Figure 7. 2-Frame AC Driving Waveform

COMMON OUTPUT CONTROL CIRCUIT

This circuit controls the relationship between the number of common outputs and the specified duty ratio. SHL Select instruction specifies the scanning direction of the common output pins.

Table 9. The Relationship Between Duty Ration and Common Output

Duty	SHL	Common Output Pins	
		COM0 to COM31	COMS
1/33	0	COM0 to COM31	COMS
	1	COM31 to COM0	COMS

LCD DRIVER CIRCUIT

This driver circuit is configured by a 34-channel (including 2 COMS channel) common driver and a 100-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

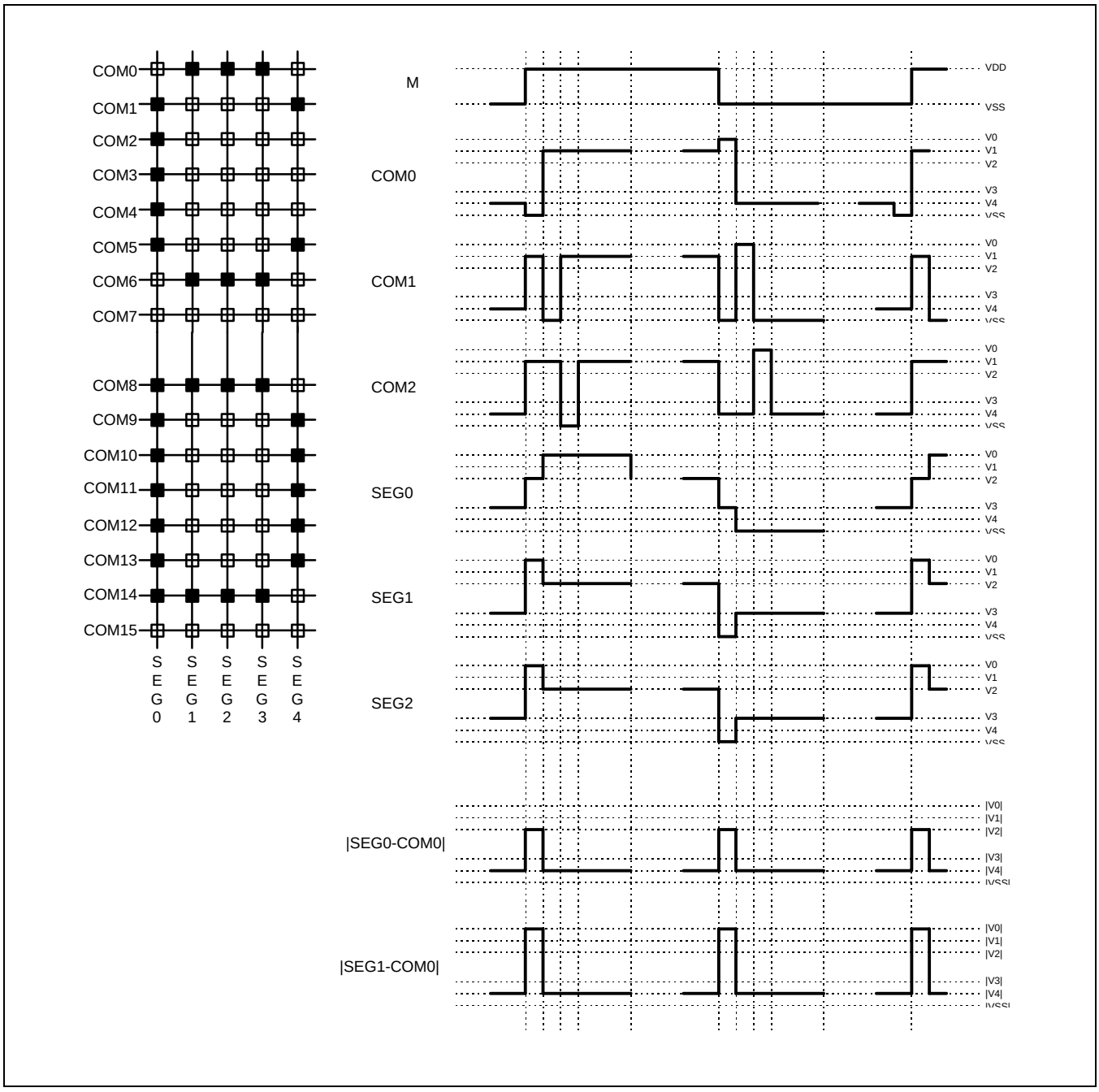


Figure 8. Segment and Common Timing

POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. These include voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and are controlled by power control instruction. For details, refer to “Instruction Description”. Table 10 shows the referenced combinations in using power supply circuits.

Table 10. Recommended Power Supply Combinations

User Setup	Power Control Register [VC, VR, VF]	V/C Circuits	V/R Circuits	V/F Circuits	VOUT Pin	V0 Pin	V1–V4 Pin
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External input	External input

VOLTAGE CONVERTER CIRCUITS

These circuits multiplies the electric potential between V_{DD} and V_{SS} to 2, 3, or 4 times toward the positive side. Boosted voltage is outputted from the VOUT pin.

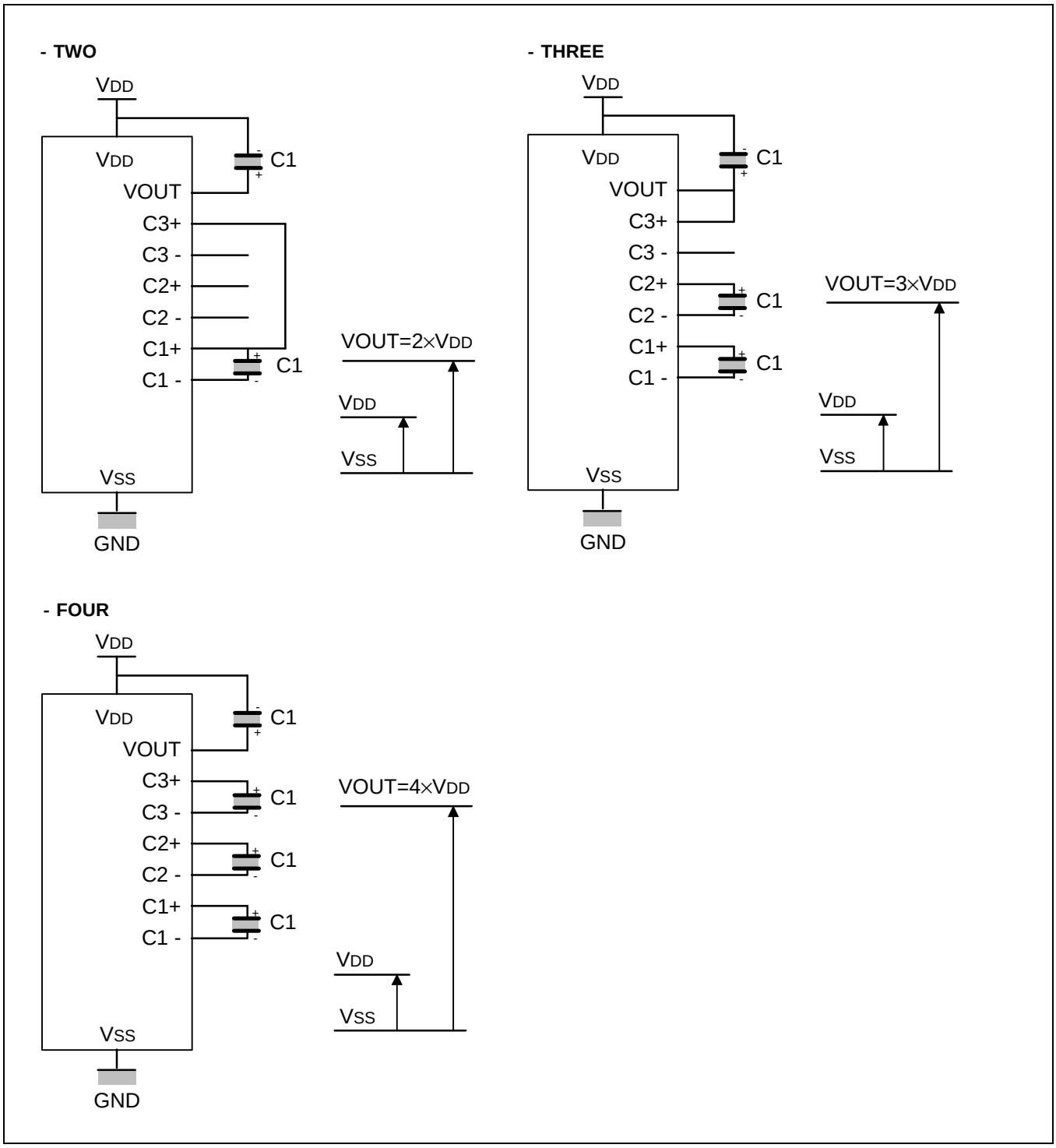


Figure 9. Boosting Two / Three / Four Times Circuit

VOLTAGE REGULATOR CIRCUITS

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors Ra and Rb, within the range of |V0| < |VOUT|. VOUT is the operating voltage of operational-amplifier circuits shown in Figure 10. So, it is necessary to apply internally or externally.

For the Equation 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected externally.
And the voltage of electronic volume (V_{EV}) is determined by Equation 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 31. V_{REF} voltage at Ta = 25°C is shown in Table 11.

<Equation 1>

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V]$$

<Equation 2>

$$V_{EV} = \left(1 - \frac{(31 - \alpha)}{150}\right) \times V_{REF} \quad [V]$$

Table 11. V_{REF} Voltage at Ta = 25°C

TEMPS	Temp. Coefficient	VREF [V]
0	– 0.05% / °C	1.9
1	– 0.2% / °C	2.0

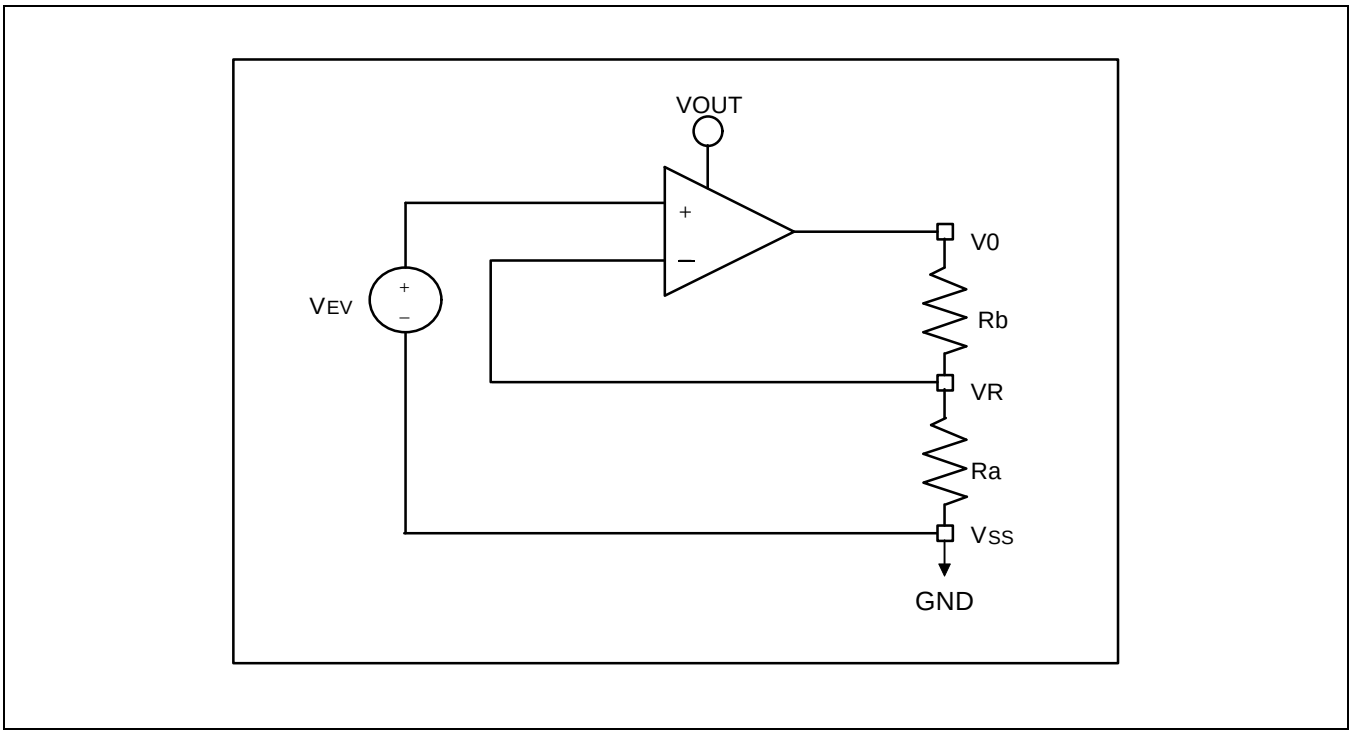


Figure 10. Internal Voltage Regulator Circuit

It is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements.

1. LCD driver voltage, V0 = 8V
2. 5-bit reference voltage register = (1, 1, 1, 1, 1)
3. Maximum current flowing Ra, Rb = 1μA

<Equation 3> From Equation 1

$$8 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \ [V]$$

<Equation 4> From Equation 1

$$V_{EV} = \left(1 - \frac{(31 - 31)}{150}\right) \times 1.9 = 1.9 \ [V]$$

<Equation 5> From requirement 3

$$\frac{8}{Ra + Rb} = 1 \ [\mu A]$$

From equations Equation 3, 4 and 5:

Ra = 1.9 [Ω]

Rb = 6.1 [Ω]

Table 12 shows the range of V0 depending on the above requirements.

Table 12. The Range of V0

	Electronic Volume Level				
	0	.....	16	.....	31
V0	6.33	.....	7.19	.....	8

VOLTAGE FOLLOWER CIRCUITS

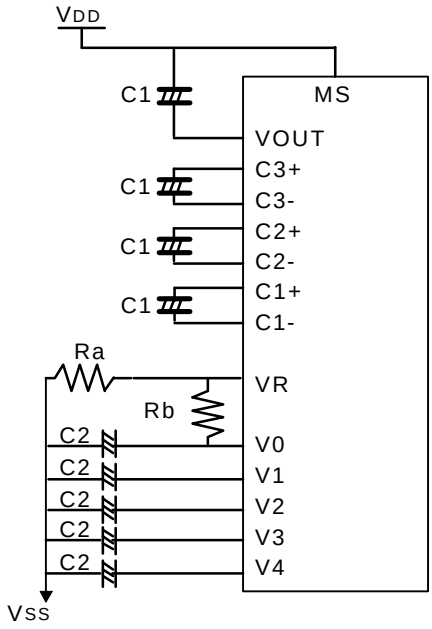
V_{LCD} voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower to increase the driving capability. Table 13 shows the relationship between V1 to V4 level and bias.

Table 13. The Relationship Between V1 to V4 Level and Each Duty Ratio

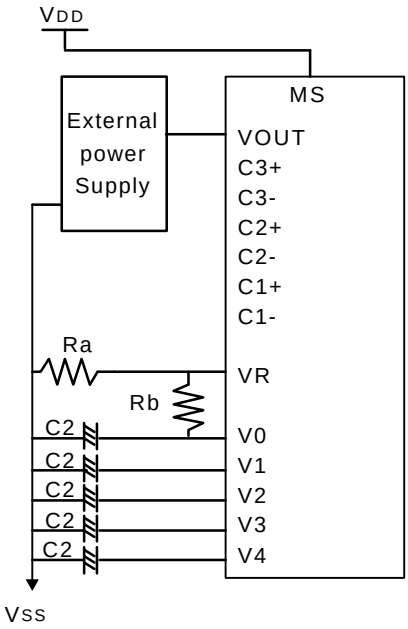
Duty Ratio	LCD Bias	V1	V2	V3	V4
1/33	1/6	5/6 × V0	4/6 × V0	2/6 × V0	1/6 × V0
	1/5	4/5 × V0	3/5 × V0	2/5 × V0	1/5 × V0

REFERENCED POWER SUPPLY CIRCUIT FOR DRIVING LCD PANEL

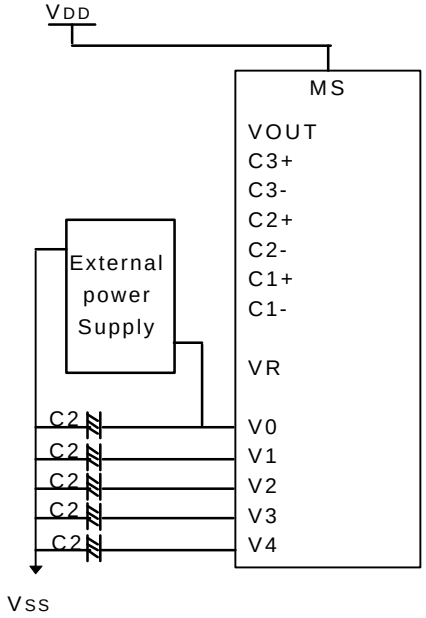
– When using all LCD power circuits
(Voltage converter, regulator and follower)
(In case of 4-times boosting circuit)



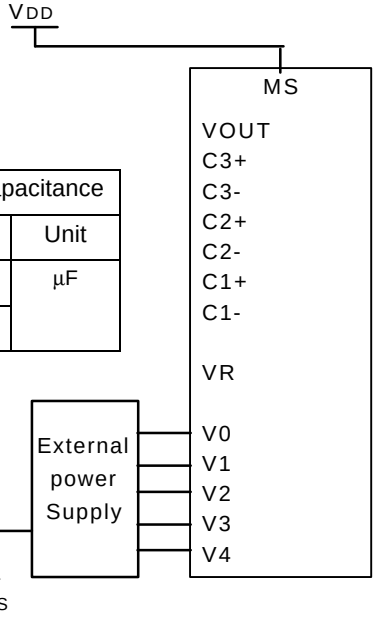
– When not using voltage converter circuits



– When using some LCD power circuits
(VC: off, VR: off, VF: on)



– When not using internal LCD power supply circuits



* Value of External Capacitance		
Item	Value	Unit
C1	1.0 – 4.7	µF
C2	0.47 – 1.0	

RESET CIRCUIT

Internal function can be initialized by setting RESETB to either Low or the Reset instruction.

When RESETB becomes low, the following procedure occurs.

- Display ON / OFF: OFF
- Entire display ON / OFF: OFF(Normal)
- ADC select: OFF(Normal)
- Reverse display ON / OFF: OFF(Normal)
- Power control register (VC, VR, VF) = (0, 0, 0)
- LCD bias ratio: 1/6
- Read modify– read: OFF
- SHL select: 0
- Static indicator mode: OFF
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Reference voltage set: OFF
  Reference voltage control register: (SV4, SV3, SV2, SV1, SV0) = (0, 0, 0, 0, 0)

When RESET instruction is issued, the following procedure occurs.

- Read– modify– read: OFF
- Static indicator mode: OFF
- SHL select: 0
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Reference voltage set: OFF
  Reference voltage control register (SV4, SV3, SV2, SV1, SV0) = (0, 0, 0, 0, 0)

While RESETB is low or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes low, any instruction can be accepted.

RESETB pin must be connected to the reset pin of MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB pin is essential before used.

INSTRUCTION DESCRIPTION

Table 14. Instruction Table

Instruction	Instruction Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON/ OFF	RE-SETB	0	0	0	0	Read the internal status
Display ON/OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON/OFF LCD panel When DON=0, display is OFF When DON=1, display is ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	1	0	0	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC=0 normal direction (SEG0 → SEG99), When ADC=1 reverse direction (SEG99 → SEG0)
Normal / Reverse display	0	0	1	0	1	0	0	1	1	REV	Select normal/reverse display When REV=0 normal, When REV=1 reverse
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal display / entire display ON When EON=0, normal display When EON=1, entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias. When BIAS=0, 1/6. When BIAS=1, 1/5
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize internal functions

Table 14. Instruction Table (Continued)

Instruction	Instruction Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL=0 normal direction (COM0 → COM31), When SHL=1 reverse direction (COM31 → COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Set static indicator register	0	0	1	0	1	0	1	1	0	SI	Set static indicator register SI=0(OFF), SI=1(ON)
Power Save	–	–	–	–	–	–	–	–	–	–	Compound command of display OFF and entire display ON
Test Instruction	0	0	1	1	1	1	×	×	×	×	Do not use this instruction

NOTE: "×" = Don't care

READ DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**1**	**Read Data**							

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

WRITE DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**0**	**Write Data**							

8-bit display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

READ STATUS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**BUSY**	**ADC**	**ON/OFF**	**RESETB**	**0**	**0**	**0**	**0**

Indicates the internal status conditions.

Flag	Description
BUSY	The device is busy when carrying out internal operation or reset. All instructions are rejected until BUSY goes to low. 0: Chip is active, 1: Chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: Reverse direction (SEG99 → SEG0), 1: Normal direction (SEG0 → SEG99)
ON/OFF	Indicates display ON / OFF status. 0: Display ON, 1: Display OFF
RESETB	Indicates initialization is in progress by RESETB signal. 0: Chip is active, 1: Chip is being reset.

DISPLAY ON/OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**DON**

Turns the display ON or OFF

DON	Display status
1	Display ON
0	Display OFF

INITIAL DISPLAY LINE

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**1**	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**

Sets the line address of display RAM to determine the initial display line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM31 when SHL = H) of the LCD panel.

ST5	ST4	ST3	ST2	ST1	ST0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

REFERENCE VOLTAGE SELECT

Set Reference Voltage Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**SV4**	**SV3**	**SV2**	**SV1**	**SV0**

Consists of two bytes instruction. The first byte sets reference voltage mode, the second one updates the contents of reference voltage register. After second instruction reference voltage mode is released.

SV4	SV3	SV2	SV1	SV0	Reference Voltage
0	0	0	0	0	0
:	:	:	:	:	:
1	1	1	1	1	31

SET PAGE ADDRESS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**1**	**P3**	**P2**	**P1**	**P0**

Sets the page address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the column address, the page address defines the address of the display RAM to write or read display data. changing the page address doesn't affect the display status.

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

SET COLUMN ADDRESS

– Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	**0**	**Y6**	**Y5**	**Y4**

– Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**0**	**Y3**	**Y2**	**Y1**	**Y0**

Sets the column address of the display RAM from the microprocessor into the column address register. The column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased, starting with the address stored in the column address register and continuously rotating right.

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99

ADC SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**ADC**

Changes the relationship between the RAM column address and segment driver. The direction of the segment driver output pins can be reversed by software. This makes the IC layout flexible in the LCD module assembly.

ADC	Direction
0	Normal direction (SEG0 → SEG99)
1	Reverse direction (SEG99 → SEG0)

NORMAL / REVERSE DISPLAY

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**REV**

Reverses the display status on the LCD panel without rewriting the contents of the display data RAM.

REV	RAM Bit Data = "1"	RAM Bit Data = "0"
0 (Normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (Reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

ENTIRE DISPLAY ON / OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**EON**

Forces all LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are put on hold. This instruction has priority over the reverse display ON / OFF instruction.

EON	Display status
0	Normal display
1	Entire display on

LCD BIAS SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**BIAS**

Selects the LCD bias ratio of the voltage required for driving the LCD.

Duty Ratio	LCD Bias	
	BIAS = 0	**BIAS = 1**
1/33	1/6	1/5

SET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data. It reduces the load of the microprocessor when the data of a specific area is repeatedly changed during cursor blinking. This mode is canceled by the reset modify-read instruction.

RESET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This instruction cancels the modify read mode, and makes the column address return to its initial value just before the set modify read instruction starts.

RESET

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This instruction resets the initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply which is initialized by the RESETB pin.

SHL SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**0**	**0**	**SHL**	´	´	´

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

SHL	Direction
0	Normal direction (COM0 → COM31)
1	Reverse direction (COM31 → COM0)

POWER CONTROL

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**1**	**VC**	**VR**	**VF**

Selects one out of eight power circuit functions by using a 3-bit register. An external power supply and a part of internal power supply functions can be used simultaneously.

VC	indicates whether the voltage converter turns on or not
VR	indicates whether the voltage regulator turns on or not
VF	indicates whether the voltage follower turns on or not

SET STATIC INDICATOR STATE

– Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**SI**

This instruction sets the static indicator ON / OFF. When it is on, the static indicator operates and blinks at an interval of approximately one second.

SI	**Status of Static Indicator Output**
0	OFF
1	ON (About 1 second blinking)

POWER SAVE (COMPOUND INSTRUCTION)

If the entire display ON / OFF instruction is issued during the display OFF state, KS0715 enters the power save status to reduce the power consumption to the static power consumption value. According to the status of the static indicator mode, power save is put into either sleep or standby mode. When the static indicator mode is ON, standby mode is issued: when OFF, sleep mode is issued. Power save mode is released by the display ON or entire display OFF instruction.

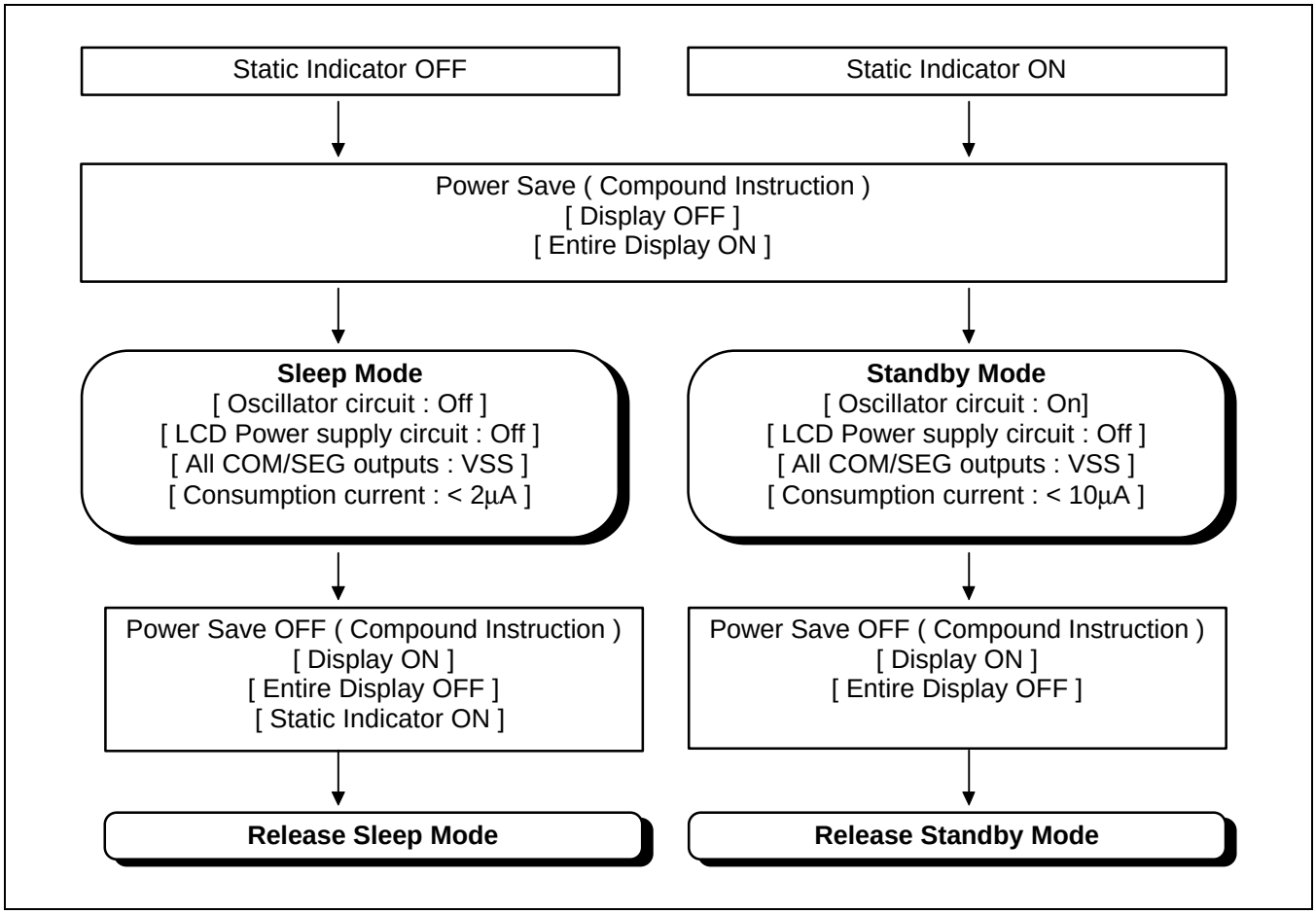


Figure 11. Power Save (Compound Instruction)

REFERENTIAL INSTRUCTION SETUP FLOW

— Initializing With the Built-in Power Supply Circuits

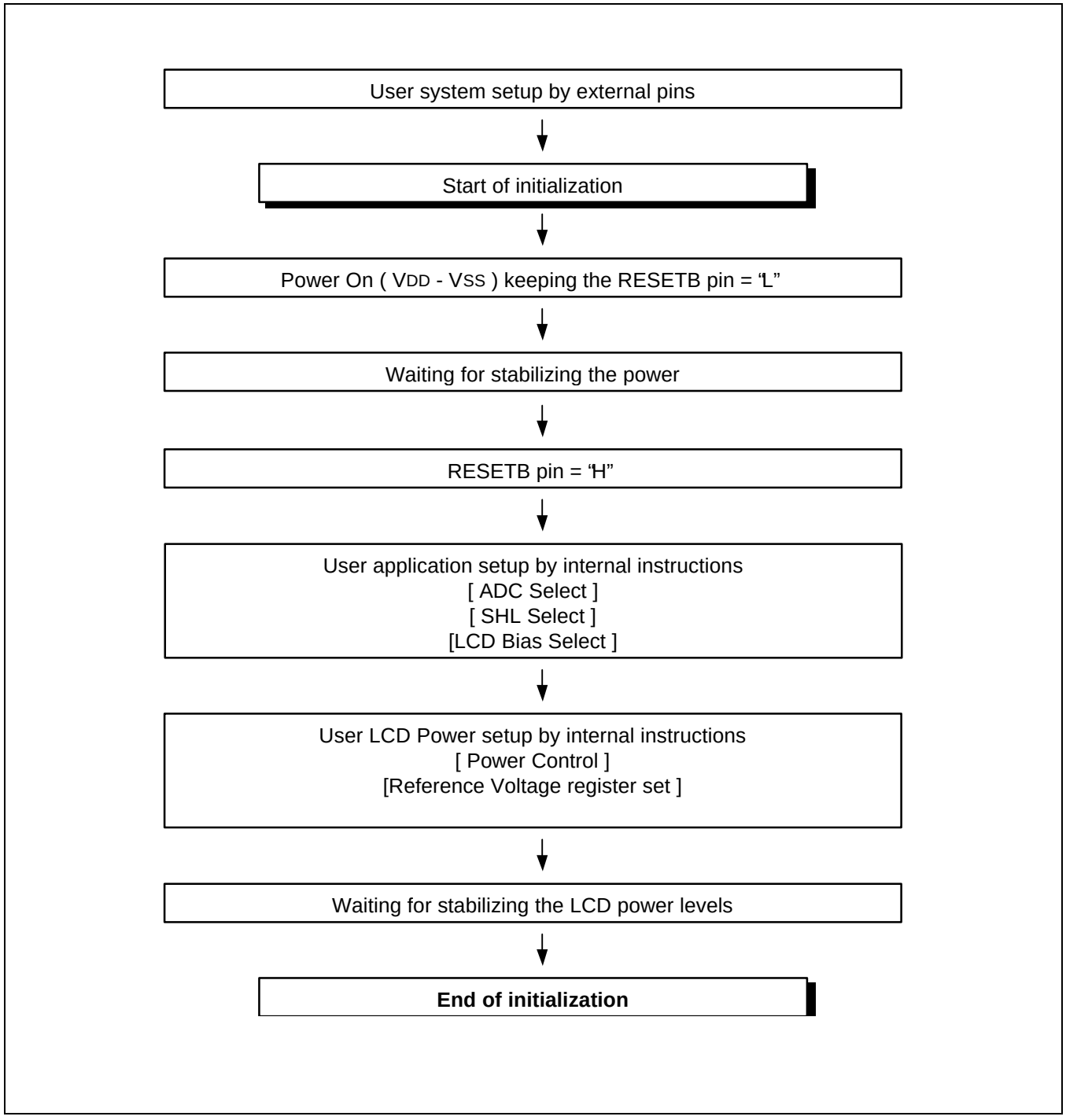


Figure 12. Initializing With The Built-in Power Supply Circuits

— Initializing Without the Built-in Power Supply Circuits

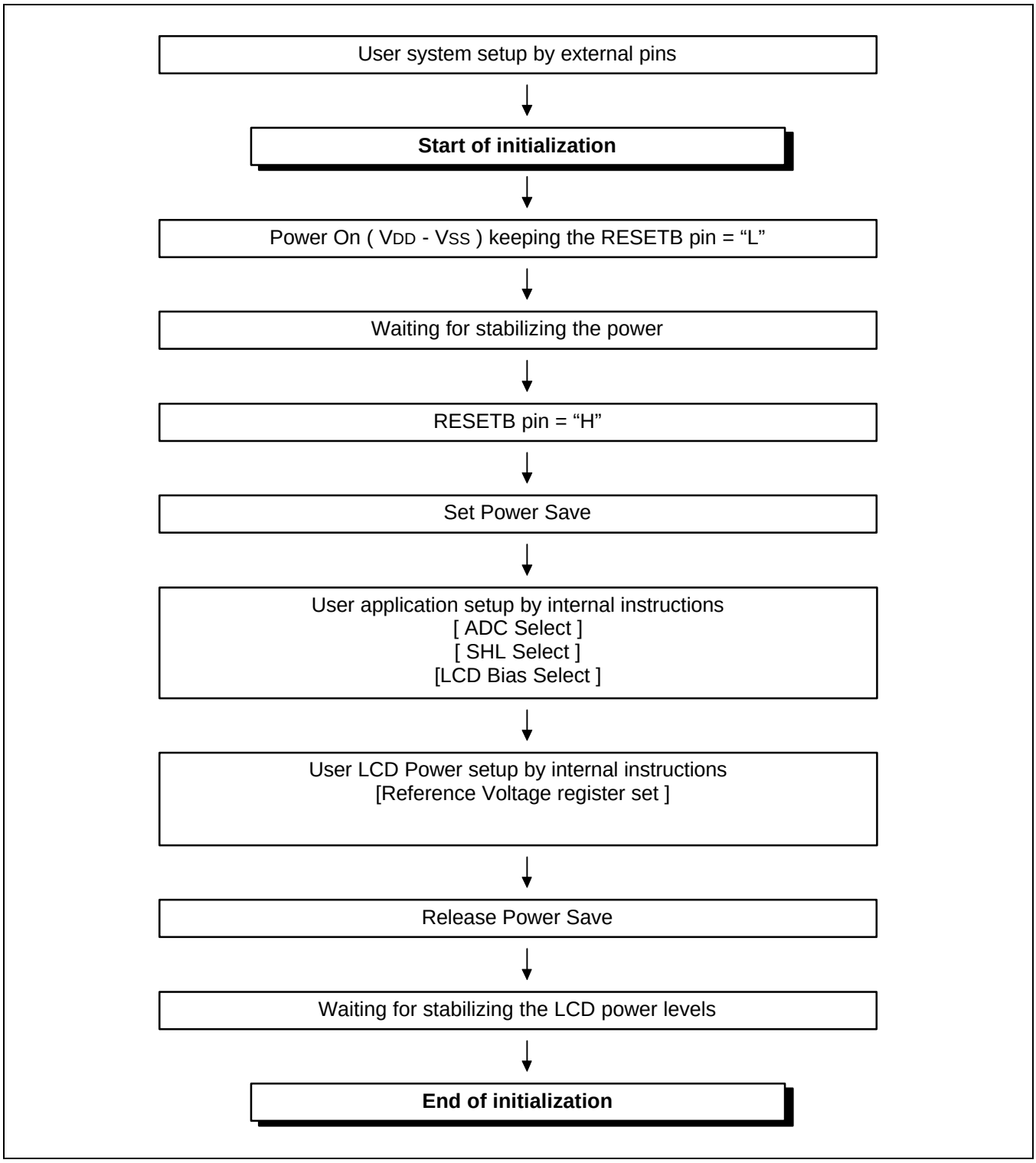


Figure 13. Initializing Without the Built-in Power Supply Circuits

— Data Displaying

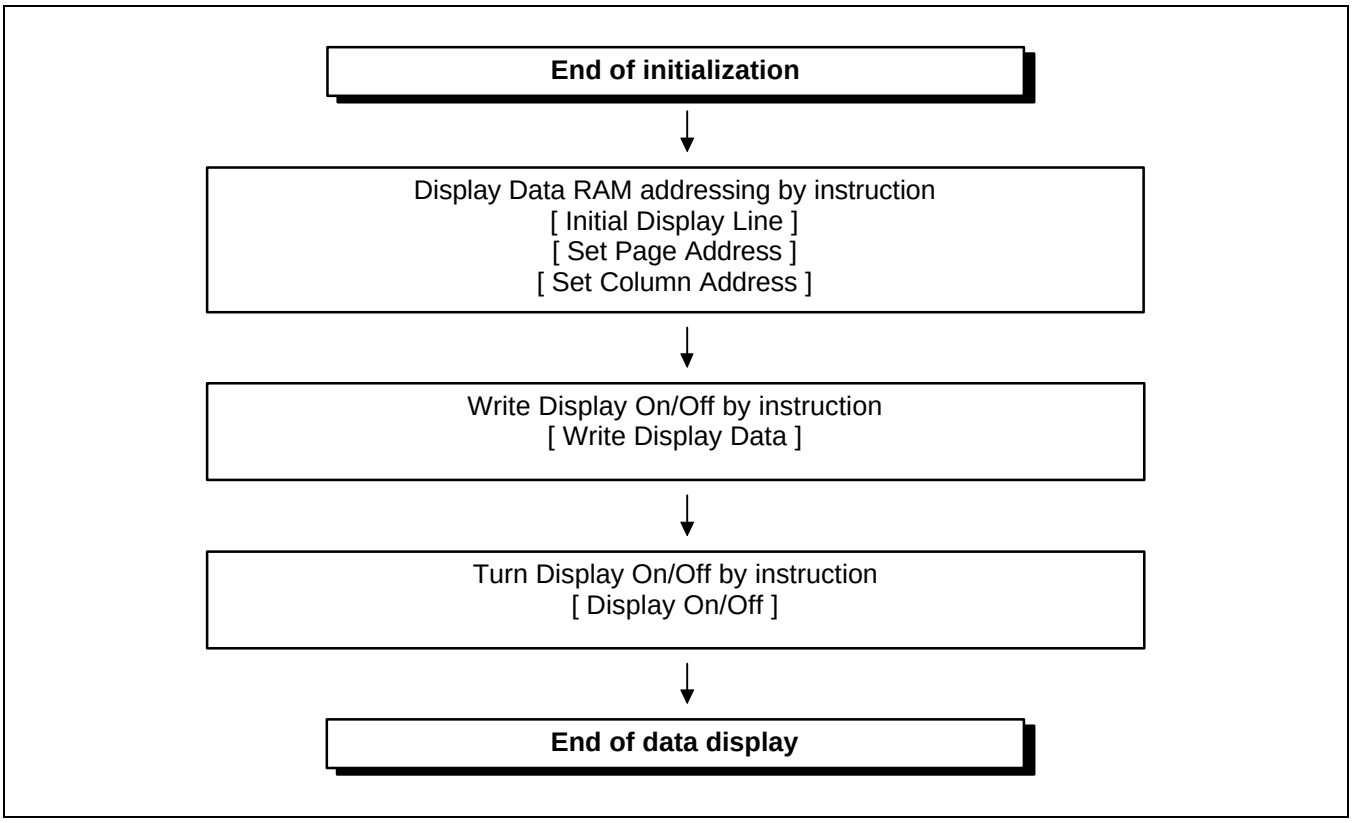


Figure 14. Data Displaying

— Power Off

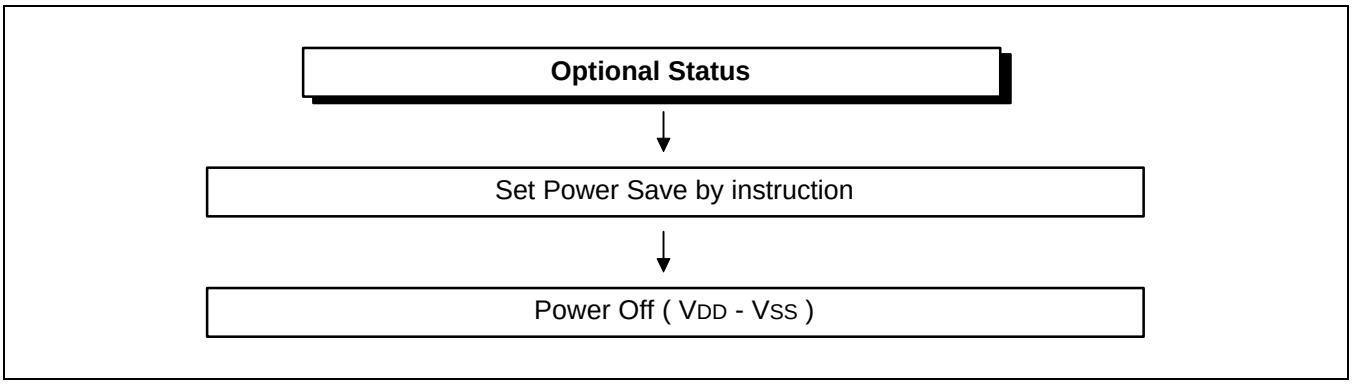


Figure 15. Power Off

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 15. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	– 0.3 to + 7.0	V
	V_{LCD}	– 0.3 to + 17	
Input voltage range	V_{IN}	– 0.3 to V_{DD} + 0.3	
Operating temperature range	T_{OPR}	– 40 to + 85	°C
Storage temperature range	T_{STR}	– 55 to +125	

NOTES:

1. V_{DD} and V_{LCD} are based on V_{SS} = 0 V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS} must always be satisfied (V_{LCD} = V0 – V_{SS}).
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 16. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Pin Used
Operating voltage (1)		V_{DD}	–	2.4	–	5.5	V	V_{DD} (1)
Operating voltage (2)		V0	–	4.0	–	15.0		V0 (2)
Input voltage	High	V_{IH}	–	0.8 V_{DD}	–	V_{DD}		(3)
	Low	V_{IL}	–	V_{SS}	–	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = – 0.5mA	0.8 V_{DD}	–	V_{DD}		(4)
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	–	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	– 1.0	–	+ 1.0	µA	(5)
Output Leakage Current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	– 3.0	–	+ 3.0		(6)
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	–	2.0	3.0	kΩ	SEGn COMn (7)
Oscillator frequency (1)	Internal	f_{OSC}	Ta = 25°C	17	22.5	27	kHz	CL (8)
	External	f_{CL}		2.13	2.81	3.37		

Table 16. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit.	Pin Used
Voltage Converter / Regulator / Follower								
Voltage converter input voltage	V_{DD}	× 2		2.4	–	5.5	V	V_{DD}
		× 3		2.4	–	5.0		
		× 4		2.4	–	3.7		
Voltage converter output voltage	VOUT	× 2/× 3/× 4 voltage conversion (no-load)		95	99	–	%	VOUT
Voltage regulator operating voltage	VOUT	–		4.0	–	15.0	V	VOUT
Voltage follower operating voltage	V0	–		4.0	–	15.0		V0 (9)
Reference voltage	V_{REF0}	T_a = 25°C	– 0.05%/°C	1.84	1.9	1.96		(10)
	V_{REF1}		– 0.2%/°C	1.94	2.0	2.06		(10)
Dynamic Current Consumption (1): When the built-In circuits is OFF (At Operate Mode).								
Dynamic current consumption (1)	I_{DD1}	V_{DD} = 3.0V, V0 – V_{SS} = 8.0V, Built-in power circuit is off, display off checker pattern		–	5	20	µA	(11)
		V_{DD} = 3.0V, V0 – V_{SS} = 8.0V, Built-in power circuit is off, display on, checker pattern		–	24	40	µA	
Dynamic Current Consumption (2): When the built-in circuits is ON (At Operate Mode).								
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, quad boosting, V0 – V_{SS} = 8.0V, Built-in power circuit is on, display off, checker pattern		–	47	70	µA	(11)
		V_{DD} = 3.0V, quad boosting, V0 – V_{SS} = 8.0V, Built-in power circuit is on, display on, checker pattern		–	75	100	µA	

Table 16. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Pin Used
Dynamic Current Consumption (3): When the built-in power is OFF (At Access Mode).							
Dynamic current consumption (3)	I_{DD3}	V_{DD} = 3.0V, V0 – V_{SS} = 8.0V, f_{cyc} = 1MHz Built-in power circuit is off	–	–	1	mA	
Current Consumption During Power Save Mode							
Sleep mode current	I_{DDS1}	During sleep	–	–	2.0	μA	
Standby mode current	I_{DDS2}	During standby	–	–	10.0	μA	

NOTES:

1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from MPU.
2. In case of external power supply is applied.
3. CS1B, CS2, RS, DB7 to DB0, E_RD, RW_WR, RESETB, MS, MI, PS, TEMPS, CL, M, DISP pins
4. DB7 to DB0, M, FRS, DISP, CL pins
5. CS1B, CS2, RS, DB7 to DB0, E_RD, RW_WR, RESETB, MS, MI, PS, TEMPS, CL, M, DISP pins
6. Applies when the DB7 to DB0, M, DISP, and CL pins are in high impedance.
7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn. R_{ON} = Δ V / 0.1 [kΩ] (Δ V: voltage change when ± 0.1[mA] is applied in the ON status.)
8. See Table 17 for the relationship between oscillation frequency and frame frequency.
9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
11. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU. The current consumption, when the built-in power supply circuit is on or off. The current flowing through voltage regulation resistors (Rb and Ra) is not included. It does not include the current of the LCD panel capacity, wiring capacity, etc.

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Table 17. The Relationship Between Oscillation Frequency and Frame Frequency

DUTY Ratio	Item	f_{CL}	f_M	Remark
1/33	On-chip oscillator circuit is used	f_{OSC} / 8	f_{OSC} / (16 × 33)	• f_{OSC} = oscillation frequency • f_{CL} = display clock frequency • f_M = LCD AC signal frequency
	On-chip oscillator circuit is not used	External input (f_{CL})	f_{CL} / (2 × 33)	

AC CHARACTERISTICS

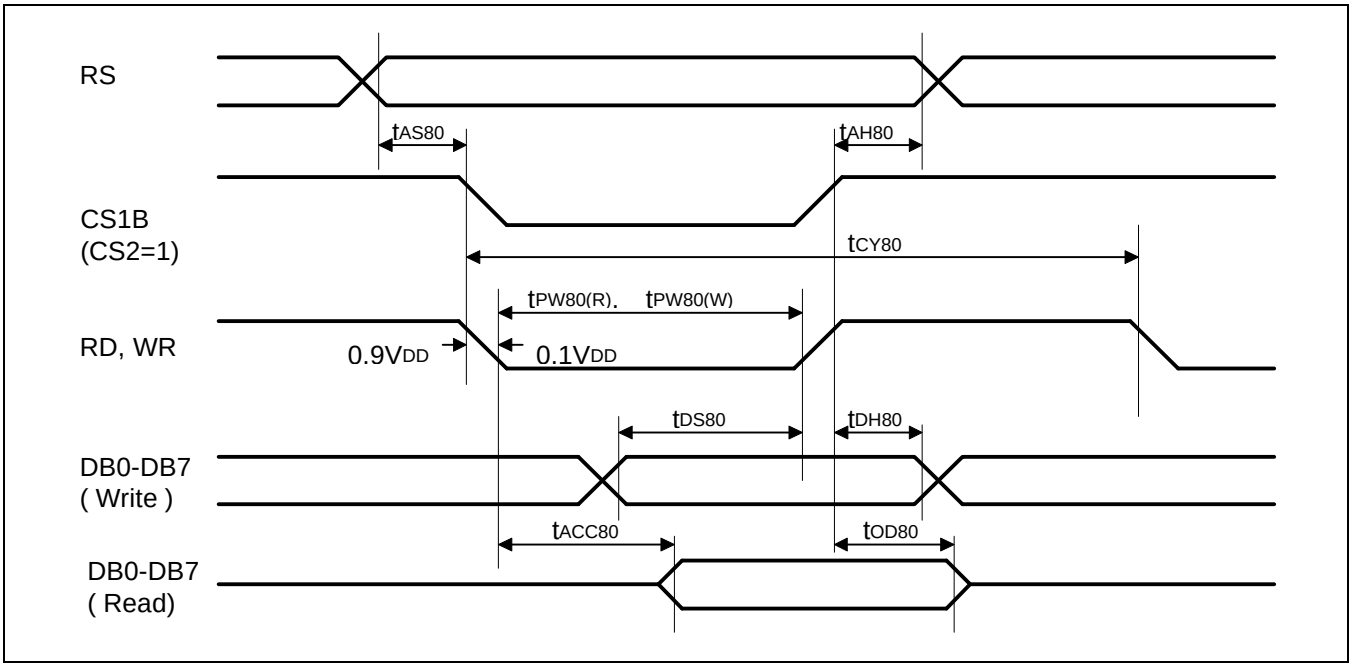


Figure 16. Read/Write Characteristics (8080-Series Microprocessor)

(V_{DD} = 2.4V to 3.3V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	13 17	–	–	ns	–
System cycle time	RS	t_{CY80}	400	–	–	ns	–
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	55	–	–	ns	–
Pulse width (RD)	E_RD	$t_{PW80(R)}$	125	–	–	ns	–
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}	35 13	–	–	ns	–
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	125 90	ns ns	C_L = 100pF

(V_{DD} = 4.5V to 5.5V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	10 10	–	–	ns	–
System cycle time	RS	t_{CY80}	150	–	–	ns	–
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	25	–	–	ns	–
Pulse width (RD)	E_RD	$t_{PW80(R)}$	65	–	–	ns	–
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}	18 10	–	–	ns	–
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	65 45	ns ns	C_L = 100pF

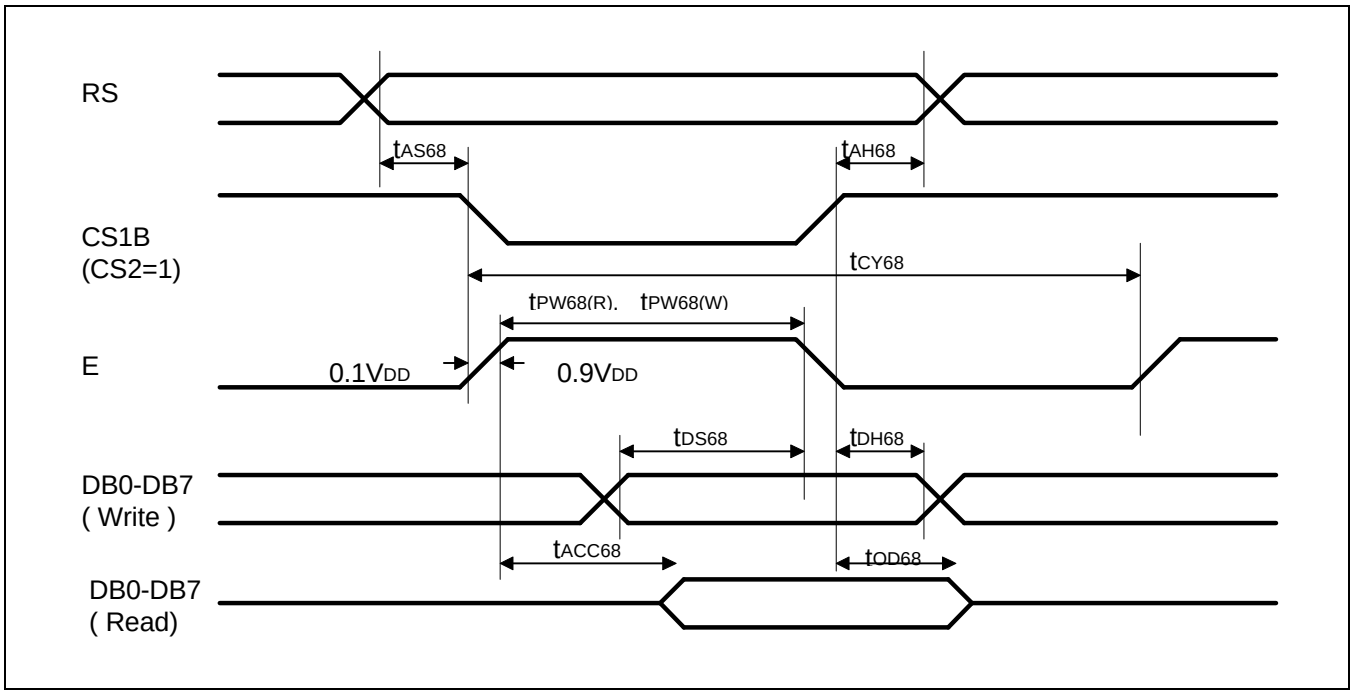


Figure 17. Read/Write Characteristics (6800-Series Microprocessor)

(V_{DD} = 2.4V to 3.3V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	13 17	–	–	ns	–
System cycle time		RS	t_{CY68}	400	–	–	ns	–
Data setup time Data hold time		DB0 to DB7	t_{DS68} t_{DH68}	35 13	–	–	ns	–
Access time Output disable time		–	t_{ACC68} t_{OD68}	- 10	– –	125 90	ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	125 55	–	–	–	–

(V_{DD} = 4.5V to 5.5V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	10 10	–	–	ns	–
System cycle time		RS	t_{CY68}	150	–	–	ns	–
Data setup time Data hold time		DB0 to DB7	t_{DS68} t_{DH68}	18 10	–	–	ns	–
Access time Output disable time			t_{ACC68} t_{OD68}	– 10	– –	65 45	ns ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	65 25	–	–	–	–

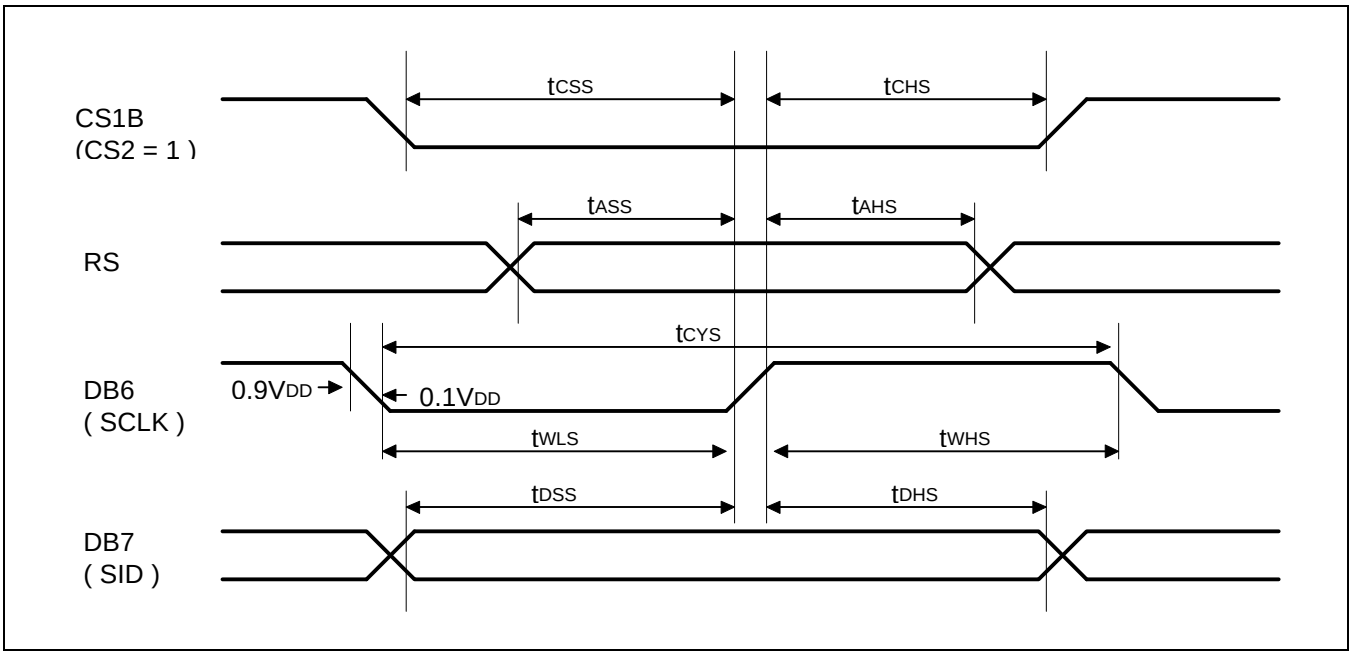


Figure 18. Serial Interface Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta =– 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	450 180 135	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	90 360	–	–	ns
Data setup time Data hold time	DB7(SID)	t_{DSS} t_{DHS}	90 90	–	–	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	55 180	–	–	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	225 90 70	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	45 180	–	–	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	45 45	–	–	ns
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	25 90	–	–	ns

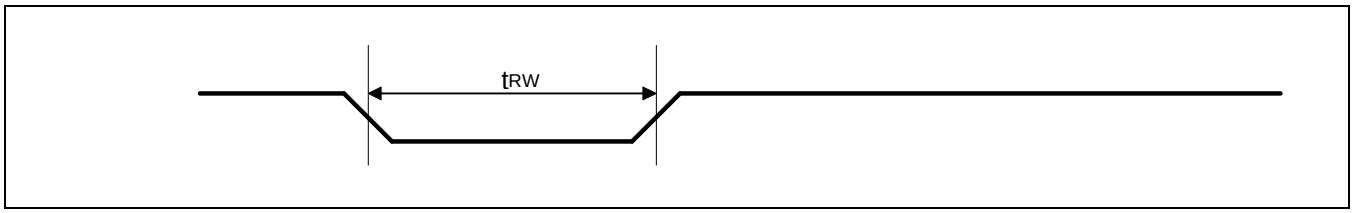


Figure 19. Reset Input Timing

(V_{DD} = 2.4 V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	900	–	–	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	450	–	–	ns

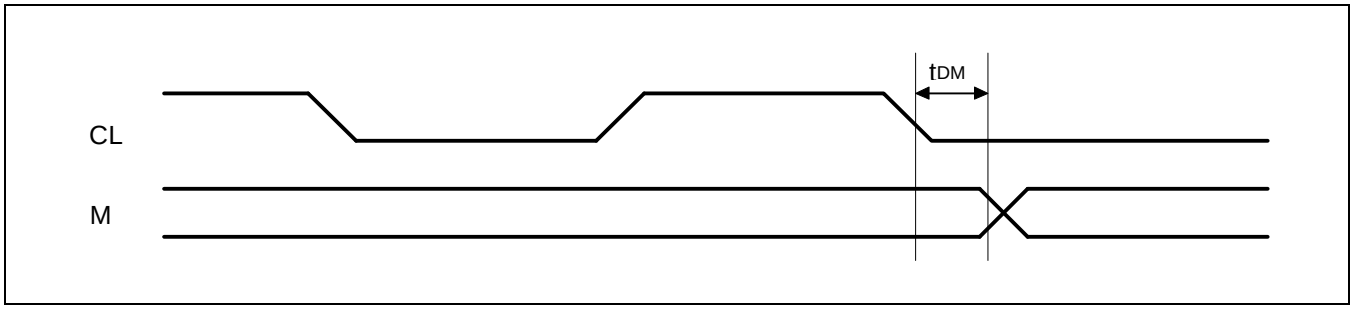


Figure 20. Display Control Output Timing

(V_{DD} = 2.4 V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	13	70	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	10	35	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

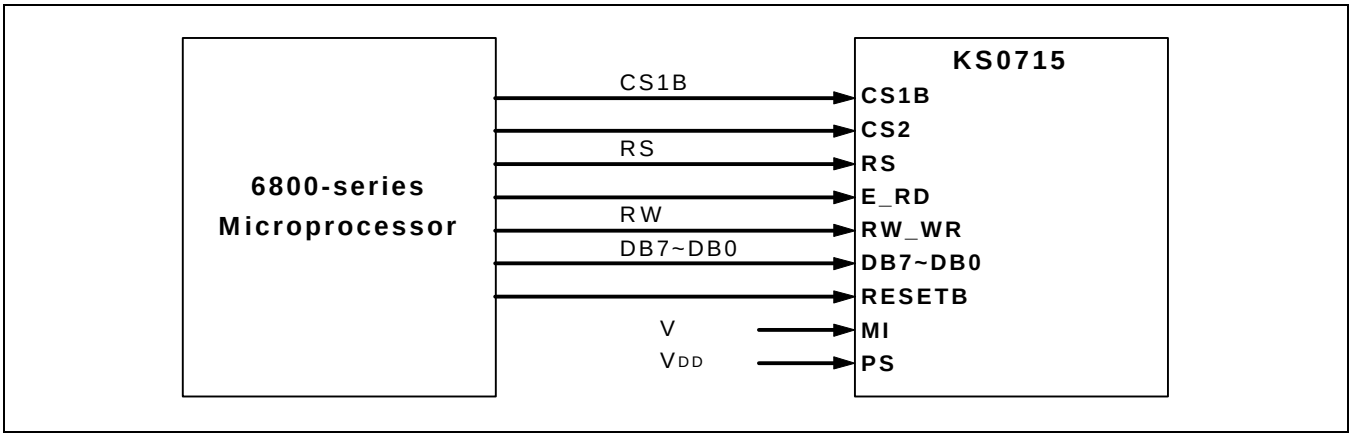


Figure 21. Interfacing with the 6800_Series (PS = “H”, MI = “H”)

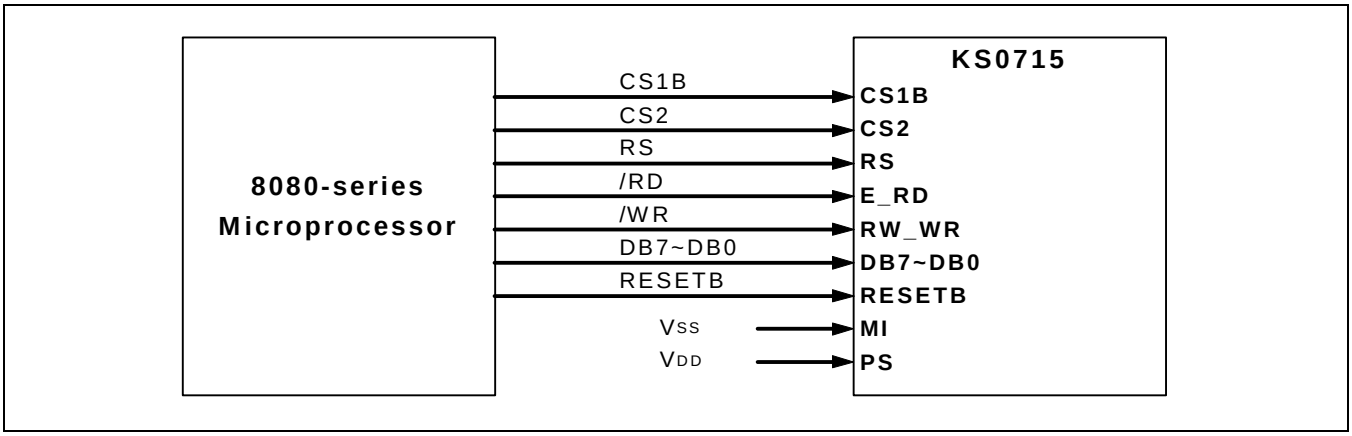


Figure 22. Interfacing with the 8080-Series (PS = “H”, MI = “L”)

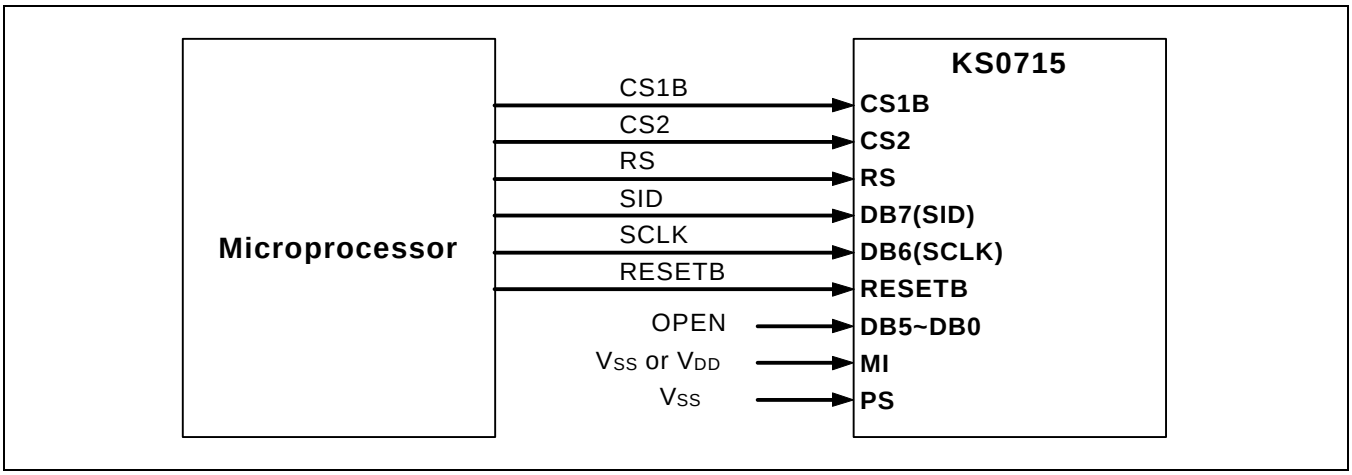
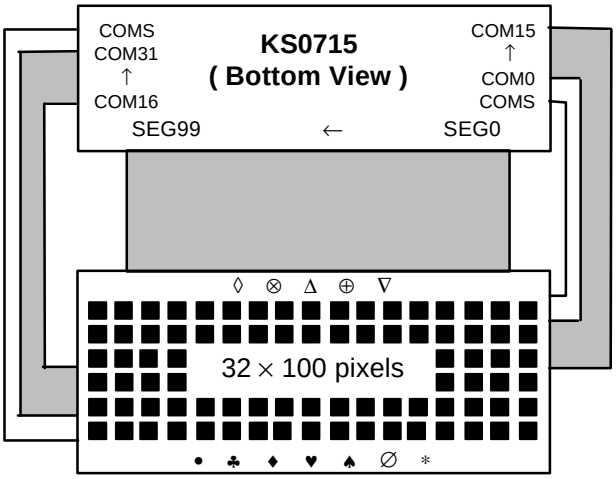


Figure 23. Serial Interface (PS = “L”, MI = “H/L”)

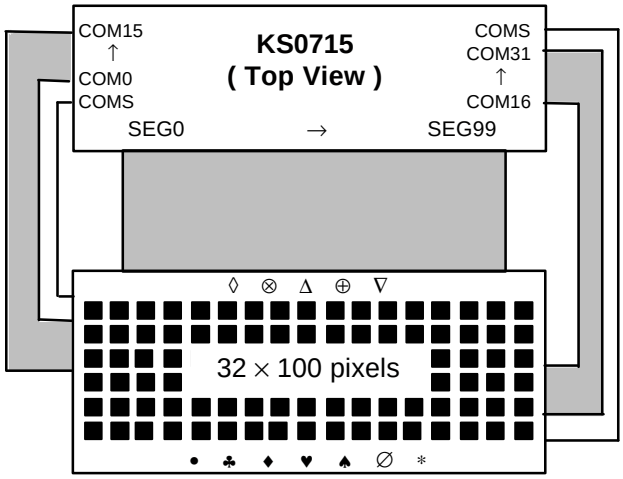
CONNECTIONS BETWEEN KS0715 AND LCD PANEL

Single-Chip Structure (1/33 Duty Configurations)

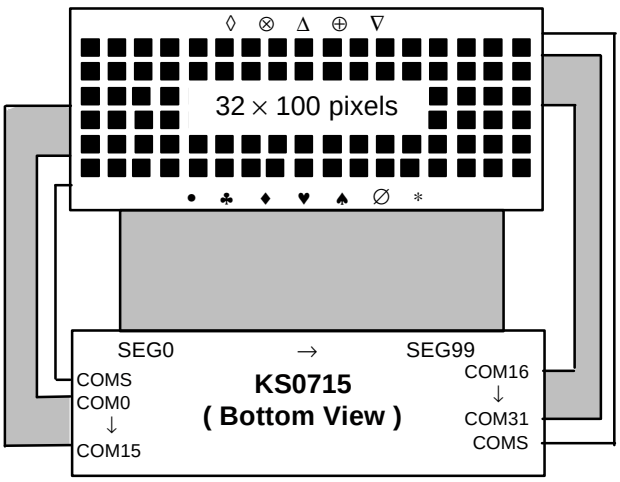
¨ **SHL = 0, ADC = 1**



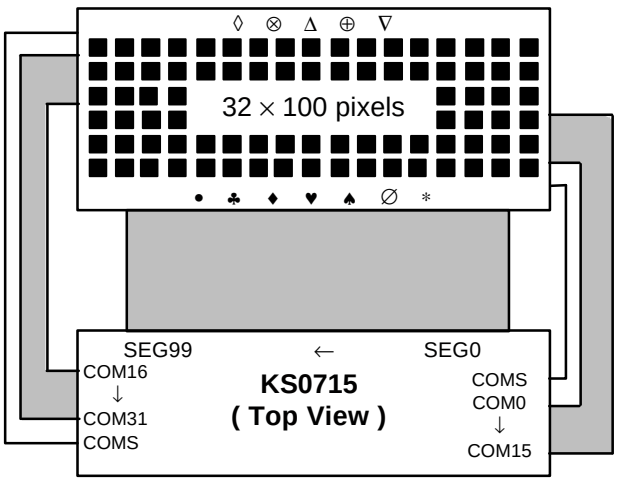
¨ **SHL = 0, ADC = 0**



¨ **SHL = 1, ADC = 0**



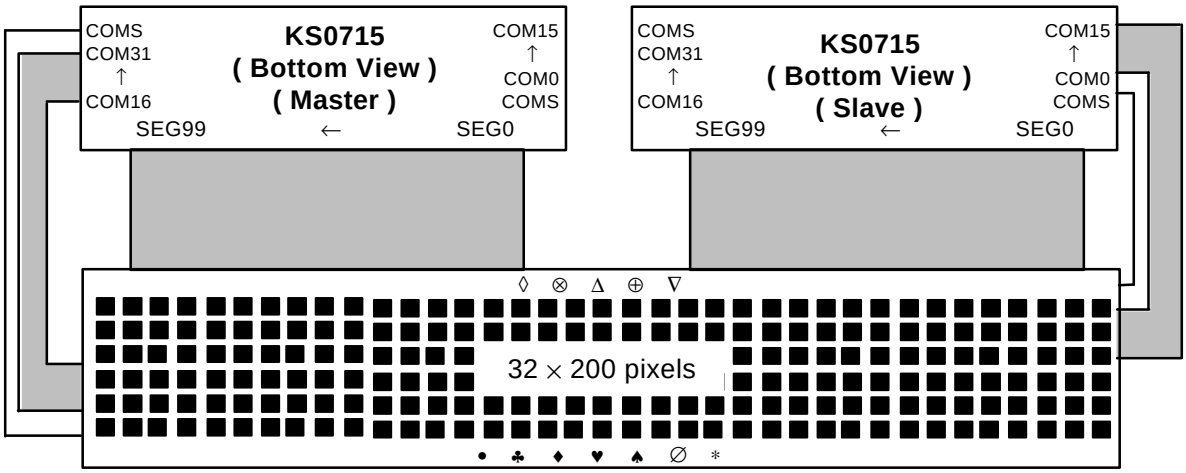
¨ **SHL = 1, ADC = 1**



SAMSUNG ELECTRONICS

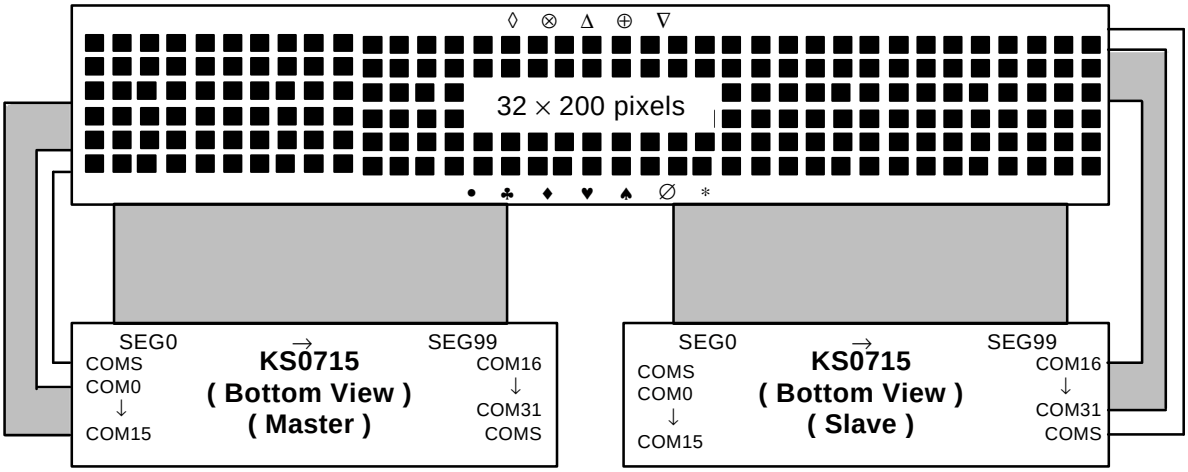
Multi-Chip Structure

¨ **SHL = 0, ADC = 1**



- Connect the following Pins of two chips each other :
  - Display Clock Pins : CL, M
  - Display Control Pin : DISP
  - LCD Power : V0, V1, V2, V3, V4

¨ **SHL = 1, ADC = 0**



- Connect the following Pins of two chips each other :
  - Display Clock Pins : CL, M
  - Display Control Pin : DISP
  - LCD Power : V0, V1, V2, V3, V4

KS0715 TCP PIN LAYOUT (SAMPLE)