SGS-THOMSON MICROELECTRONICS

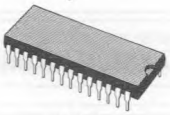
L3000
L3090

SUBSCRIBER LINE INTERFACE CIRCUIT KIT

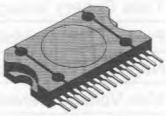
- PROGRAMMABLE DC FEEDING RESISTANCE and LIMITING CURRENT (42/62mA)
- FOUR OPERATING MODES : POWER DOWN, STAND-BY, CONVERSATION, RINGING
- SIGNALLING FUNCTION (off-hook/GND-Key)
- QUICK OFF-HOOK DETECTION IN CVS FOR LOW DISTORTION (< 1 %) DIAL PULSE DETECTION
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) and RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- PARALLEL LATCHED DIGITAL INTERFACE (5 pins)
- LOW NUMBER of EXTERNAL COMPONENTS WITH STANDARD TOLERANCE ONLY : 9 1 % RESISTORS and 5 10-20 % CAPACITORS (for 600 ohm appl.)
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20 dB at 10 Hz ; 40 dB at 1 KHz)
- INTEGRATED THERMAL PROTECTION

This kit is fabricated using a 140 V Bipolar technology for L3000 and a 12 V Bipolar I2L technology for L3090.

This kit is specially suitable to Private Automatic Branch Exchange (PABX).



DIP28



FLEXIWATT 15

ORDER CODES : L3090 (DIP28)
L3000 (FLEXIWATT)

PIN CONNECTION

DESCRIPTION

The SLIC KIT (L3000/L3090) is a set of solid state devices designed to integrate many of the functions needed to interface a telephone line. It consists of 2 integrated devices ; the L3000 line interface circuit and the L3090 control unit.

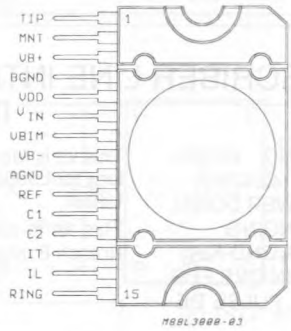
The kit implements the main features of the BORSHT functions :

- Battery feed (balance mode)
- Ringing
- Signalling
- Hybrid

The SLIC KIT injects the ringing signal in balanced mode and requires a positive supply voltage of typically + 72 V to be available on the subscriber card.

The L3000/L3090 KIT generates the ringing signal internally, avoiding the requirement for expensive external circuitry. A low level 1.5 V_{rms} input is required. (This can be provided by the combo).

PIN CONNECTION (continued)



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_b-	Negative Battery Voltage	– 80	V
V_b+	Positive Battery Voltage	80	V
$\|V_b\text{-}\| + \|V_b\text{+}\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5	V
$\|V_{agnd} - V_{bgnd}\|$	Max Voltage Between Analog Ground and Battery Ground	5	V
T_j	Max Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

L3000 HIGH VOLTAGE

R_{thjc}	Max Resistance Junction to Case	4	°C/W
R_{thja}	Max Resistance Junction to Ambient	50	°C/W

L3090 LOW VOLTAGE

R_{thja}	Max Resistance Junction to Ambient	80	°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range	0		70	°C
V_b-	Negative Battery Voltage	– 70	– 48	–24	V
V_b+	Positive Battery Voltage	0	+ 72	+ 75	V
$\|V_b\text{-}\| + \|V_b\text{+}\|$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current (I_L + I_T)			85	mA

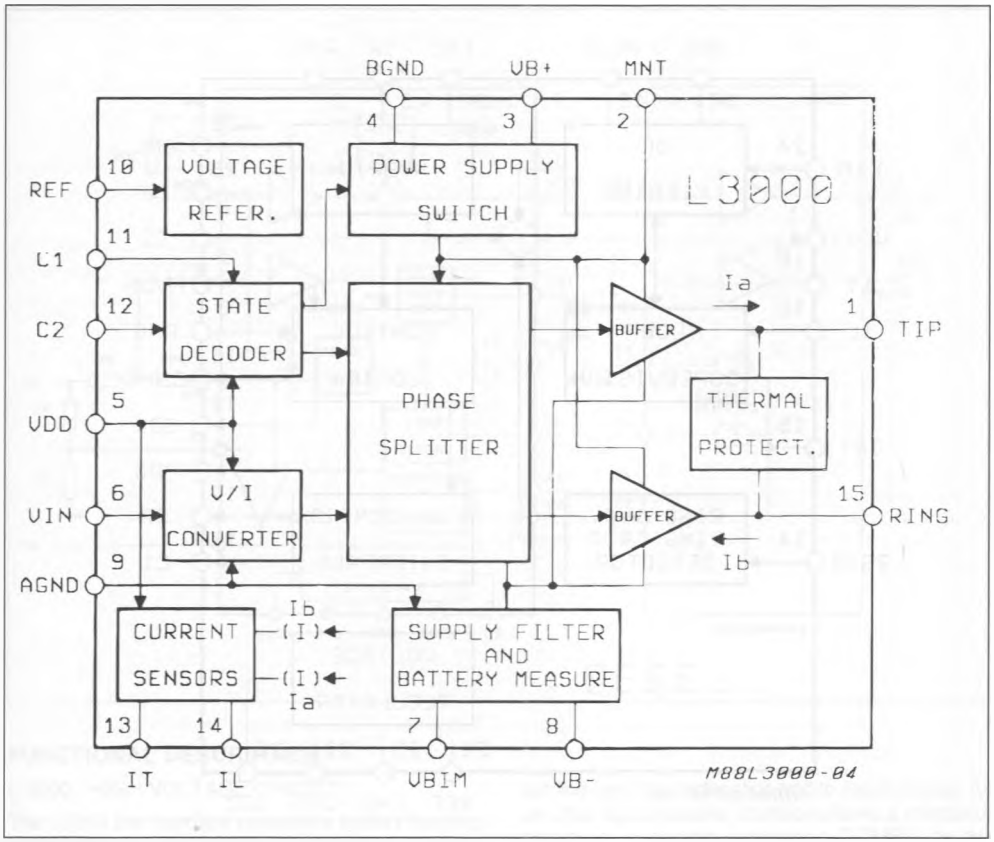
PIN DESCRIPTION (L3000)

N°	Name	Description
1	TIP	A line termination output with current capability up to 100 mA (I_a is the current sourced from this pin).
2	MNT	Positive Supply Voltage Monitor
3	V_B+	Positive Battery Supply Voltage
4	BGND	Battery Ground Relative to the V_B+ and the V_B- supply Voltages. It is also the reference ground for TIP and RING signals.
5	V_{DD}	Positive Power Supply + 5 V
6	VIN	2 Wire unbalanced Voltage Input.
7	VBIM	Output Voltage without current capability, with the following functions : – give an image of the total battery voltage scaled by 40 to the low voltage part. – filter by an external capacitor the noise on V_B-
8	V_B-	Negative Battery Supply Voltage
9	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets internal circuit bias current.
11	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	IL	Scaled longitudinal line current signal. $IL = \frac{I_a - I_b}{100}$
15	RING	B line termination output with current capability up to 100 mA (I_b is the current sunk into this pin).

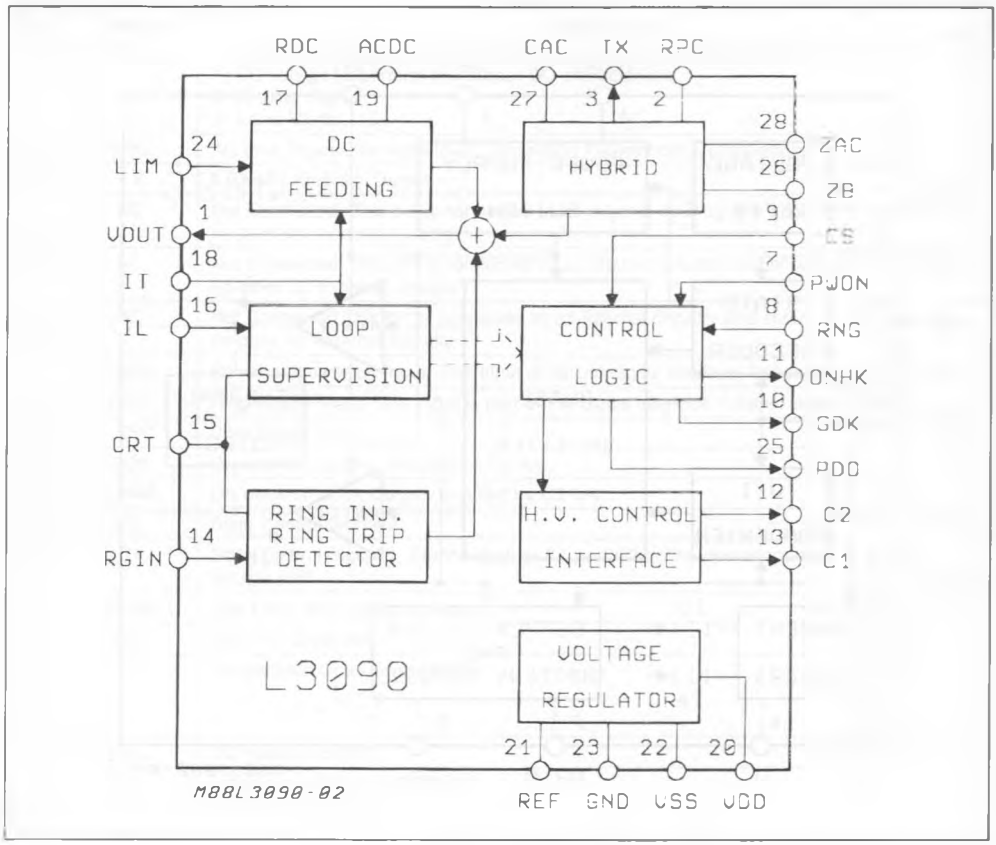
PIN DESCRIPTION (L3090)

N°	Name	Description
1	VOUT	Two wire unbalanced output carrying out the following signals reduced by 40 1) DC voltage to perform the proper DC characteristic. 2) Ringing Signal 3) Voice Signal
2	RPC	AC Line Impedance Adjustment. Protection Resistances Compensation.
3	TX	Transmit Amplifier Output
4	NC	Not Connected. This pin is connected to an internal circuitry and should not be used as a tie-point for external circuitry.
5	NC	Not Connected. This pin is connected to an internal circuitry and should not be used as a tie–point for external circuitry.
6	NC	Not Connected.This pin is connected to an internal circuitry and should not be used as a tie-point for external circuitry.
7	PWON	Power on/power off Input. This input is part of digital interface. Loaded when CS is low.
8	RNG	Ring Enable Input. This input is part of the digital interface. Loaded when CS is low.
9	CS	Chip Select Input
10	GDK	Ground Key Output. Enabled by CS low.
11	ONHK	On Hook/off Hook Output. Enabled by CS low.
12	C2	State Control Signal 2
13	C1	State Control Signal 1. Combination of C1 and C2 define operating mode of the high voltage part.
14	RGIN	Low Level Ringing Signal Input.
15	CRT	Ring Trip Detection
16	IL	Longitudinal Line Current Input $IL = \frac{I_a - I_b}{100}$
17	RDC	DC Feeding System
18	IT	Transversal Line Current Input $IT = \frac{I_a + I_b}{100}$
19	ACDC	AC – DC Feedback Input
20	VDD	Positive Supply Voltage, + 5 V
21	REF	Bias Setting Pin
22	VSS	Negative Supply Voltage, – 5 V
23	GND	Analog and Digital Ground
24	LIM	Limiting Current Selection Input
25	PDO	Power Down Output. Driving the high voltage part L3000 through its bias resistor RH.
26	ZB	TX Amplifier Negative Input. Performing the two to four wire conversion.
27	CAC	AC Feedback Input
28	ZAC	AC Line Impedance Synthesis

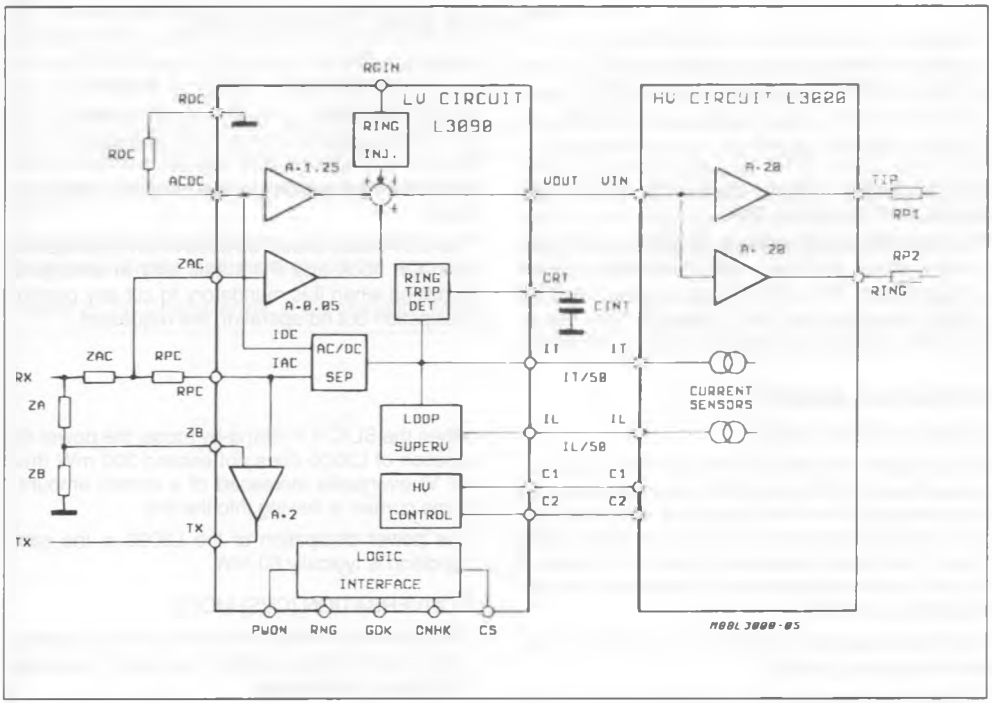
L3000 BLOCK DIAGRAM



L3090 BLOCK DIAGRAM



FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

L 3000 - HIGH VOLTAGE CIRCUIT

The L3000 line interface provides a battery feeding for telephone lines and ringing injection. The IC contains a state decoder that under external control can force the following operational modes : stand-by, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor to VDD.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000 amplifies both the AC and DC signals entering at pin 6 (VIN).

Separate grounds are provided :

- Analog ground as a reference for analog signals
- Battery ground as a reference for the output stages

L3090 - LOW VOLTAGE CIRCUIT

The L3090 Low Voltage Control Unit controls the L3000 line interface module providing set up data to set line feed characteristics and to inject ringing. An on chip digital parallel interface allows a microprocessor or a second generation COMBO as the TS5070 to control all the operations.

L3090 defines working states of line interface and also informs the controller about line status.

WORKING STATES OF THE KIT

In order to carry out the different possible operations, the SLIC kit has several different working states. Each state is defined by the voltage respectively applied by pins 12 and 13 of L3090 to the pins 12 and 11 of L3000.

Three different voltage levels (5, 0, + 5) are available at each connection, so defining nine possible states as listed in tab. 1.

Appropriate combinations of two pins define three of the four possible status of the kit, that are :

a) Stand-by (SBY)

b) Conversation (CVS)

c) Ringing (RING)

Table 1.

		Pin 12 of L3090 / Pin 12 of L3000		
		+ 5	0	– 5
Pin 13 of L3090	+ 5	Stand–by	Conversation	Not Used
———	0	Not Used	Not Used	Not Used
Pin 11 of L3000	– 5	Not Used	Ringing	Not Used

The fourth status, Power down (PD), is set by the output pin PDO of the L3090.

The main difference between Stand-by and Power down is that in SBY the power consumption on the voltage battery VB– (–48 V) is reduced but the SLIC can still recognize yet the On hook/Off hook status. In PD the power consumption on VB– is reduced to zero, but none operation can be performed by the SLIC.

The SBY status should be used when the telephone is in On hook and PD status only in emergency condition when it is mandatory to cut any possible dissipation but no operation are requested.

OPERATING MODES

STAND-BY (SBY) MODE

In this mode (PWON=OV RNG=OV) the bias currents of both L3000 and L3090 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them. The current supplied to the line is limited at 12 mA, and the slope of the DC characteristic corresponds to 2xRFS.

The AC characteristic in Stand-by corresponds to a low impedance (2xRP).

In Stand-by mode the line voltage polarity is just in direct condition, that is the TIP wire more positive than the RING one.

When the SLIC is in Stand-by mode, the power dissipation of L3000 does not exceed 200 mW (from 48 V) eventually increased of a certain amount if some current is flowing into the line.

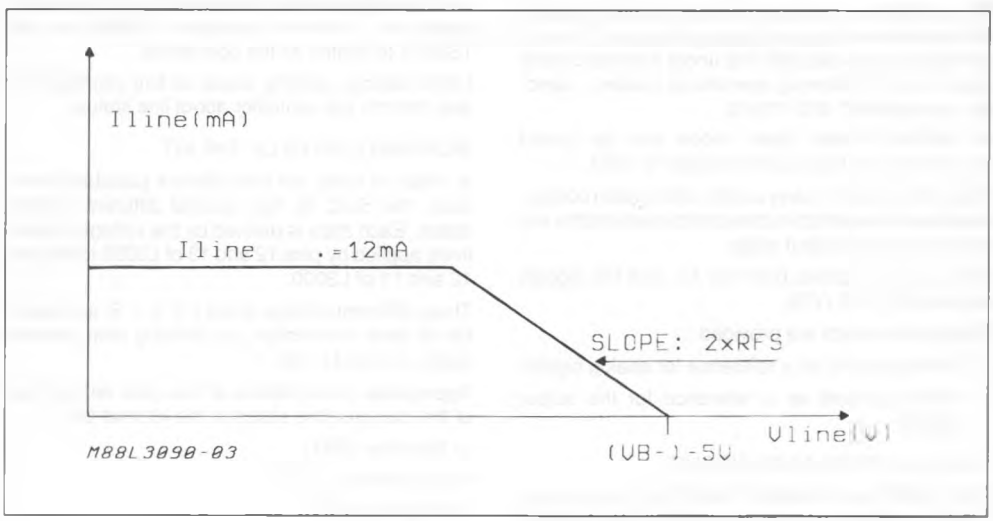
The power dissipation of the L3090 in the same condition is typically 60 mW.

CONVERSATION (CVS) MODE

This operating mode is set by the control processor when the Off hook condition has been recognized (PWON=+5V RNG=0V).

As far as the DC Characteristic is concerned two different feeding conditions are present :

Figure 1 : DC Characteristic in Stand-by Mode.



a) Current limiting region : the DC impedance of the SLIC is very high (> 20 KΩ) and therefore the system works like a current generator. The input pin LIM of the L3090 selects the value of the limiting current : 62 mA (LIM=0V) or 42 mA (LIM=+5V)

b) A standard resistive feeding mode : the characteristic is equal to a battery voltage (VB–) minus 5 V, in series with a resistor, whose value is set by external components (see external component list of L3090).

Switching between the two regions is automatic without discontinuity, and depends on the loop resistance. Fig. 2 shows the DC characteristic in conversation mode.

Fig. 3 shows the line current versus loop resistance for two different battery values and RFS = 200 Ω.

The allowed maximum loop resistance depends on the values of the battery voltage (VB), on the RFS and on the value of the longitudinal current (I_{GDK}). With a battery voltage of 48 V, RFS = 200 Ω and I_{GDK} = 0 mA, the maximum loop resistance is over 3000 Ω and with I_{GDK} = 20 mA is about 2000 Ω (see Application Note on maximum loop resistance for L3000/L3090 SLIC KIT).

Figure 2 : DC Characteristic in Conversation Mode.

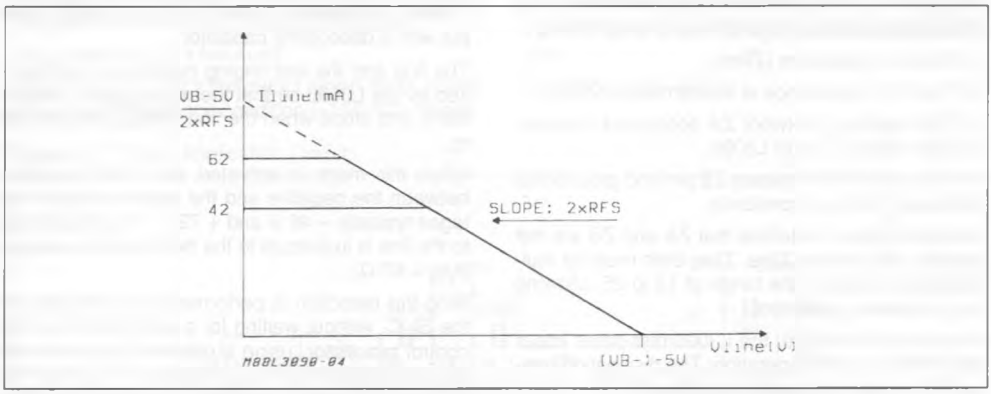
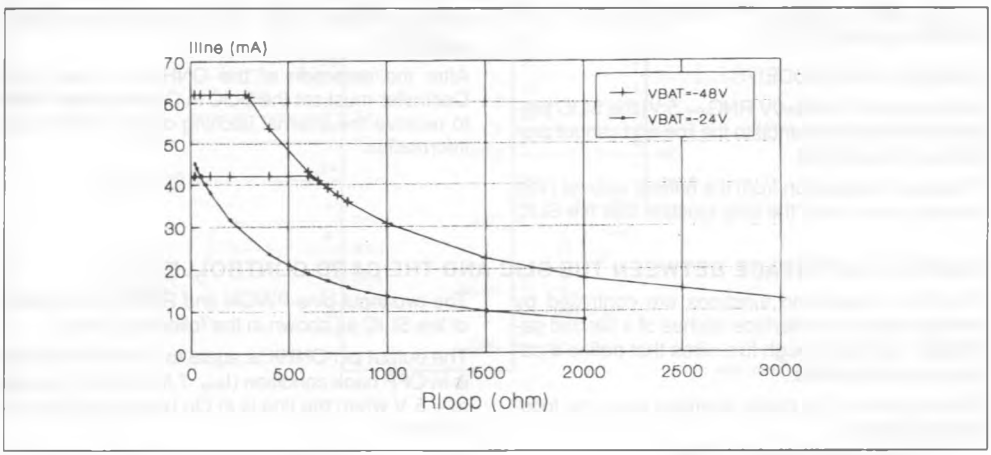


Figure 3 : Line Current Versus Loop Resistance - RFS = 200 Ω ; Limiting Currents : 42 ; 62 mA.



In conversation mode the AC impedance at the line terminals is synthetized by the external components ZAC and RP, according to the following formula :

$$ZML = \frac{ZAC}{25} + 2 \times RP$$

Depending on the characteristic of the ZAC network, ZML can be either a pure resistance or a complex impedance. This allows for ST SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheatstone bridge, the branches of which being :

1) The line impedance (Zline),

2) The SLIC impedance at line terminals (ZML),

3) The balancing network ZA connected between RX input and ZB pin of L3090,

4) The network ZB between ZB pin and ground that shall copy the line impedance.

It is important to underline that ZA and ZB are not equal to ZML and to Zline. They both must be multiplied by a factor in the range of 10 to 25, allowing use of smaller capacitors.

In conversation mode, the L3000 dissipates about 500 mW for its own operation. The dissipation related to the current supplied to the line shall be added, in order to get the total dissipation.

In the same condition the power dissipation of L3090 is typically 100 mW.

POWER DOWN MODE

In this mode (PWON=0V RNG=+ 5 V) the SLIC presents an high impedance to the line and cannot provide any line current.

The power dissipation from the battery voltage (VB) is equal to zero and the only function that the SLIC can perform is to recognize a command on PWON and RNG input pins and change its operating mode.

In this condition the power dissipation of the L3090 is typically 60 mW.

RINGING MODE

When the ringing function is selected by the control processor (PWON = + 5 V, RNG = + 5 V), a low level signal (1.5 Vrms) with a frequency in the range from 16 to 70 Hz, permanently applied to the L3090 (pin RGIN), is amplified and injected in balanced mode into the line through the L3000 with a super imposed DC voltage of 22 V.

This low level sinewave can be obtained also from COMBO connecting RGIN pin to RX COMBO output with a decoupling capacitor.

The first and the last ringing cycles are synchronized by the L3090 so that the ringing signal always starts and stops when the line voltage crosses zero.

When this mode is activated, the L3000 operates between the negative and the positive battery voltages typically – 48 V and + 72 V. The impedance to the line is just equal to the two external resistors (typ. = 60 Ω).

Ring trip detection is performed autonomously by the SLIC, without waiting for a command from the control processor, using a patented system which allows detection during a ringing burst ; when the off-hook condition is detected, the SLIC stops the ringing signal and forces the Conversation Mode.

In this condition, if CS = 0 V, the output pin ONHK goes to 0 V.

After the detection of the ONHK = 0, the Card Controller must set the SLIC in Conversation Mode to remove the internal latching of the On/Off hook information.

CONTROL INTERFACE BETWEEN THE SLIC AND THE CARD CONTROLLER

The SLIC states and functions are controlled by microprocessor or interface latches of a second generation combo through five wires that define a parallel digital interface.

The five pins of the digital interface have the following functions :

- Power on/off input (PWON)
- Ring enable input (RNG)
- Chip select input (CS)
- On hook/Off hook detection output (ONHK)
- Ground key detection output (GDK)

The two input pins PWON and RNG set the status of the SLIC as shown in the following Table.

The output pin ONHK is equal to 0 V when the line is in OFF hook condition (I_{line} 7,5 mA) and is equal to + 5 V when the line is in On hook condition (I_{line} 5,5 mA).

The output pin GDK monitors the ground key functions.

When I_{GDK} (longitudinal current) > 12 mA, pin GDK set to 0 V

		PWON PIN	
		0 V	+ 5 V
RNG PIN	0 V	Stand–by	Conversation
	+ 5 V	Power Down	Ringing

When I_{GDK} < 8 mA, pin GDK set to + 5 V

The longitudinal current (I_{GDK}) is defined as follows :

$$I_{GDK} = \frac{I_A - I_B}{2}$$

Where I_A is the current sourced from pin TIP and I_B is the current sunk into pin RING.

The CS input pin allows to connect the I/O pins of the digital interfaces of many SLIC together.

It is possible to do it because :

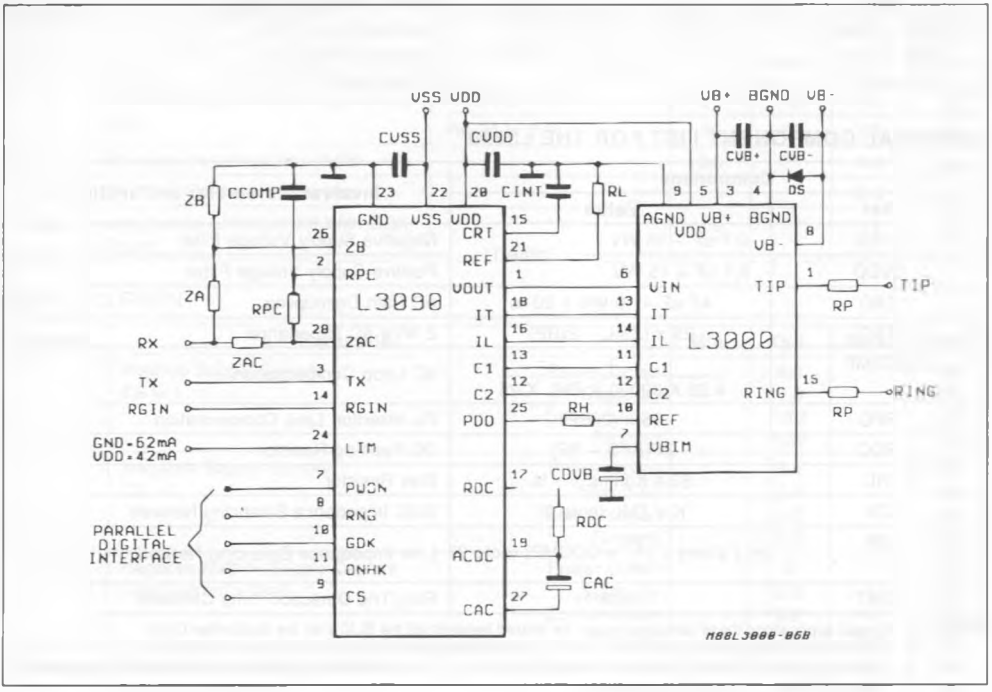
When the CS = + 5 V the output pins (ONHK, GDK) are in high impedance condition (>100 KΩ). The signals present at the input pins (PWON and RNG) are not transfered into the SLIC.

When the CS = 0 V the output pins change in function of the values of the line current (I_{line}) and the longitudinal current (I_{GDK}). The operating status of the SLIC are set by the voltage applied to the input pins.

The rising edge of the CS signal latches the signal applied to the input pins. The status of the SLIC will not change until the CS signal will be again equal to zero.

See timings fig. 5 & 6.

Figure 4 : Typical Application Circuit.



EXTERNAL COMPONENTS LIST

To set up the SLIC kit into operation, the following parameters have to be defined :

- The DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common value for RFS are 200, 400 or 500).
- The AC input/output SLIC impedance at line terminals, ZML, to which the return loss measurement is refered. It can be real (typically 600Ω) or complex.
- The equivalent AC impedance of the line Zline used for evaluation of the trans-hybrid loss (2/4 wire conversion). It is usually a complex impedance.
- The frequency of the ringing signal Fr (SLIC can work with this frequency ranging from 16 to 68 Hz).
- The value of the two resistors RP in series with the line terminals : main purpose of the a.m. resistors is to allow primary protection to fire. A minimum value of 30Ω for each side is suggested.

With these assumptions, the following component list is defined :

EXTERNAL COMPONENT LIST FOR THE L3000

Component		Involved Parameter or Function
Ref	Value	
RH	24.9 Kohms ± 2 %	Bias Resistor
RP	30 to 100 ohm	Line Series Resistor
CDVB	47 uF – 20 WV ± 20 %	Battery Voltage Rejection
CVB + (note 1)	0,1 uF – 100 WV ± 20 %	Positive Battery Filter
CVB – (note 1)	0, 1 uF – 100 WV ± 20 %	Negative Battery Filter
DS (note 1)	BAT 49	Protective Shottky Diode

EXTERNAL COMPONENT LIST FOR THE L3090

Component		Involved Parameter or Function
Ref	Value	
CVSS	0,1 uF – 15 WV (note 1)	Negative Supply Voltage Filter
CVDD	0,1 uF – 15 WV	Positive Supply Voltage Filter
CAC	47 uF – 10 WV ± 20 %	AC Path Decoupling
ZAC	25 x (ZML – 2xRP)	2 Wire AC Impedance
CCOMP	$\frac{1}{6.28 \times 30000 \times ZML \times 25}$	AC Loop Compensation
RPC	25 x (2xRP)	R_P Insertion Less Compensation
RDC	2x (RFS – RP)	DC Feeding Resistor
RL	63.4 Kohms ± 1 %	Bias Resistor
ZA	K x ZML (note 2)	SLIC Impedance Balancing Network
ZB	(K x Zline) // ($\frac{25}{K}$ x CCOMP) (note 3)	Line Impedance Balancing Network
CINT	(note 4)	Ring Trip Detection Time Constant

Notes : 1. In most applications these components can be shared between all the SLIC's on the Subscriber Card.
2. The structure of this network shall copy the SLIC output impedance multiplied by a factor K=10 to 25.
3. The structure of this network shall copy the line impedance, Z line, multiplied by a factor K=10 to 25 and compensate the effect of CCOMP on transhybrid rejection.
4. The CINT value depends on the ringing frequency Fr :

Fr [Hz]	16/18	19/21	22/27	28/32	33/38	39/46	47/55	56/68
CINT [nF]	680	560	470	390	330	270	220	180

The CINT value can be optimized experimentally for each application choosing the lower value that in correspondance of the lower ringing frequency, the minimum line lenght and the higher number of ringers doesn't produce false off-hook detection.

ELECTRICAL CHARACTERISTICS

(VDD = + 5 V ; VSS = 5 V ; VB + = + 72 V ; VB – = – 48 V ; Tamb = + 25 °C)

STANDBY

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
VLS	Output Voltage at L3OOO Terminals	I Line = 0 mA		43		V
ILCC	Short Circuit Current		10		14	mA
Iot	Off–hook Detection Threshold		5.6		9.8	mA
Hys	Off–hook/On– hook Hysteresis		1.5		2.5	mA
Vls	Symmetry to Ground	I Line = 0 mA			.75	V

DC OPERATION – NORMAL BATTERY

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
VLO	Output Voltage at L3000 Line Terminals	I Line = 0 mA		43		V
Ilim	Current programmed through the LIM Input	Pin 24 to + 5 V	38	42	46	mA
		Pin 24 to 0 V	56	62	68	mA
Iot	Off–hook Detection Threshold		5.6		9.8	mA
Hys	Off–hook/On–hook Hysteresis		1.5		2.5	mA
Ilgk	Longitudinal Line Current With GDK Detect		6.5		15	mA

SUPPLY CURRENT

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{DD}	Positive Supply Current CS = 1	Power Down Stand-by Conversation Ringing		6.0 7.8 13.2 12.8		mA mA mA mA
I_{SS}	Negative Supply Current CS = 1	Power Down Stand-by Conversation Ringing		5.4 5.4 8.2 8.2		mA mA mA mA
I_{BAT-}	Negative Battery Supply Current Line Current = 0mA	Power Down Stand-by Conversation Ringing		0 2.9 9.8 26	 4 12 28.5	mA mA mA mA
I_{BAT+}	Positive Battery Supply Current Line Current = 0mA	Power Down Stand-by Conversation Ringing		0 10 10 16	 15 15 18.5	mA µA µA mA

AC OPERATION

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Ztx	Sending Output Impedance on TX				15	ohm
THD	Signal Distortion at 2 W and 4 W Terminals	Vtx = 0 dBm@ 1020 Hz			0.5	%
Rl	2 W Return Loss	f = 300 to 3400 Hz	20			dB
Thl	Transhybrid Loss	f = 300 to 3400 Hz	24			dB
Gs	Sending Gain	Vso = 0 dBm f = 1020 Hz	– 0.25		+ 0.25	dB
Gsf	Sending Gain Flatness vs. Frequency	f = 300 to 3400 Hz respect to 1020 Hz	– 0.1		+ 0.1	dB
Gl	Sending Gain Linearity	fr = 1020 Hz Vsoref = – 10 dBm Vso = + 4 / – 40 dBm	– 0.1		+ 0.1	dB
Gr	Receiving Gain	Vri = 0 dBm f = 1020 Hz	– 0.25		+ 0.25	dB
Grf	Receiving Gain Flatness	f = 300 to 3400 Hz Respect to 1020 Hz	– 0.1		+ 0.1	dB
Grl	Receiving Gain Linearity	fr = 1020 Hz Vriref = – 10 dBm Vri = + 4 / – 40 dBm	– 0.1		+ 0.1	dB
Np4W	Psophomet. Noise 4 W– Tx Terminals		– 70	– 75		dBmp
NP2W	Psophomet. at Line Terminals		– 70	– 75		dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB–	f = 10 Hz Vn = 0.7 Vrms		– 20		dB
		f = 1 KHz Vn = 0.7 Vrms			– 40	dB
		f = 3.4 KHz Vn = 0.7 Vrms			– 36	dB
Ltc	Longitudinal to Transversal Conversion	f = 300 to 3400 Hz I Line = 30 mA ZML = 600 ohms	49 (*)	60		dB
Tlc	Transversal to Longitudinal Conversion		49	60		dB

(*) : up to 52dB using selected L3000.

RINGING PHASE

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Vlr	Superimposed DC Voltage	Rloop > 100 Kohms	19		29	V
		Rloop = 1 Kohm	17		27	V
Vacr	Ringing Signal at Line Terminal	Rloop > 100 kOhms V_{RGIN} = 1.5 Vrms/30 Hz	56.0			Vrms
		Rloop = 1 Kohm +1 uF V_{RGIN} = 1.5 Vrms/30 Hz	56.0			Vrms
If	DC Off–hook Det. Threshold			5.5		mA
Ilim	Output Current Capability		85		130	mA
V_{rs}	Ringing Symmetry				2	Vrms
THDr	Ringing Signal Distorsion				5	%
Zir	Ringing Amplicat. Input Impedance	L3090's Pin RGIN	50			Kohm
Vrr	Residual of Ringing Signal at Tx Output				100	mVrms
Trt	Ring Trip Detection Time	fring = 25 Hz (T = 1/fring) CINT = 470 nF		120 (3T)		ms
Toh	Off–hook Status Delay After the Ringing Stop				50	us

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(VDD = + 5 V ; VSS = – 5 V ; Tamb = 25 °C)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Vil	Input Voltage at Logical "0"	Pins CS PWON RNG LIM	0		0.8	V
Vih	Input Voltage at Logical "1"		2,0		5	V
Iil	Input Current at Logical "0"	Vil = 0 V			200	uA
Iih	Input Current at Logical "1"	Vih = 5 V			100	uA
Vol	Output Voltage at Logical "0"	Pins ONHK GDK Iout = – 1 mA			0.4	V
Voh	Output Voltage at Logical "1"	Iout = 1 mA	2.4			V
Ilk	Tristate Leak. Current	CS = "1"			10	uA

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Tsd	PWON, RNG Set up Time to + Edge CS		400			nS
Thd	PWON, RNG Hold Time to + Edge CS		500			nS
Tww	CS Impulse Width (writing Op.)		800			nS
Thv	ONHK, GDK Data Out to "0" CS Delay				600	nS
Tvh	ONHK, GDK High Imped. to "1" CS Delay				600	nS
Twr	CS Impulse Width (writing Op.)		800			nS

Figure 5 : Writing Operation Timing (controller to slic).

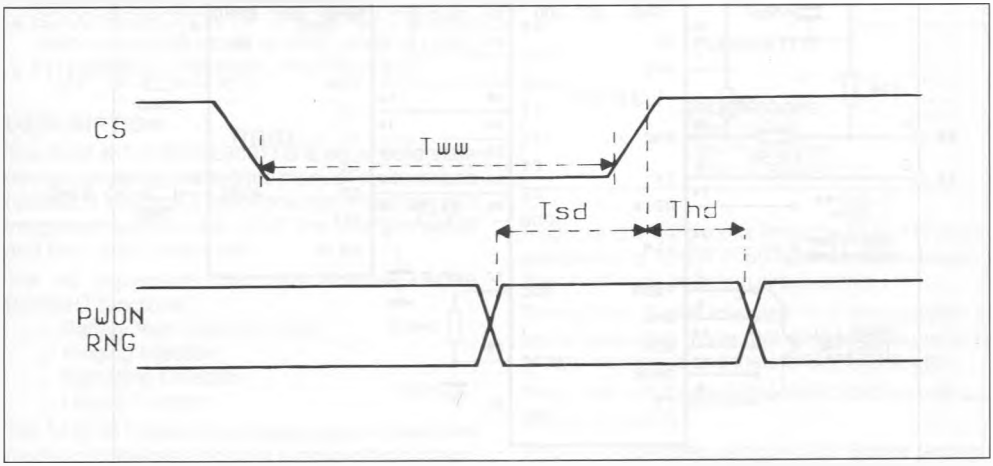


Figure 6 : Reading Operation Timing (from slic to controller).

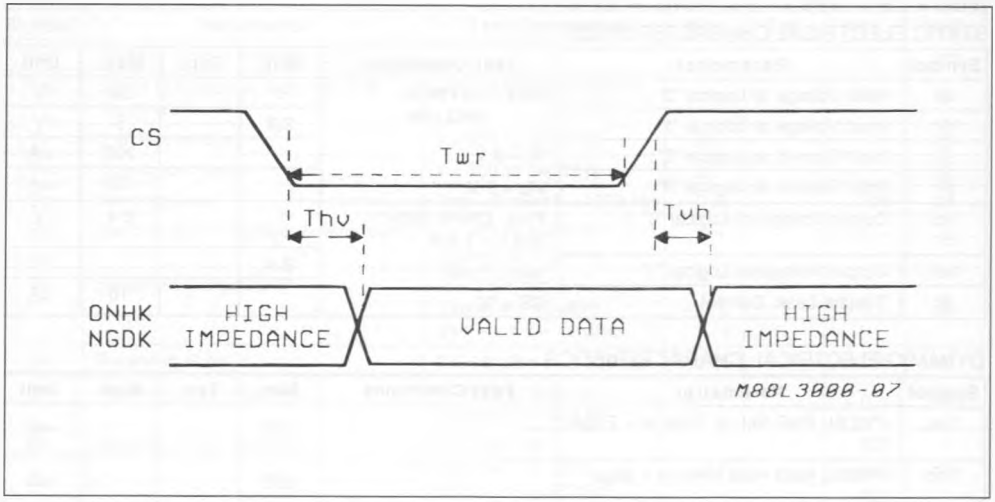
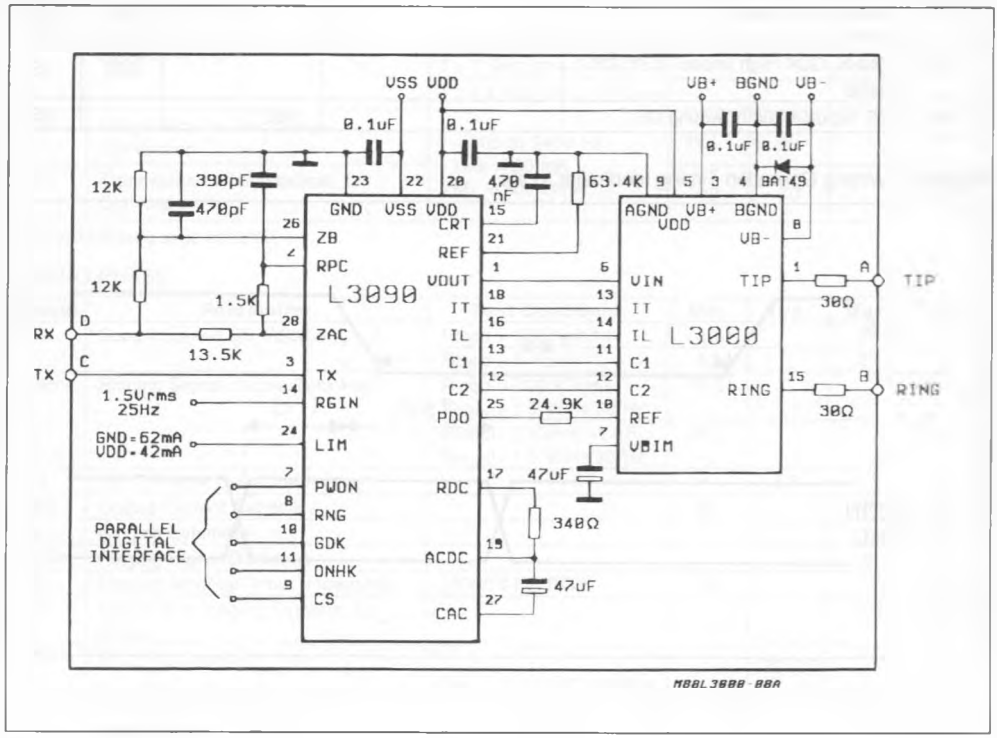


Figure 7 : Test Circuit.



A, B, C, D are test reference points used driving testing.