

## 1.5A POWER SWITCHING REGULATOR

PRELIMINARY DATA

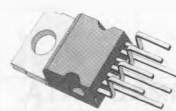
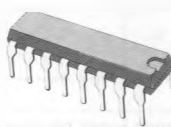
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE ( $\pm 2\%$ ) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage variable from 5V to 40V in step down configuration. Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip

plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.


**Powerdip**

(12 + 2 + 2)

**Heptawatt**
**ORDERING NUMBER :**

L4962 (12 + 2 + 2 Powerdip)

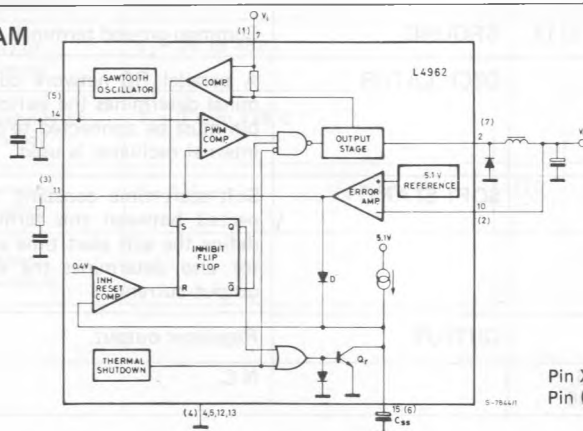
L4962E (Heptawatt)

L4962EH (Horizontal Heptawatt)

### ABSOLUTE MAXIMUM RATINGS

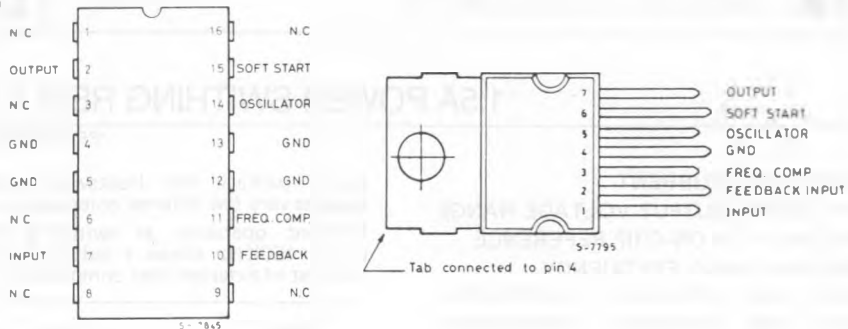
$V_I$	Input voltage	50	V
$V_I - V_2$	Input to output voltage difference	50	V
$V_2$	Negative output DC voltage	-1	V
	Output peak voltage at $t = 0.1\mu s, f = 100KHz$	-5	V
$V_{11}, V_{15}$	Voltage at pin 11, 15	5.5	V
$V_{10}$	Voltage at pin 10	7	V
$I_{11}$	Pin 11 sink current	1	mA
$I_{14}$	Pin 14 source current	20	mA
$P_{tot}$	Power dissipation at $T_{plns} \leq 90^\circ C$ (Powerdip)	4.3	W
	$T_{case} \leq 90^\circ C$ (Heptawatt)	15	W
$T_J, T_{stg}$	Junction and storage temperature	-40 to 150	$^\circ C$

### BLOCK DIAGRAM



Pin X = Powerdip  
 Pin (X) = Heptawatt

CONNECTION DIAGRAMS  
(Top view)



THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ J-case}$	Thermal resistance junction-case	max	4°C/W	14°C/W
$R_{th\ J-pins}$	Thermal resistance junction-pins	max	50°C/W	80°C/W*
$R_{th\ J-amb}$	Thermal resistance junction-ambient	max		

\* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit,  $T_J = 25^\circ\text{C}$ ,  $V_I = 35\text{V}$ , unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### DYNAMIC CHARACTERISTICS

$V_O$	Output voltage range	$V_I = 46\text{V}$ $I_O = 1\text{A}$	$V_{ref}$		40	V
$V_I$	Input voltage range	$V_O = V_{ref}$ to 36V $I_O = 1.5\text{A}$	9		46	V
$\Delta V_O$	Line regulation	$V_I = 10\text{V}$ to 40V $V_O = V_{ref}$ $I_O = 1\text{A}$		15	50	mV
$\Delta V_O$	Load regulation	$V_O = V_{ref}$ $I_O = 0.5\text{A}$ to 1.5A		8	20	mV
$V_{ref}$	Internal reference voltage (pin 10)	$V_I = 9\text{V}$ to 46V $I_O = 1\text{A}$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_J = 0^\circ\text{C}$ to $125^\circ\text{C}$ $I_O = 1\text{A}$		0.4		mV/ $^\circ\text{C}$
$V_d$	Dropout voltage	$I_O = 1.5\text{A}$		1.5	2	V
$I_{om}$	Maximum operating load current	$V_I = 9\text{V}$ to 46V $V_O = V_{ref}$ to 36V	1.5			A
$I_{2L}$	Current limiting threshold (pin 2)	$V_I = 9\text{V}$ to 46V $V_O = V_{ref}$ to 36V	2		3.3	A
$I_{SH}$	Input average current	$V_I = 46\text{V}$ ; output short-circuit		15	30	mA
$\eta$	Efficiency	$f = 100\text{KHz}$ $I_O = 1\text{A}$	$V_O = V_{ref}$		70	%
			$V_O = 12\text{V}$		80	%
SVR	Supply voltage ripple rejection	$\Delta V_I = 2V_{rms}$ $f_{ripple} = 100\text{Hz}$ $V_O = V_{ref}$ $I_O = 1\text{A}$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	$V_I = 9\text{V}$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_J}$	Temperature stability of switching frequency	$T_J = 0^\circ\text{C}$ to $125^\circ\text{C}$		1		%
$f_{max}$	Maximum operating switching frequency	$V_O = V_{ref}$ $I_O = 1\text{A}$	120	150		KHz
$T_{sd}$	Thermal shutdown junction temperature			150		$^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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## DC CHARACTERISTICS

$I_{7Q}$	Quiescent drain current	100% duty cycle pins 2 and 14 open	$V_I = 46V$		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA

## SOFT START

$I_{15SO}$	Source current		100	130	160	$\mu A$
$I_{15SI}$	Sink current		50	70	120	$\mu A$

## ERROR AMPLIFIER

$V_{11H}$	High level output voltage	$V_{10} = 4.7V$	$I_{11} = 100\mu A$	3.5			V
$V_{11L}$	Low level output voltage	$V_{10} = 5.3V$	$I_{11} = 100\mu A$			0.5	V
$I_{11SI}$	Sink output current	$V_{10} = 5.3V$		100	150		$\mu A$
$-I_{11SO}$	Source output current	$V_{10} = 4.7V$		100	150		$\mu A$
$I_{10}$	Input bias current	$V_{10} = 5.2V$			2	10	$\mu A$
$G_v$	DC open loop gain	$V_{11} = 1V$ to $3V$		46	55		dB

## OSCILLATOR

$-I_{14}$	Oscillator source current		5			mA
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## CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to  $\pm 2\%$ ).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor  $C_{ss}$  and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about  $150^{\circ}\text{C}$  and has hysteresis to prevent unstable conditions.

Fig. 1 – Soft start waveforms

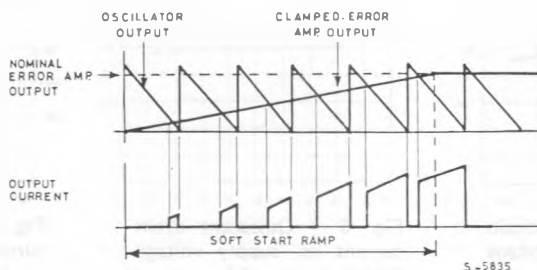


Fig. 2 – Current limiter waveforms

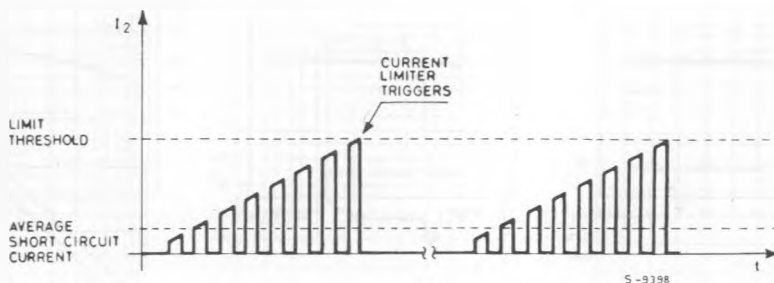
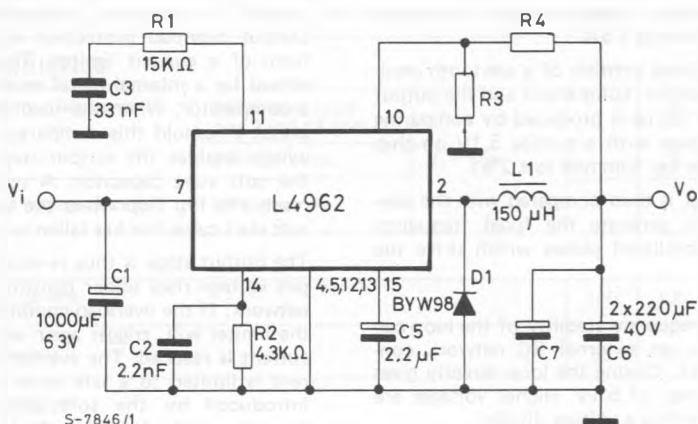


Fig. 3 - Test and application circuit (Powerdip)



- 1) D<sub>1</sub>: BYW98 or 3A Schottky diode, 45V of VRRM;
- 2) L<sub>1</sub>: CORE TYPE - MAGNETICS 58120 - A2 MPP  
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
- 3) C<sub>6</sub>, C<sub>7</sub>: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

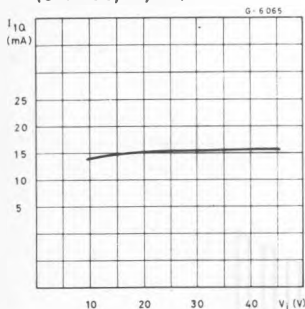


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

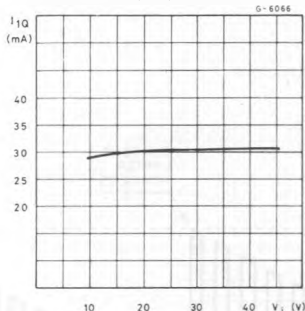


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

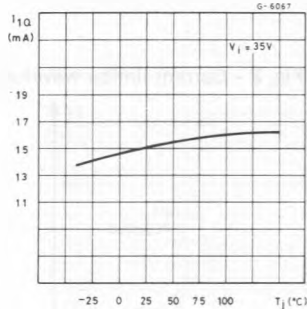


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

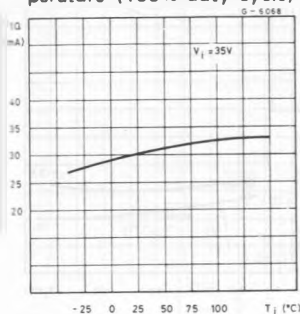


Fig. 8 - Reference voltage (pin 10) vs.  $V_I$  rdip) vs.  $V_I$

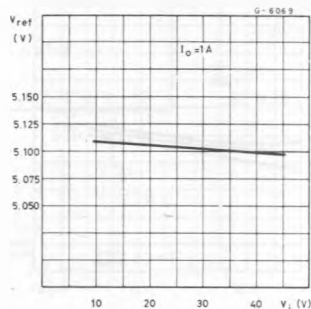


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

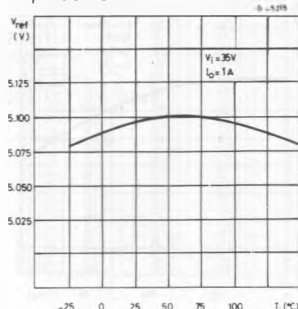


Fig. 10 - Open loop frequency and phase response of error amplifier

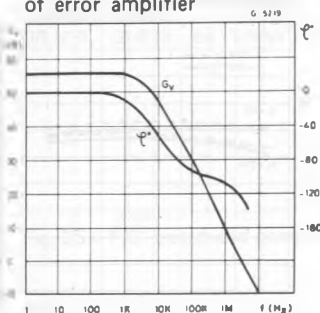


Fig. 11 - Switching frequency vs. input voltage

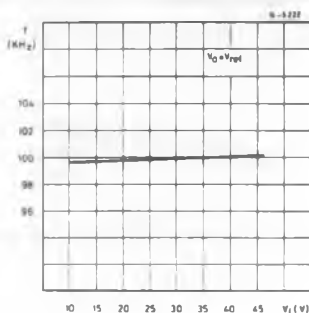


Fig. 12 - Switching frequency vs. junction temperature

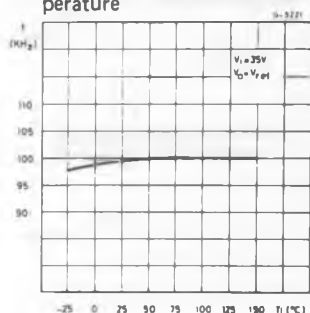


Fig. 13 - Switching frequency vs.  $R_2$  (see test circuit)

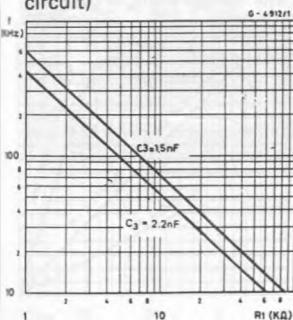


Fig. 14 - Line transient response

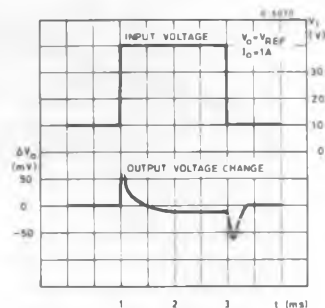


Fig. 15 - Load transient response

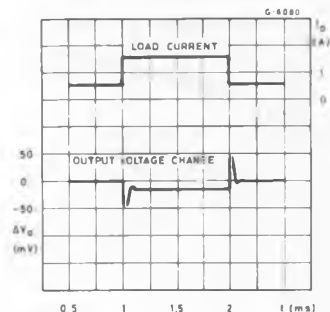


Fig. 16 - Supply voltage ripple rejection vs. frequency

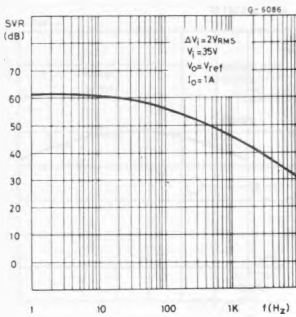


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

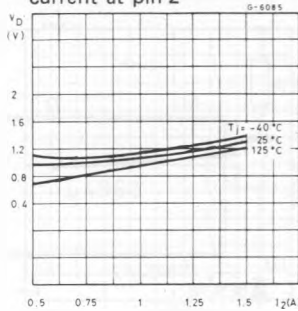


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

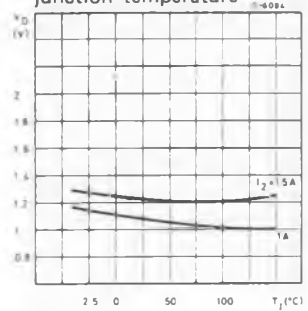


Fig. 19 - Efficiency vs. output current

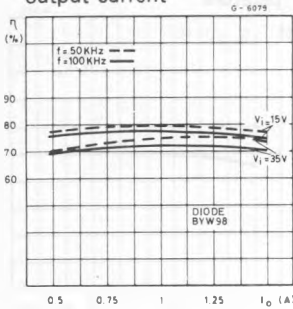


Fig. 20 - Efficiency vs. output current

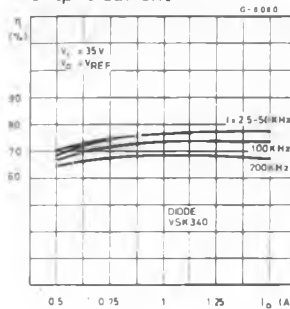


Fig. 21 - Efficiency vs. output current

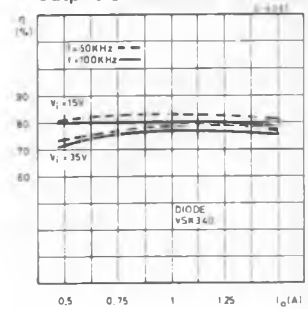


Fig. 22 - Efficiency vs. output voltage

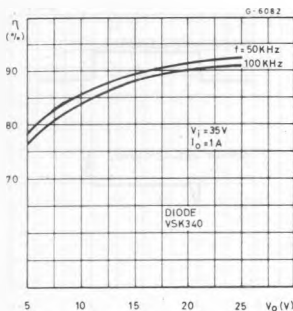


Fig. 23 - Efficiency vs. output voltage

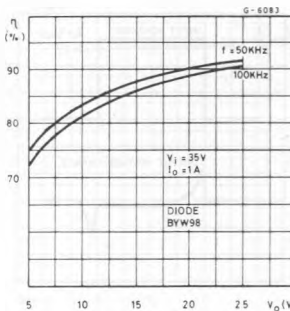
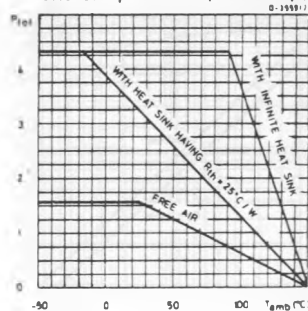


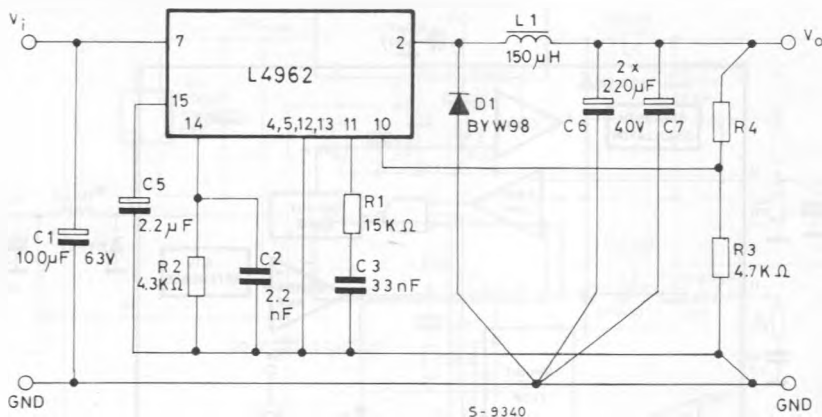
Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)





## APPLICATION INFORMATION

Fig. 25 – Typical application circuit



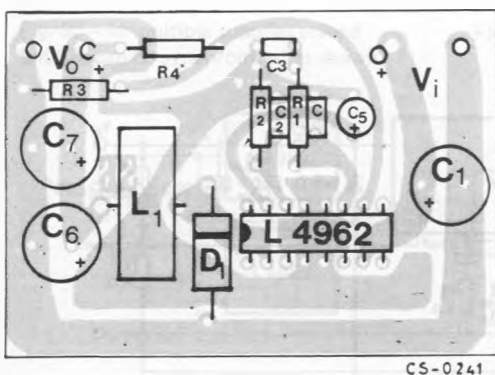
C<sub>1</sub>, C<sub>6</sub>, C<sub>7</sub>: EKR (ROE)

D<sub>1</sub>: BYW98 OR VISK340 (SCHOTTKY)

SUGGESTED INDUCTORS (L<sub>1</sub>): MAGNETICS 68120 – A2MPP – 45 TURNS – wire GAUGE 0.8mm (20AWG) – COGEMA 946043

OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) – COGEMA 969051

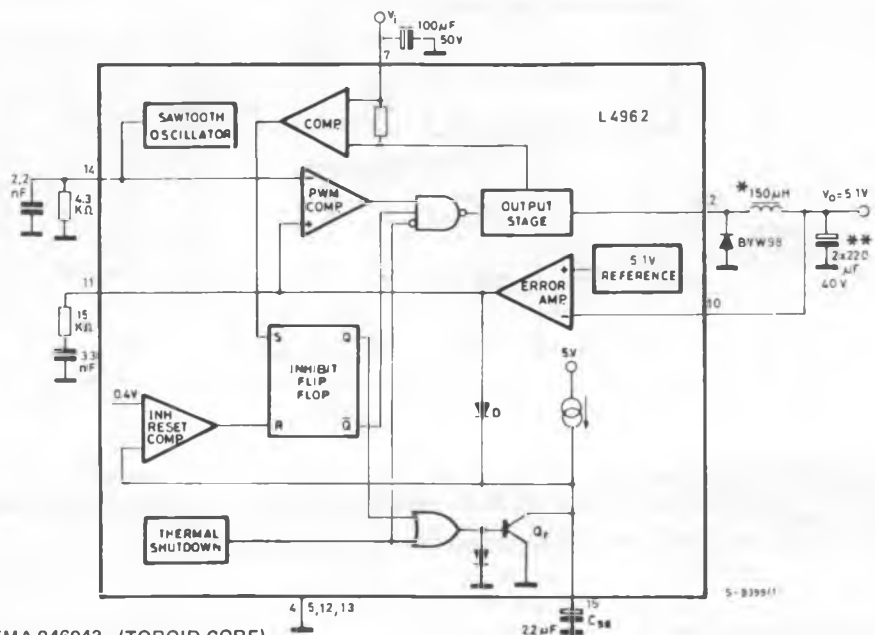
Fig. 26 – P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)

Resistor values for  
standard output 7 voltages

V <sub>O</sub>	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

# APPLICATION INFORMATION (continued)

Fig. 27 - A minimal 5.1V fixed regulator; very few components are required

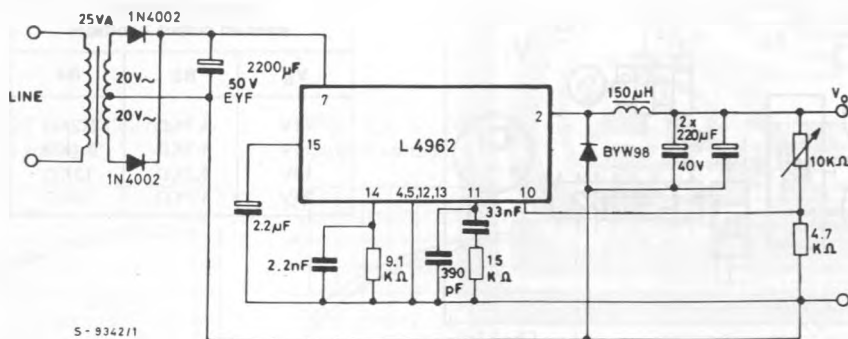


\* COGEMA 946043 (TOROID CORE)

969051 (U15 CORE)

\*\* EKR (ROE)

Fig. 28 - Programmable power supply



$V_O = 5.1V \text{ to } 15V$

$I_O = 1.5A \text{ max}$

Load regulation (0.5A to 1.5A) = 10mV ( $V_O = 5.1V$ )

Line regulation (220V  $\pm$  15% and to  $I_O = 1A$ ) = 15mV ( $V_O = 5.1V$ )

## APPLICATION INFORMATION (continued)

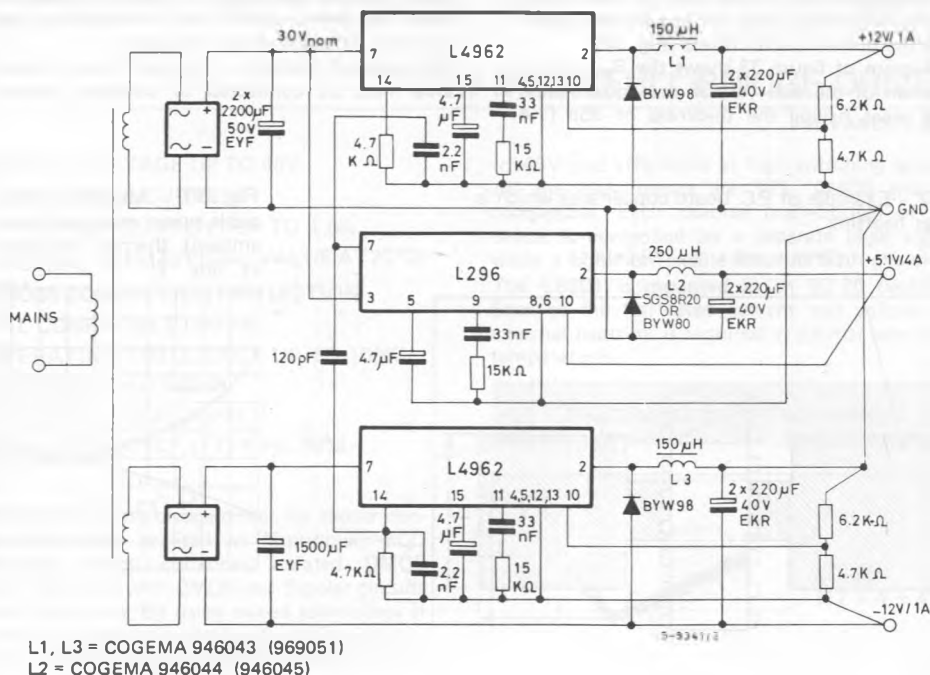
Fig. 29 – DC-DC converter 5.1V/4A,  $\pm 12V/1A$ . A suggestion how to synchronize a negative output

Fig. 30 – In multiple supplies several L4962s can be synchronized as shown

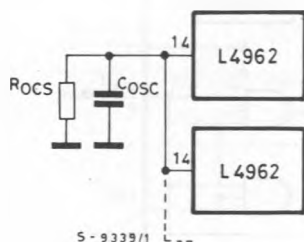
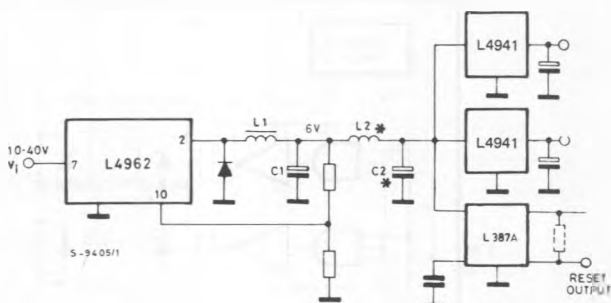


Fig. 31 – Preregulator for distributed supplies



\* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The  $R_{thj-amb}$  of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32). The diagram of figure 33 shows the  $R_{thj-amb}$  as a function of the side "Q" of two equal square copper areas having the thickness of  $35\mu$  (1.4

mils). During soldering the pins temperature must not exceed  $260^{\circ}\text{C}$  and the soldering time must not be longer than 12 seconds. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 – Example of P.C. board copper area which is used as heatsink

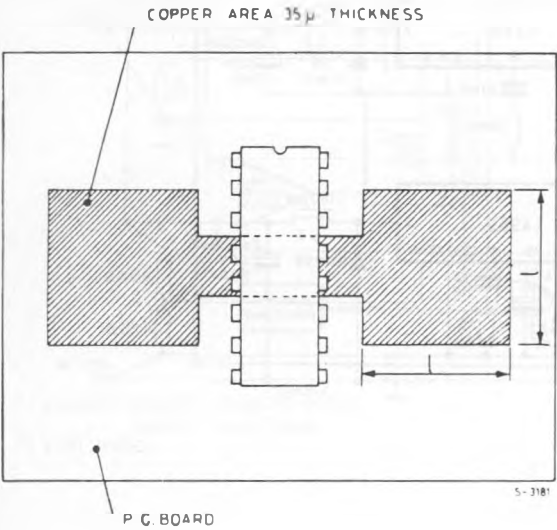


Fig. 33 – Maximum dissippable power and junction to ambient thermal resistance vs. side "Q"

