SGS-THOMSON MICROELECTRONICS

L4970

10 A SWITCHING REGULATOR

ADVANCE DATA

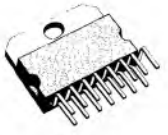
- 10 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 90 % DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1 V +/- 2 % ON CHIP REFERENCE
- RESET AND P. FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500 KHz
- THERMAL SHUTDOWN

DESCRIPTION

The L4970 is a stepdown monolithic power switching regulator delivering 10 A at a voltage variable from 5.1 to 40 V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500 KHz allows reduction in the size and cost of external filter components.

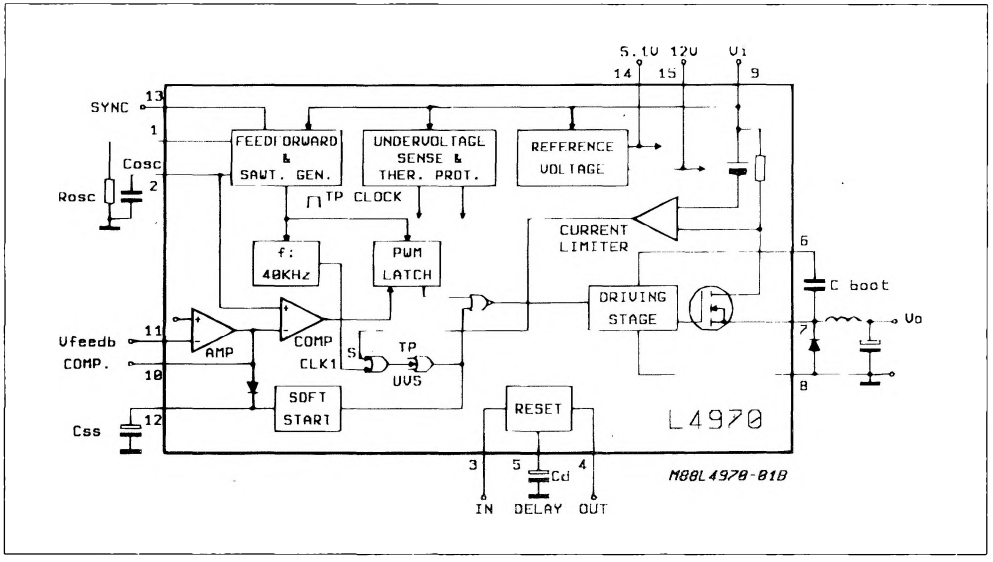
MultiPower BCD Technology



Multiwatt 15

ORDER CODE : L4970

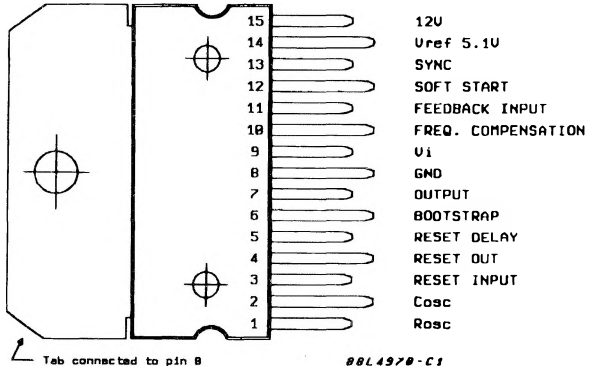
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1 µs f = 200 KHz	– 1 – 7	V V
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{11}, V_{12}	Input Voltage at Pins 3, 11, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{13}	Input Voltage at Pin 5, 10, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	10	mA
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120 °C	30	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top views)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1 V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external resistor when not used.
4	RESET OUT	Open Collector Reset/Power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output.
8	GROUND	Common Ground Terminal.
9	SUPPLY VOLTAGE	Unregulated Voltage Input.
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4970's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage.
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage.

Figure 1 : Feedforward Waveform.

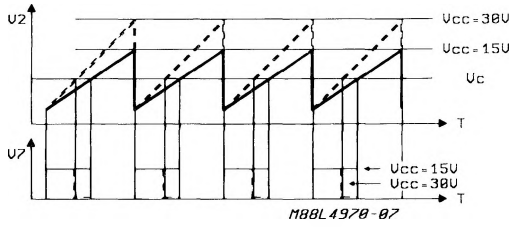


Figure 2 : Soft Start Function.

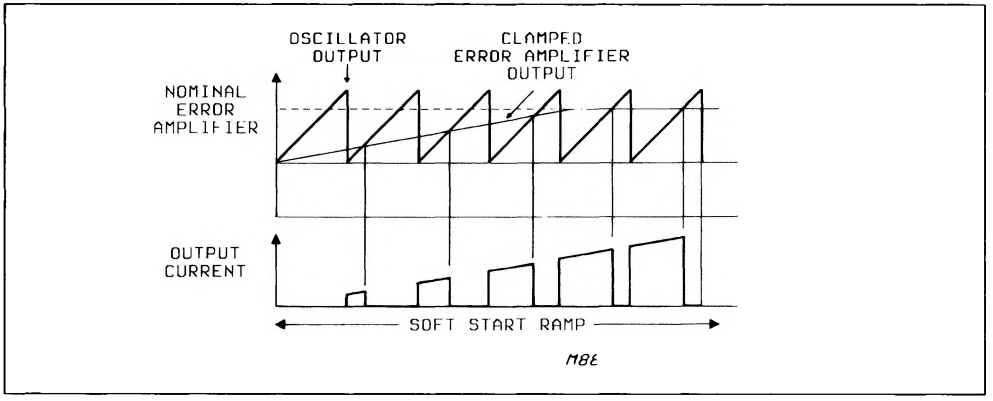


Figure 3 : Limiting Current Function.

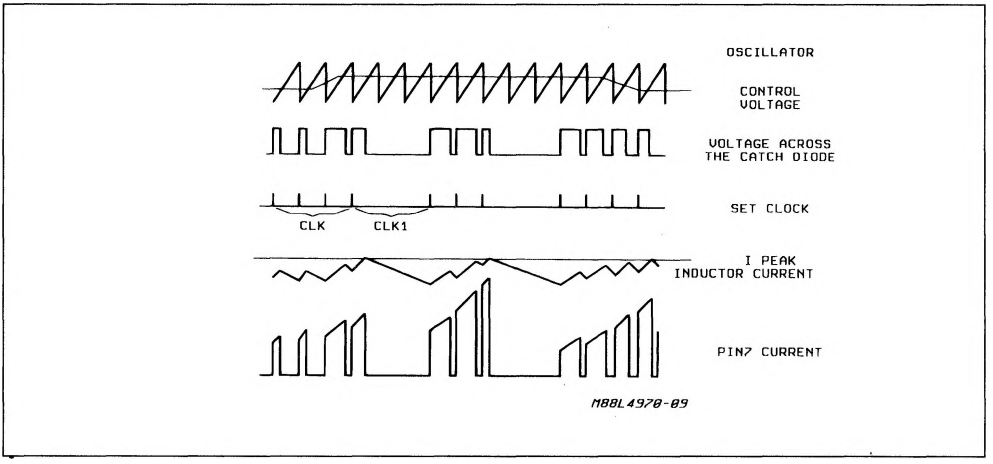
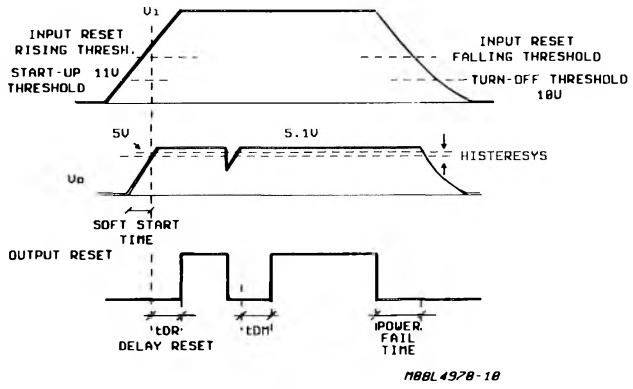
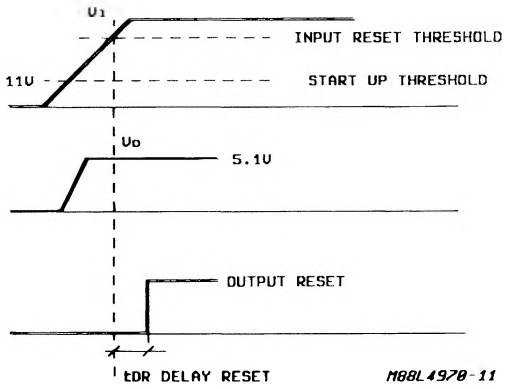


Figure 4 : Reset and Power Fall Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_j = 25 °C, V_i = 35 V, f = 200 kHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS							
V_i	Input Volt. Range (pin 9)	$V_o = V_{ref}$ to 40 V I_o = 10 A	15		50	V	5
V_o	Output Voltage	V_i = 15 V to 50 V I_o = 5 A ; $V_o = V_{ref}$	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15 V to 50 V I_o = 2 A ; $V_o = V_{ref}$		12	30	mV	5
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 3 A to 6 A I_o = 2 A to 10 A		10 20	30 50	mV mV	5
V_{REF} SECTION (pin 14)							
V_{REF}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{REF}	Line Regulation	V_i = 15 V to 50 V V_{12} = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3 mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff. Ref. Voltage	T_j = 0 °C to 125 °c		0.4		mV/C	7
I_{REF}	Short Circuit Curr. Limit	V_{REF} = 0		70		mA	7
V_{START} SECTION (pin 15)							
V_{ref}	Reference Voltage	P_{12} = 0 V	11.4	12	12.6	V	7
ΔV_{ref}	Line Regulation	P_{12} = 0 V ; V_i = 15 to 50 V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1 mA P_{12} = 0 V		50	200	mV	7
I_{ref}	Short Circuit Current Limit	P_{12} = 0 V ; P_{15} = 0 V		80		mA	7
V_d	Dropout Voltage between Pin 9 and 7	I_o = 5 A I_o = 10 A		0.55 1.1	0.8 1.6	V V	5
I_{7L}	Max Limiting Current	V_i = 15 V to 50 V $V_o = V_{ref}$ to 40 V	11	12.5	14	A	5
Efficiency		I_o = 5 A $V_o = V_{ref}$ V_o = 12 V	80	85 92		% %	5
		I_o = 10 A $V_o = V_{ref}$ V_o = 12 V	75	80 87		%	5

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SVR	Supply Voltage Ripple Reject.	V_i = 2 VRMS ; I_o = 5 A f = 100 Hz ; V_o = Vref	56	60		dB	5
f	Switching Freq.	R = 15 KΩ ; C = 2.2 nF	180	200	220	KHz	5
$\Delta f/_{\Delta Vi}$	Volt. Stability of Switching Freq.	V_i = 15 V to 45 V		2	6	%	5
$\Delta f/_{T_j}$	Temp. Stability of Switch. Freq.	T_j = 0 to 125 °C		1		%	5
f_{max}	Max. Operating Switch. Freq.	$V_o = V_{ref}$ I_o = 10 A	500			KHz	5

DC CHARACTERISTICS

V_{9on}	Turn–on Thresh.		10	11	12	V	7A
V_{9Hyst}	Turn–off Hyster.			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0 ; S1 = D ; S2 = C ; S4 = A		10	16	mA	7A
I_{9OQ}	Operating Quiescent Curr.	V_{12} = 0 f = 200 KHz		16	20	mA	7A
I_{7L}	Out Leak Current	V_i = 55 V ; S3 = A ; V_{12} = 0 V ; f = 200 KHz			2	mA	7A

SOFT START (pin 12)

I_{12}	Soft Start Source Current	V_{12} = 3 V ; V_{11} = 0 V	70	100	130	µA	7B
V_{12s}	Output Saturation Voltage	I_{12s} = 20 mA ; V_9 = 10 V			0.7	V	7B

ERROR AMPLIFIER

V_{10H}	High Level out Voltage	I_{10} = – 50µA ; S2 = A P_{11} = 0 V ; S1 = C	6			V	7C
V_{10L}	Low Level out Voltage	I_{10} = 50µA ; S2 = A P_{11} = 6 V ; S1 = C			0.7	V	7C
I_{11}	Input Bias Current	V_{11} = 5 ; S1 = B ; R_S = 10 K		2	10	uA	7C
VOS	Input off Voltage	P_{11} = Vos ; R_s = 50 Ω ; S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	P_{VCM} = 4 V ; R_S = 50 Ω ; S1 = A	60			dB	7C
SVR	Supply Volt. Rej.	15 < Vi < 50 V	60	80		dB	7C

RAMP GENERATOR (pin 2)

	Ramp Valley			1.5		V	7A
	Ramp Peak	V_i = 15 V V_i = 45 V		2.5 5.5		V V	7A
	MIn Ramp Current	S1 = A ; I1 = 100 µA		270	300	µA	7A
	Max Ramp Current	S1 = A ; I1 = 1 mA	2.4	2.7		mA	7A

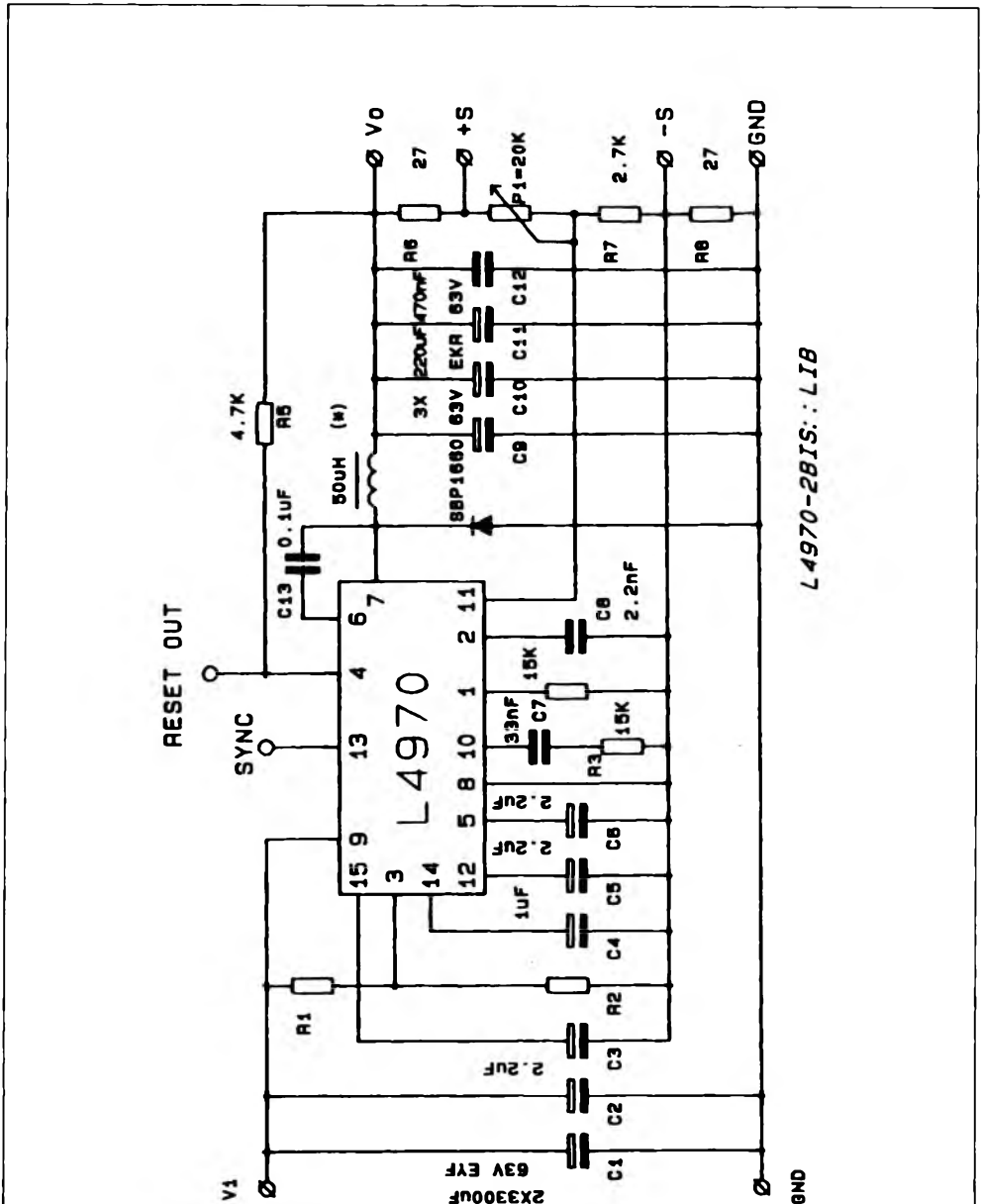
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_i = 15 V to 50 V	− 0.3		0.9	V	
SYNC	High Input Voltage	V_{12} = 0	3.5		5.5	V	
$-I_{13L}$	Sync Input Current with Low Input Voltage	V_{13} = 0.9 V			0.4	mA	
$-I_{13H}$	Input Current with High Input Voltage	V_{13} = 3.5 V			1.5	mA	
SYNC	Delay			50		ns	
	Output Amplitude			5		V	
	Output Pulse Width			0.5		µsec.	

RESET AND P. FAIL FUNCTIONS

V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50 V S1 = B	Vref − 150	Vref − 100	Vref − 50	V mV	7D
	Hysteresis	S1 = B	80	100	120	mV	7D
V_{5H}	Delay High Threshold Voltage	S1 = B	5	5.1	5.2	V	7D
V_{5L}	Delay Low Threshold Voltage	S1 = B	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3 V ; V_5 = 3 V S1 = A	40	55	70	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7 V ; V_5 = 3 V S1 = A	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15 mA ; S2 = B			0.4	V	7D
I_4	Output Leak Current	V_4 = 50 V ; S2 = A			100	µA	7D
V_{3R}	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit.



(*) core 58930 MAGNETICS
N. turns : 18
Wire gauge : 4x0.75 mm (21 AWG)

Figure 6 : Mockup of the Circuit of Fig. 5 (1.1 scale).

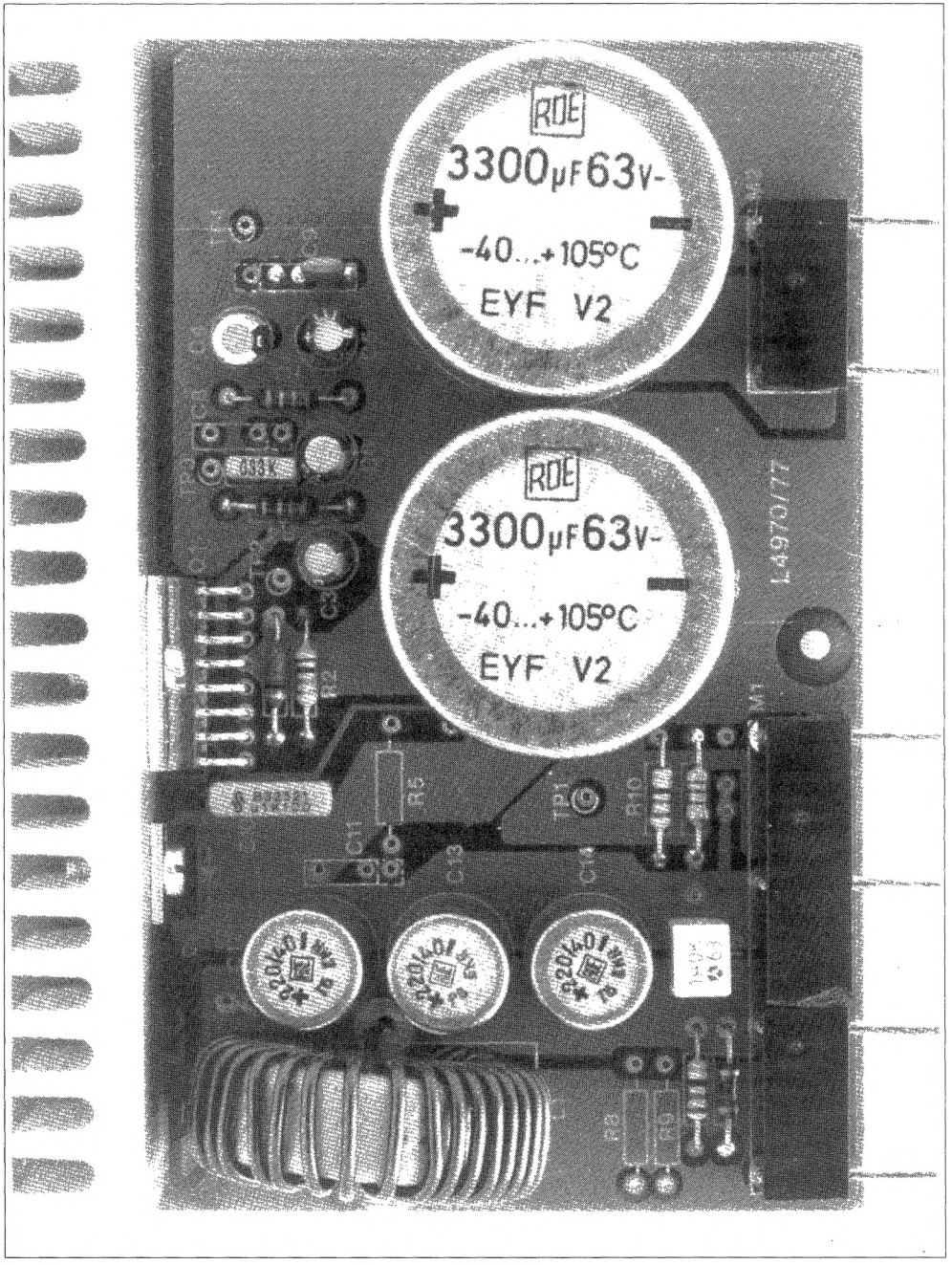


Figure 7 : DC Test Circuits.

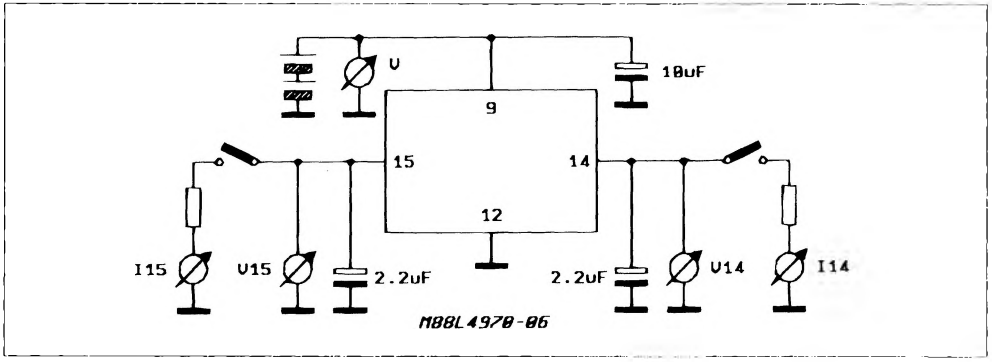


Figure 7A.

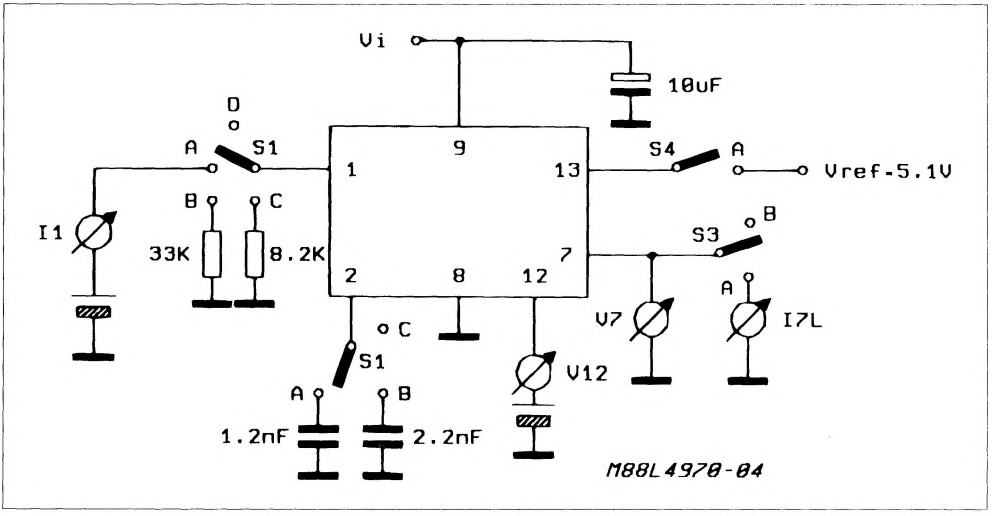


Figure 7B.

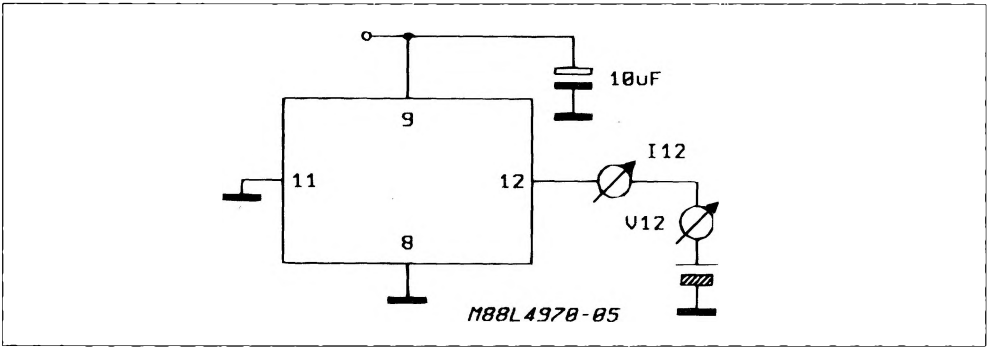


Figure 7C.

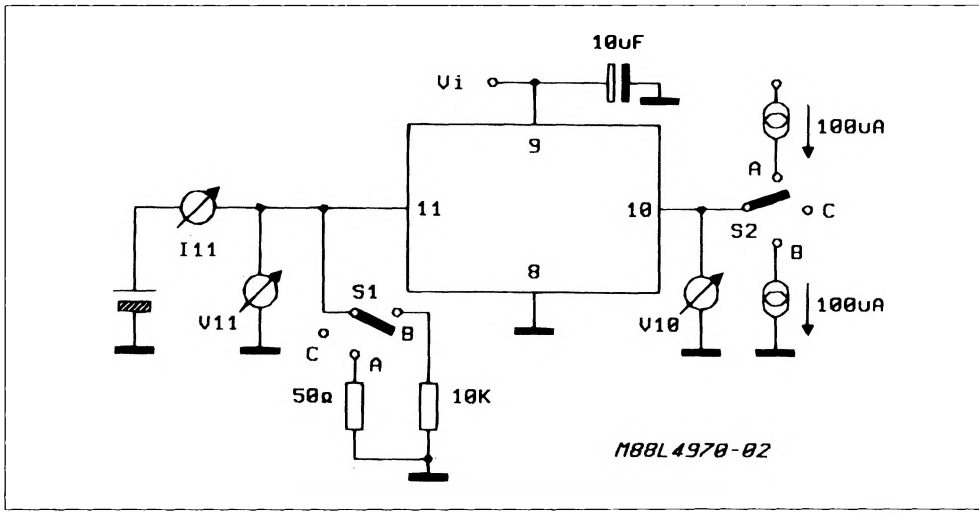


Figure 7D.

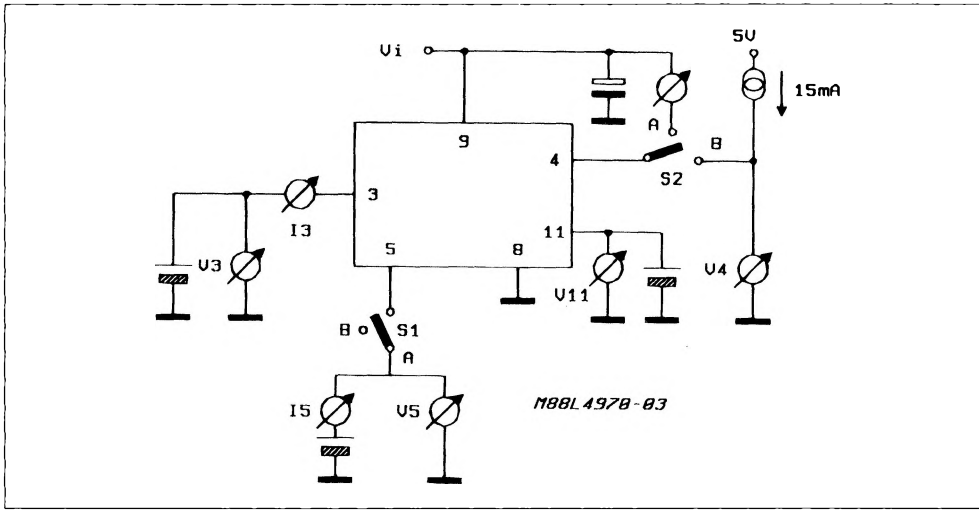


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0 % duty cycle - see fig. 7A).

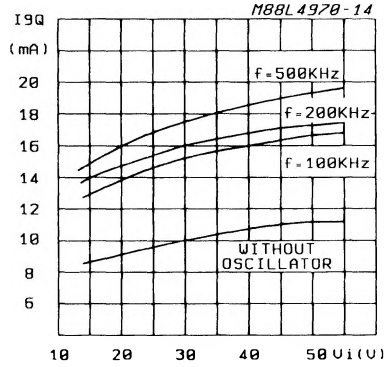


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % duty cycle).

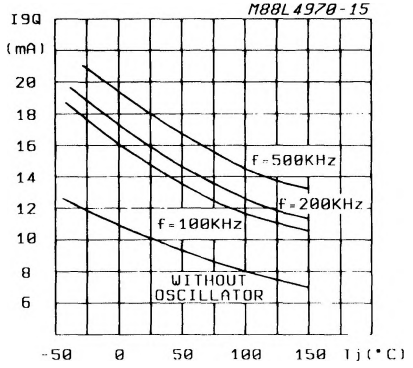


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

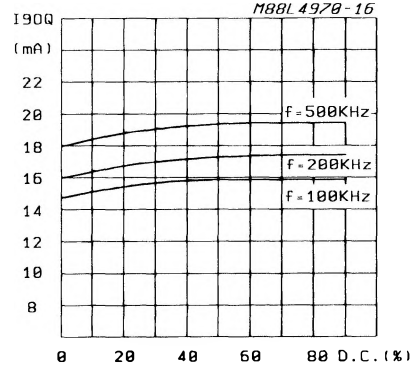


Figure 11 : Reference Voltage (pin 14) vs. V_i (see fig. 7).

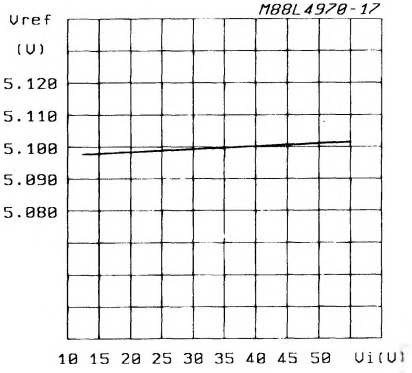


Figure 12 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

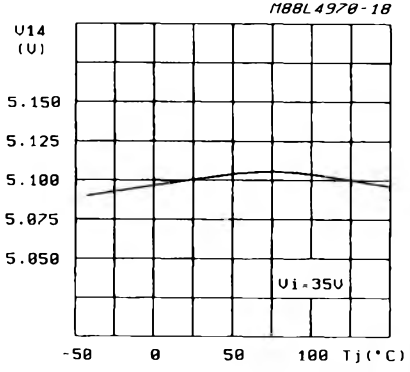


Figure 13 : Reference Voltage (pin 15) vs. V_i (see fig. 7).

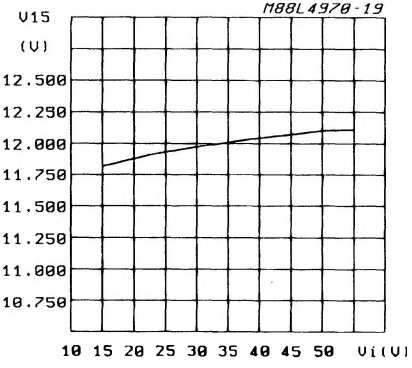


Figure 14 : Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7).

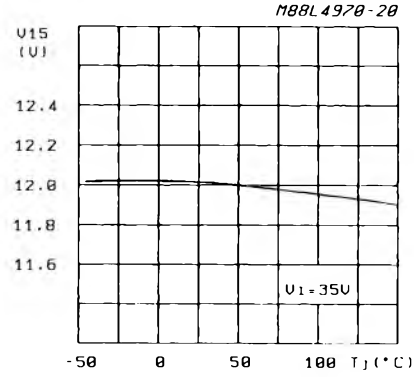


Figure 15 : Switching Frequency vs. Input Voltage (see fig. 5).

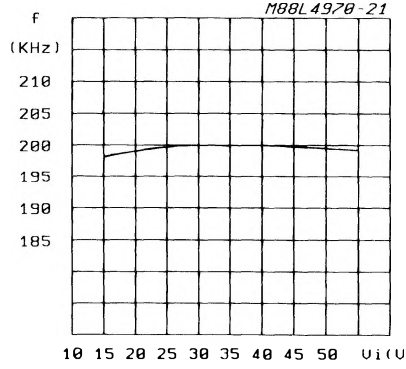


Figure 16 : Switching Frequency vs. Junction Temperature (see fig. 5).

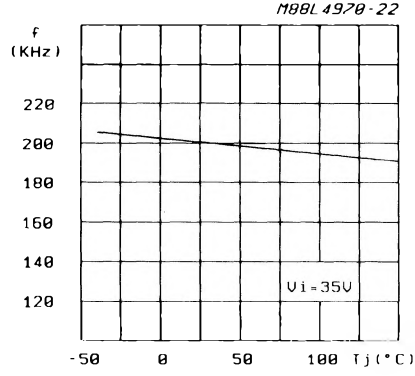


Figure 17 : Switching Frequency vs. R4 (see fig. 5).

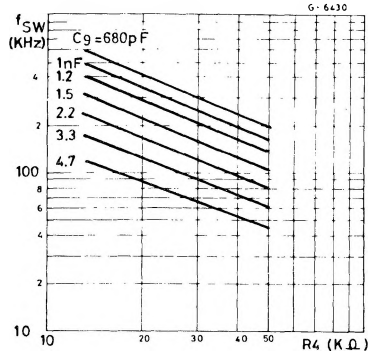


Figure 18 : Line Transient Response (see fig. 5).

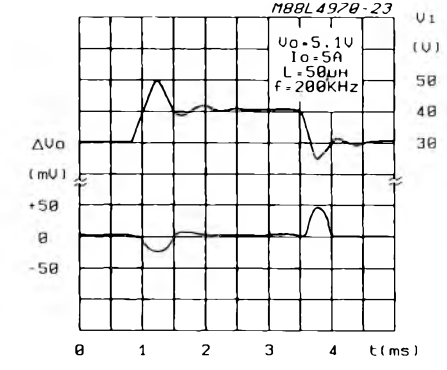


Figure 19 : Load Transient Response (see fig. 5).

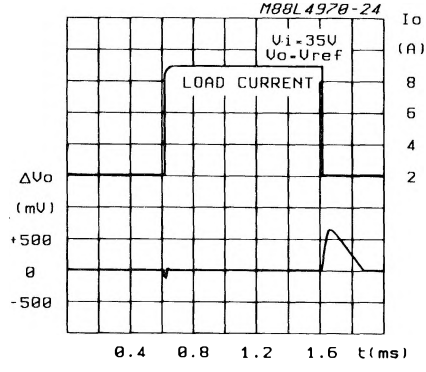


Figure 20 : Dropout Voltage between Pin 9 and Pin 7 vs. Current at Pin 7.

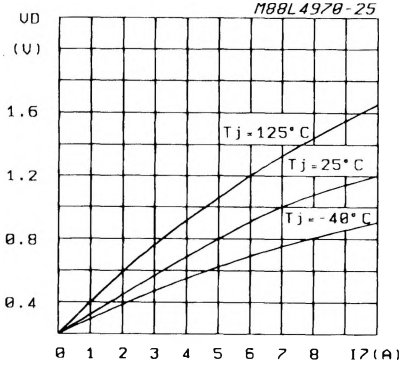


Figure 21 : Dropout Voltage between Pin 9 and Pin 7 vs. Junction Temperature.

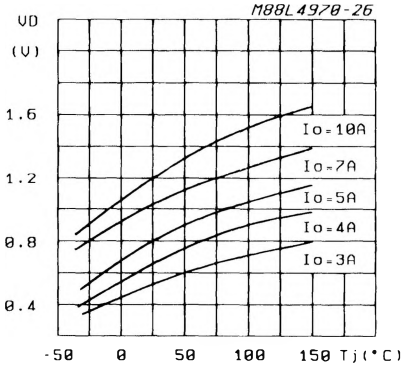


Figure 22 : Power Dissipation (device only) vs. Input Voltage.

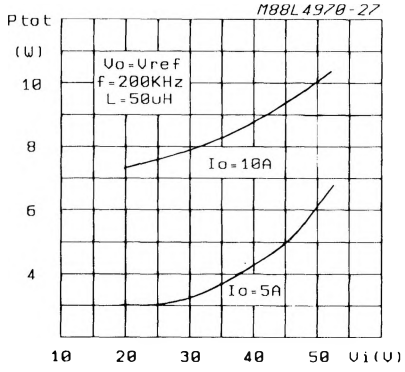


Figure 23 : Power Dissipation (device only) vs. Output Voltage.

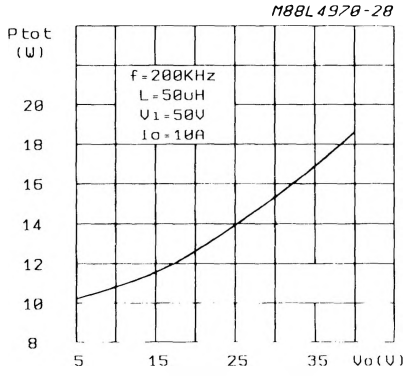


Figure 24 : Efficiency vs. Output Current.

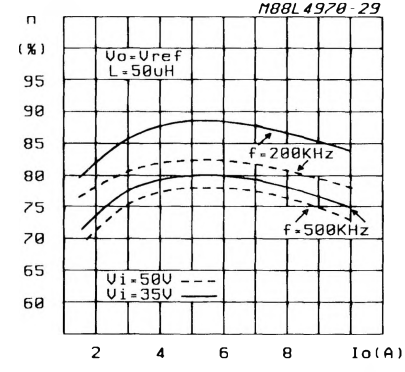


Figure 25 : Efficiency vs. Output Voltage.

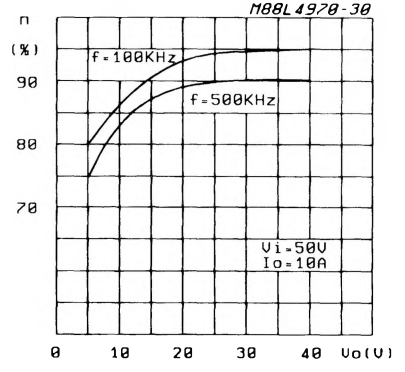


Figure 26 : Power Dissipation Derating Curve.

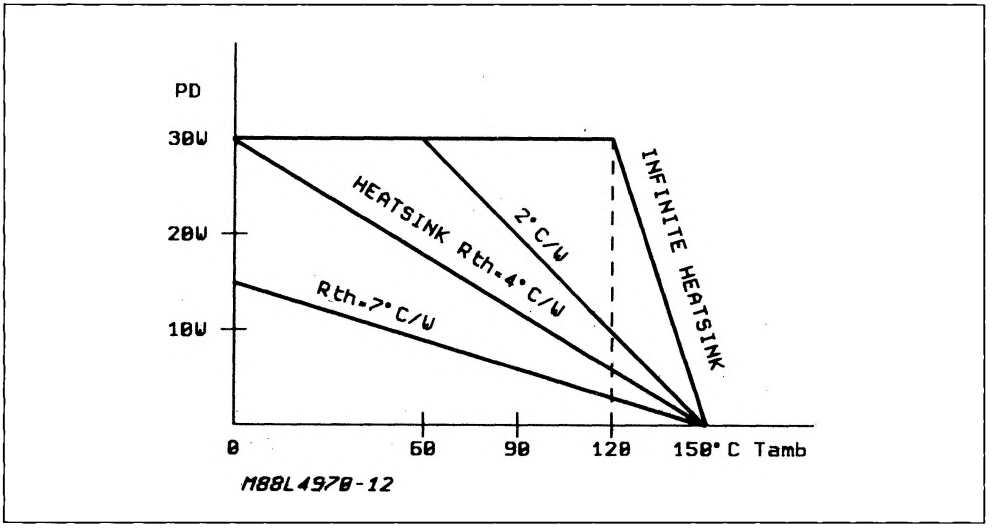
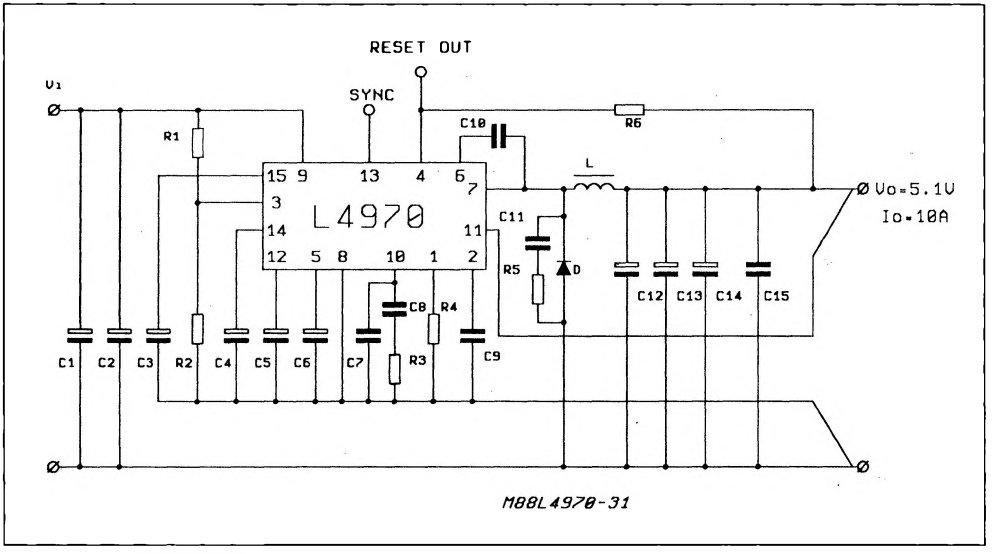


Figure 27 : 10 A - 5.1 V Application Circuit.



TYPICAL PERFORMANCES :

n = 83 % (V_i = 35 V ; V_o = V_{REF} ; I_o = 10 A ; f_{SW} = 200 KHz)

$V_{o\ RIPPLE}$ = 30 mV (at 10 A)

Line regulator = 5 mV (V_i = 15 to 50 V)

Load regulator = 15 mV (I_o = 2 to 10 A)